

# MC10ELT21, MC100ELT21

## 5 V Differential PECL to TTL Translator

### Description

The MC10ELT/100ELT21 is a differential PECL to TTL translator. Because PECL (Positive ECL) levels are used, only +5 V and ground are required. The small outline 8-lead package and the single gate of the ELT21 makes it ideal for those applications where space, performance and low power are at a premium.

The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu$ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

The 100 Series contains temperature compensation.

### Features

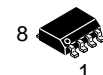
- 3.5 ns Typical Propagation Delay
- 24 mA TTL Output
- Flow Through Pinouts
- Operating Range:  $V_{CC} = 4.75$  V to 5.25 V with GND = 0 V
- Q Output Will Default LOW with Inputs Left Open or < 1.3 V
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



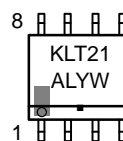
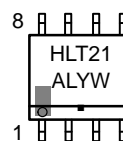
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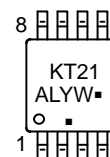
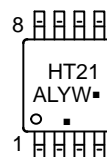
### MARKING DIAGRAMS\*



**SOIC-8**  
**D SUFFIX**  
**CASE 751**



**TSSOP-8**  
**DT SUFFIX**  
**CASE 948R**



H = MC10  
K = MC100

A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

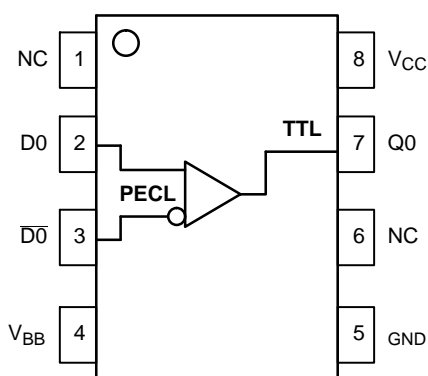
(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# MC10ELT21, MC100ELT21



**Figure 1. 8-Lead Pinout and Logic Diagram**  
(Top View)

**Table 1. PIN DESCRIPTION**

| Pin                 | Function                  |
|---------------------|---------------------------|
| Q0                  | TTL Outputs               |
| D0, $\overline{D0}$ | PECL Differential Outputs |
| $V_{BB}$            | Reference Voltage Output  |
| $V_{CC}$            | Positive Supply           |
| GND                 | Ground                    |
| NC                  | No Connect                |

**Table 2. ATTRIBUTES**

| Characteristics   | Value                |
|---|----------------------|
| Internal Input Pulldown Resistor                              | 50 k $\Omega$        |
| Internal Input Pullup Resistor                                | N/A                  |
| ESD Protection Human Body Model                               | > 2 kV               |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | Pb-Free Pkg          |
| SOIC-8<br>TSSOP-8   | Level 1<br>Level 3   |
| Flammability Rating Oxygen Index: 28 to 34                    | UL 94 V-0 @ 0.125 in |
| Transistor Count  | 81 Devices           |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test        |                      |

1. For additional information, see Application Note AND8003/D.

**Table 3. MAXIMUM RATINGS**

| Symbol           | Parameter                                | Condition 1                          | Condition 2        | Rating      | Unit   |
|------------------|--|--------------------------------------|--------------------|-------------|--|
| $V_{CC}$         | PECL Power Supply                        | GND = 0 V                            |                    | 7           | V  |
| $V_{IN}$         | PECL Input Voltage                       | GND = 0 V                            | $V_I \leq V_{CC}$  | 0 to 6      | V  |
| $I_{BB}$         | $V_{BB}$ Sink/Source                     |                                      |                    | $\pm 0.5$   | mA   |
| TA               | Operating Temperature Range              |                                      |                    | -40 to +85  | $^{\circ}\text{C}$                           |
| T <sub>stg</sub> | Storage Temperature Range                |                                      |                    | -65 to +150 | $^{\circ}\text{C}$                           |
| $\theta_{JA}$    | Thermal Resistance (Junction-to-Ambient) | 0 lfpm<br>500 lfpm                   | SOIC-8<br>SOIC-8   | 190<br>130  | $^{\circ}\text{C/W}$<br>$^{\circ}\text{C/W}$ |
| $\theta_{JC}$    | Thermal Resistance (Junction-to-Case)    | Standard Board                       | SOIC-8             | 41 to 44    | $^{\circ}\text{C/W}$                         |
| $\theta_{JA}$    | Thermal Resistance (Junction-to-Ambient) | 0 lfpm<br>500 lfpm                   | TSSOP-8<br>TSSOP-8 | 185<br>140  | $^{\circ}\text{C/W}$<br>$^{\circ}\text{C/W}$ |
| T <sub>sol</sub> | Wave Solder Pb-Free                      | <2 to 3 sec @ 260 $^{\circ}\text{C}$ |                    | 265         | $^{\circ}\text{C}$                           |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

# MC10ELT21, MC100ELT21

**Table 4. 10ELT SERIES PECL INPUT DC CHARACTERISTICS**  $V_{CC} = 5.0 \text{ V}$ ;  $GND = 0.0 \text{ V}$  (Note 2)

| Symbol      | Characteristic   | -40°C |     |      | 25°C |     |      | 85°C |     |      | Unit          |
|-------------|--|-------|-----|------|------|-----|------|------|-----|------|---------------|
|             |  | Min   | Typ | Max  | Min  | Typ | Max  | Min  | Typ | Max  |               |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)  | 3770  |     | 4110 | 3870 |     | 4190 | 3930 |     | 4265 | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)   | 3050  |     | 3500 | 3050 |     | 3520 | 3050 |     | 3555 | mV            |
| $V_{BB}$    | Output Voltage Reference   | 3.57  |     | 3.7  | 3.65 |     | 3.75 | 3.69 |     | 3.81 | V             |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | 2.2   |     | 5.0  | 2.2  |     | 5.0  | 2.2  |     | 5.0  | V             |
| $I_{IH}$    | Input HIGH Current   |       |     | 255  |      |     | 175  |      |     | 175  | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current  | 0.5   |     |      | 0.5  |     |      | 0.3  |     |      | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

2. Output parameters vary 1:1 with  $V_{CC}$ .  $V_{CC}$  can vary  $\pm 0.25 \text{ V}$ .

3.  $V_{IHCMR}$  min varies 1:1 with  $GND$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ .

**Table 5. 100ELT SERIES PECL INPUT DC CHARACTERISTICS**  $V_{CC} = 5.0 \text{ V}$ ;  $GND = 0.0 \text{ V}$  (Note 4)

| Symbol      | Characteristic   | -40°C |     |      | 25°C |     |      | 85°C |     |       | Unit          |
|-------------|--|-------|-----|------|------|-----|------|------|-----|-------|---------------|
|             |  | Min   | Typ | Max  | Min  | Typ | Max  | Min  | Typ | Max   |               |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)  | 3835  |     | 4120 | 3835 |     | 4120 | 3835 |     | 4120  | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)   | 3190  |     | 3525 | 3190 |     | 3525 | 3190 |     | 3525  | mV            |
| $V_{BB}$    | Output Voltage Reference   | 3.62  |     | 3.74 | 3.62 |     | 3.74 | 3.62 |     | 3.745 | V             |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 5) | 2.2   |     | 5.0  | 2.2  |     | 5.0  | 2.2  |     | 5.0   | V             |
| $I_{IH}$    | Input HIGH Current   |       |     | 255  |      |     | 175  |      |     | 175   | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current  | 0.5   |     |      | 0.5  |     |      | 0.5  |     |       | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

4. Input parameters vary 1:1 with  $V_{CC}$ .  $V_{CC}$  can vary  $\pm 0.25 \text{ V}$ .

5.  $V_{IHCMR}$  min varies 1:1 with  $GND$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ .

**Table 6. TTL OUTPUT DC CHARACTERISTICS**  $V_{CC} = 4.75 \text{ V}$  to  $5.25 \text{ V}$ ;  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$

| Symbol    | Characteristic               | Condition                  | Min  | Typ | Max      | Unit |
|-----------|------------------------------|----------------------------|------|-----|----------|------|
| $V_{OH}$  | Output HIGH Voltage          | $I_{OH} = -3.0 \text{ mA}$ | 2.4  |     | (Note 6) | V    |
| $V_{OL}$  | Output LOW Voltage           | $I_{OL} = 24 \text{ mA}$   |      |     | 0.5      | V    |
| $I_{CCH}$ | Power Supply Current         |                            |      | 20  | 29       | mA   |
| $I_{CCL}$ | Power Supply Current         |                            |      | 22  | 32       | mA   |
| $I_{OS}$  | Output Short Circuit Current |                            | -150 |     | -60      | mA   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

6. Maximum level is  $V_{CC} - 0.7$  by design.

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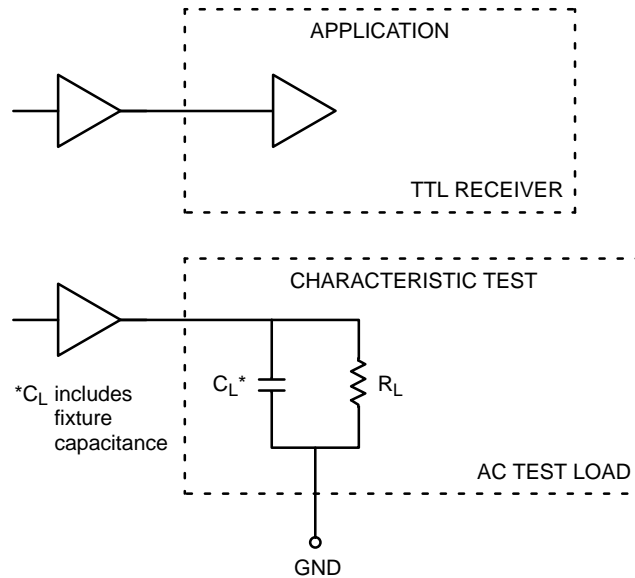
**AC CHARACTERISTICS**  $V_{CC} = 4.75 \text{ V to } 5.25 \text{ V}$ ;  $GND = 0.0 \text{ V}$  (Note 7)

| Symbol              | Characteristic                 | -40°C |     |      | 25°C |     |      | 85°C |     |      | Unit |
|---------------------|--------------------------------|-------|-----|------|------|-----|------|------|-----|------|------|
|                     |                                | Min   | Typ | Max  | Min  | Typ | Max  | Min  | Typ | Max  |      |
| $f_{\max}$          | Maximum Toggle Frequency       |       |     |      |      | 100 |      |      |     |      | MHz  |
| $t_{\text{JITTER}}$ | Random Clock Jitter (RMS)      |       |     |      |      | 35  |      |      |     |      | ps   |
| $t_{\text{PLH}}$    | Propagation Delay @ 1.5 V      | 2.0   |     | 5.5  | 2.0  |     | 5.5  | 2.0  |     | 5.5  | ns   |
| $t_{\text{PHL}}$    | Propagation Delay @ 1.5 V      | 2.0   |     | 5.5  | 2.0  |     | 5.5  | 2.0  |     | 5.5  | ns   |
| $V_{\text{PP}}$     | Input Swing (Note 8)           | 200   |     | 1000 | 200  |     | 1000 | 200  |     | 1000 | mV   |
| $t_r/t_f$           | Output Rise/Fall Time (10–90%) |       |     |      |      | 750 |      |      |     |      | ps   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

7.  $R_L = 500 \Omega$  to GND and  $C_L = 20 \text{ pF}$  to GND. Refer to Figure 2.

8.  $V_{\text{PP}}(\text{min})$  is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of  $\approx 40$ .



**Figure 2. TTL Output Loading Used for Device Evaluation**

# MC10ELT21, MC100ELT21

## ORDERING INFORMATION

| Device          | Package              | Shipping <sup>†</sup> |
|-----------------|----------------------|-----------------------|
| MC10ELT21DG     | SOIC-8<br>(Pb-Free)  | 98 Units / Rail       |
| MC10ELT21DR2G   | SOIC-8<br>(Pb-Free)  | 2500 / Tape & Reel    |
| MC10ELT21DTG    | TSSOP-8<br>(Pb-Free) | 100 Units / Rail      |
| MC10ELT21DTR2G  | TSSOP-8<br>(Pb-Free) | 2500 / Tape & Reel    |
| MC100ELT21DG    | SOIC-8<br>(Pb-Free)  | 98 Units / Rail       |
| MC100ELT21DR2G  | SOIC-8<br>(Pb-Free)  | 2500 / Tape & Reel    |
| MC100ELT21DTG   | TSSOP-8<br>(Pb-Free) | 100 Units / Rail      |
| MC100ELT21DTR2G | TSSOP-8<br>(Pb-Free) | 2500 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

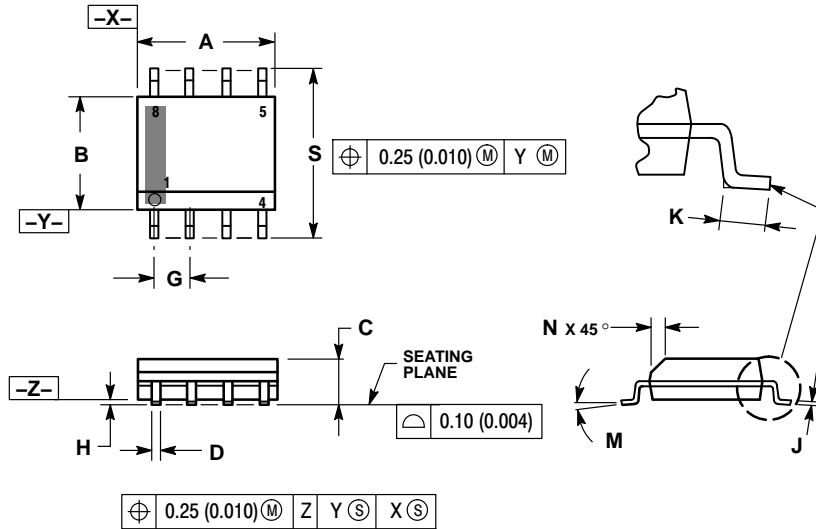
## Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# MC10ELT21, MC100ELT21

## PACKAGE DIMENSIONS

SOIC-8 NB  
CASE 751-07  
ISSUE AK

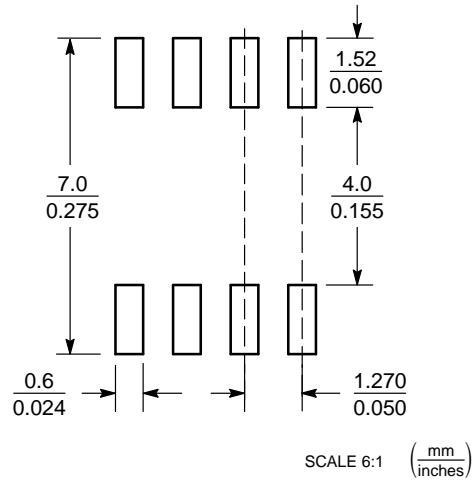


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| E   | 1.27 BSC    |      | 0.050 BSC |       |
| F   | 0.10        | 0.25 | 0.004     | 0.010 |
| G   | 0.19        | 0.25 | 0.007     | 0.010 |
| H   | 0.40        | 1.27 | 0.016     | 0.050 |
| I   | 0°          | 8°   | 0°        | 8°    |
| J   | 0.25        | 0.50 | 0.010     | 0.020 |
| K   | 5.80        | 6.20 | 0.228     | 0.244 |

### SOLDERING FOOTPRINT\*

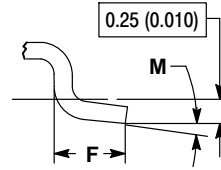
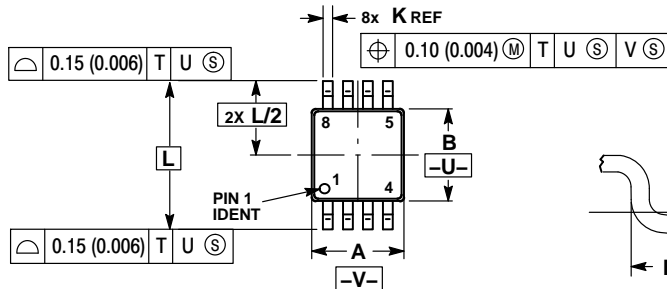


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

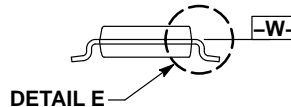
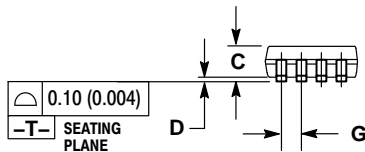
# MC10ELT21, MC100ELT21

## PACKAGE DIMENSIONS

**TSSOP-8**  
**DT SUFFIX**  
**CASE 948R-02**  
**ISSUE A**




**DETAIL E**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 2.90        | 3.10 | 0.114     | 0.122 |
| B   | 2.90        | 3.10 | 0.114     | 0.122 |
| C   | 0.80        | 1.10 | 0.031     | 0.043 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.40        | 0.70 | 0.016     | 0.028 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| K   | 0.25        | 0.40 | 0.010     | 0.016 |
| L   | 4.90 BSC    |      | 0.193 BSC |       |
| M   | 0°          | 6°   | 0°        | 6°    |

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