

MC10H640

68030/040 PECL to TTL Clock Driver

Description

The MC10H640 generates the necessary clocks for the 68030, 68040 and similar microprocessors. It is guaranteed to meet the clock specifications required by the 68030 and 68040 in terms of part-to-part skew, within-part skew and also duty cycle skew.

The user has a choice of using either TTL or PECL (ECL referenced to +5.0 V) for the input clock. TTL clocks are typically used in present MPU systems. However, as clock speeds increase to 50 MHz and beyond, the inherent superiority of ECL (particularly differential ECL) as a means of clock signal distribution becomes increasingly evident. The H640 also uses differential PECL internally to achieve its superior skew characteristic.

The H640 includes divide-by-two and divide-by-four stages, both to achieve the necessary duty cycle skew and to generate MPU clocks as required. A typical 50 MHz processor application would use an input clock running at 100 MHz, thus obtaining output clocks at 50 MHz and 25 MHz (see Logic Diagram).

Features

- Generates Clocks for 68030/040
- Meets 030/040 Skew Requirements
- TTL or PECL Input Clock
- Extra TTL and PECL Power/Ground Pins
- Asynchronous Reset
- Single +5.0 V Supply
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

Function

Reset (R): LOW on RESET forces all Q outputs LOW and all \bar{Q} outputs HIGH.

Power-Up: The device is designed to have the POS edges of the $\div 2$ and $\div 4$ outputs synchronized at power up.

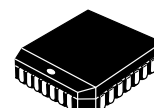
Select (SEL): LOW selects the ECL input source (DE/\bar{DE}). HIGH selects the TTL input source (DT).

The H640 also contains circuitry to force a stable state of the ECL input differential pair, should both sides be left open. In this case, the DE side of the input is pulled LOW, and \bar{DE} goes HIGH.



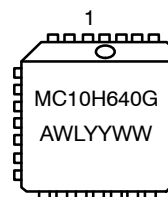
ON Semiconductor®

www.onsemi.com



PLL-28
FN SUFFIX
CASE 776-02

MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*For additional marking information, refer to Application Note [AND8002/D](#).

ORDERING INFORMATION

Device	Package	Shipping
MC10H640FNG	PLL-28 (Pb-Free)	37 Units / Tube

MC10H640

Table 3. 10H PECL DC CHARACTERISTICS ($V_T = V_E = 5.0\text{ V} \pm 5\%$)

Symbol	Characteristic	Condition	0°C		25°C		85°C		Unit
			Min	Max	Min	Max	Min	Max	
I_{INH} I_{INL}	Input HIGH Current Input LOW Current		0.5	255	0.5	175	0.5	175	μA
V_{IH1} V_{IL1}	Input HIGH Voltage Input LOW Voltage	$V_E = 5.0\text{ V}$	3.83 3.05	4.16 3.52	3.87 3.05	4.19 3.52	3.94 3.05	4.28 3.555	V
V_{BB1}	Output Reference Voltage		3.62	3.73	3.65	3.75	3.69	3.81	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. PECL levels are referenced to V_{CC} and will vary 1:1 with the power supply. The values shown are for $V_{CC} = 5.0\text{V}$.
1. PECL levels are referenced to V_{CC} and will vary 1:1 with the power supply. The values shown are for $V_{CC} = 5.0\text{V}$.

Table 4. TTL DC CHARACTERISTICS ($V_T = V_E = 5.0\text{ V} \pm 5\%$)

Symbol	Characteristic	Condition	0°C		25°C		85°C		Unit
			Min	Max	Min	Max	Min	Max	
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage		2.0	0.8	2.0	0.8	2.0	0.8	V
I_{IH}	Input HIGH Current	$V_{IN} = 2.7\text{ V}$ $V_{IN} = 7.0\text{ V}$		20 100		20 100		20 100	μA
I_{IL}	Input LOW Current	$V_{IN} = 0.5\text{ V}$		-0.6		-0.6		-0.6	mA
V_{OH}	Output HIGH Voltage	$I_{OH} = -3.0\text{ mA}$ $I_{OH} = -15\text{ mA}$	2.5 2.0		2.5 2.0		2.5 2.0		V
V_{OL}	Output LOW Voltage	$I_{OL} = 24\text{ mA}$		0.5		0.5		0.5	V
V_{IK}	Input Clamp Voltage	$I_{IN} = -18\text{ mA}$		-1.2		-1.2		-1.2	V
I_{OS}	Output Short Circuit Current	$V_{OUT} = 0\text{ V}$	-100	-225	-100	-225	-100	-225	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

MC10H640

Table 5. AC CHARACTERISTICS ($V_T = V_E = 5.0 \text{ V} \pm 5\%$)

Symbol	Characteristic	Condition	0°C		25°C		85°C		Unit	
			Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay ECL D to Output	Q0 – Q3	CL = 25 pF	4.0	6.0	4.0	6.0	4.2	6.2	ns
t_{PLH}	Propagation Delay TTL D to Output		CL = 25 pF	4.0	6.0	4.0	6.0	4.3	6.3	ns
tskwd*	Within-Device Skew		CL = 25 pF		0.5		0.5		0.5	ns
t_{PLH}	Propagation Delay ECL D to Output	$\overline{Q0}, \overline{Q1}$	CL = 25 pF	4.0	6.0	4.0	6.0	4.2	6.2	ns
t_{PLH}	Propagation Delay TTL D to Output		CL = 25 pF	4.0	6.0	4.0	6.0	4.3	6.3	ns
t_{PLH}	Propagation Delay ECL D to Output	Q4, Q5	CL = 25 pF	4.0	6.0	4.0	6.0	4.2	6.2	ns
t_{PLH}	Propagation Delay TTL D to Output		CL = 25 pF	4.0	6.0	4.0	6.0	4.3	6.3	ns
t_{PD}	Propagation Delay R to Output	All Outputs	CL = 25 pF	4.3	6.3	4.3	6.3	5.0	7.0	ns
t_R t_F	Output Rise/Fall Time 0.8 V to 2.0 V	All Outputs	CL = 25 pF		2.5 2.5		2.5 2.5		2.5 2.5	ns
f_{max}	Maximum Input Frequency		CL = 25 pF	135		135		135		MHz
t_{pw}	Minimum Pulse Width			1.50		1.50		1.50		ns
t_{rr}	Reset Recovery Time			1.25		1.25		1.25		ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Within-Device Skew defined as identical transitions on similar paths through a device.

Table 6. V_{CC} and C_L RANGES TO MEET DUTY CYCLE REQUIREMENTS

($0^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ Output Duty Cycle Measured Relative to 1.5 V)

Symbol	Characteristic	Condition	Min	Nom	Max	Unit
	Range of V_{CC} and C_L to meet minimum pulse width (HIGH or LOW) = 11.5 ns at $f_{out} \leq 40$ MHz	$\overline{Q0} - \overline{Q3}$ $\overline{Q0} - \overline{Q1}$	4.75 10	5.0	5.25 50	V pF
	Range of V_{CC} and C_L to meet minimum pulse width (HIGH or LOW) = 9.5 ns at $40 < f_{out} \leq 50$ MHz	Q0 – Q3	4.875 15	5.0	5.125 27	V pF

MC10H640

10H640 DUTY CYCLE CONTROL

To maintain a duty cycle of $\pm 5\%$ at 50MHz, limit the load capacitance and/or power supply variation as shown in Figures 3 and 4. Figure 5 shows typical TPD versus load. Figure 6 shows reset recovery time. Figure 7 shows output states after power up. Best duty cycle control is obtained with a single μP load and minimum line length.

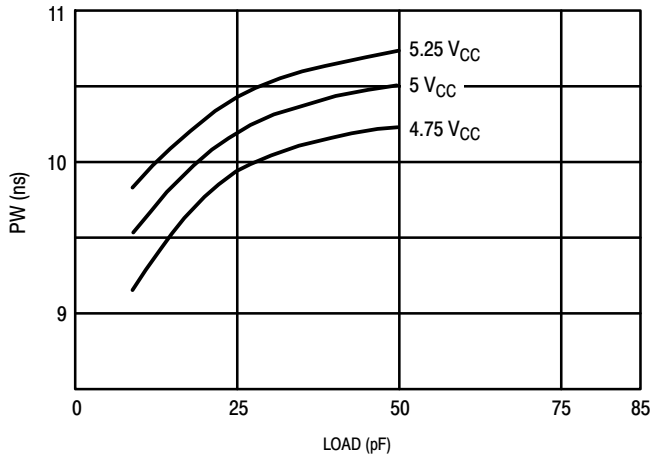


Figure 3. Positive Pulse Width at 25°C Ambient and 50 MHz Out

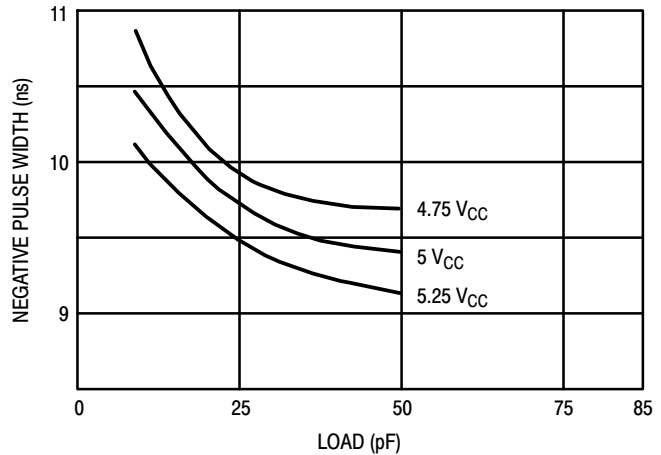


Figure 4. Negative Pulse Width at 25°C Ambient and 50 MHz Out

Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

MC10H640

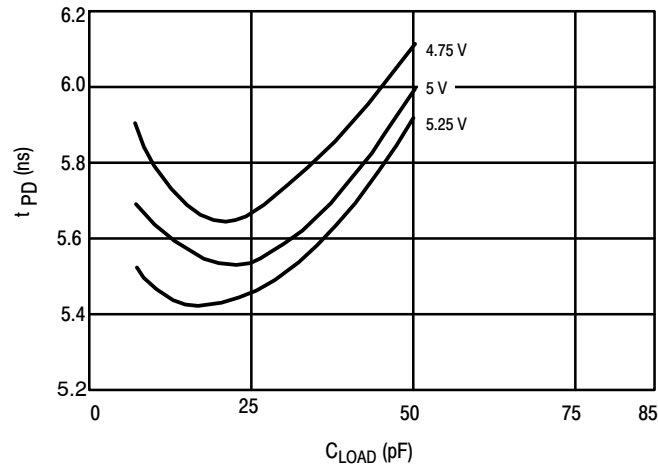


Figure 5. t_{PD} versus Load Typical at $T_A = 25^\circ\text{C}$

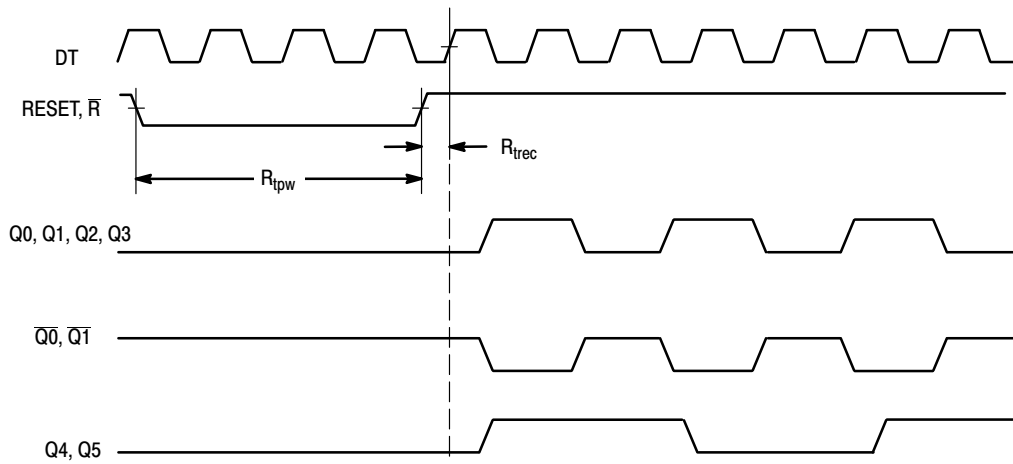
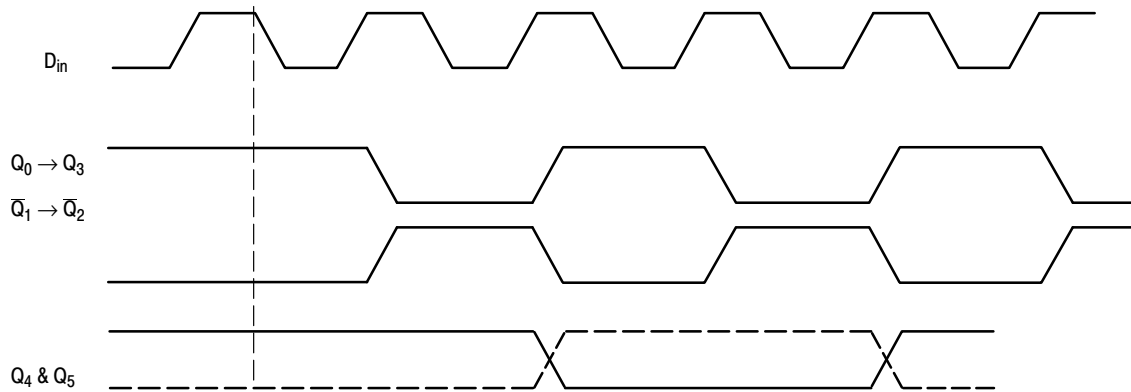


Figure 6. MC10H640 Clock Phase and Reset Recovery Time After Reset Pulse



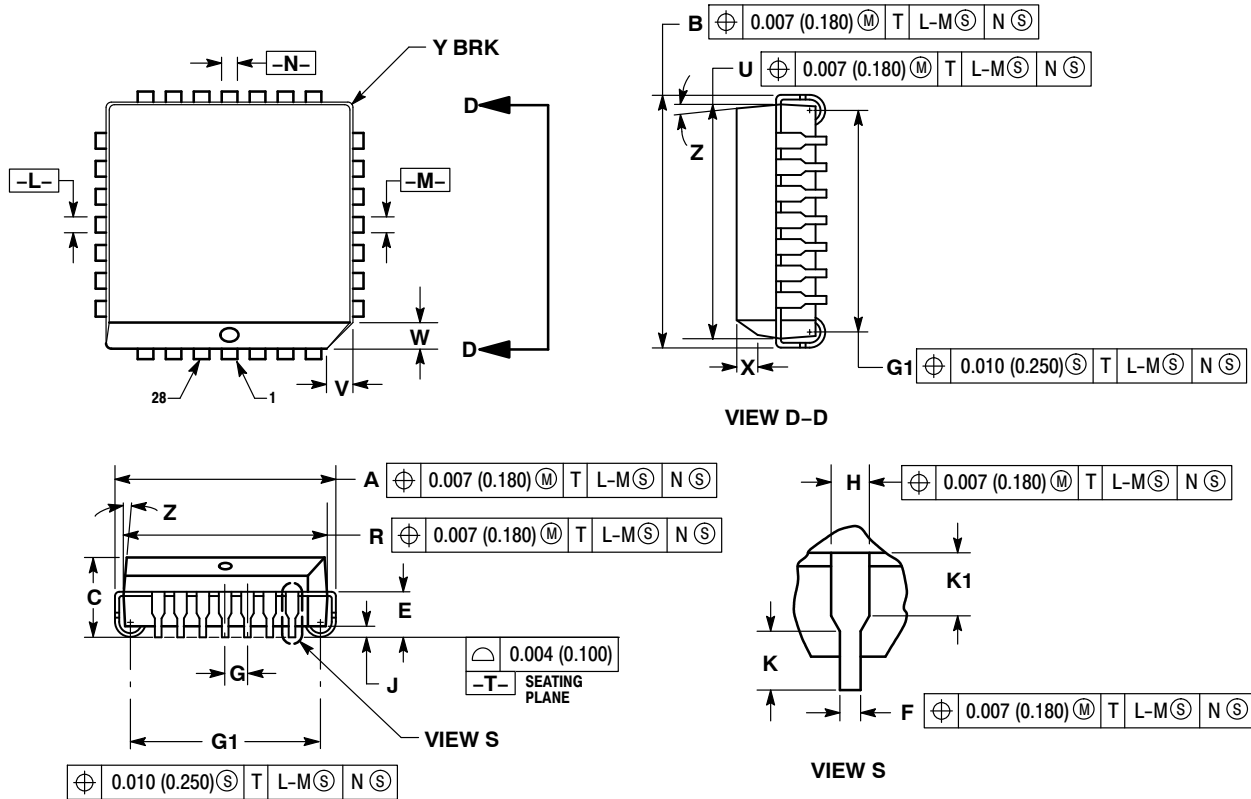
AFTER POWER UP
 OUTPUTS Q_4 & Q_5 WILL SYNC WITH POSITIVE EDGES OF D_{in} & $Q_0 \rightarrow Q_3$ & NEGATIVE EDGES OF \bar{Q}_0 & \bar{Q}_1

Figure 7. Output Timing Diagram

MC10H640

PACKAGE DIMENSIONS

28 LEAD PLLC
FN SUFFIX
CASE 776-02
ISSUE F




NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1. TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

MC10H640

ECLinPS and MECL are trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local
Sales Representative