# **Single 2-Input NOR Gate**

The MC74VHC1G02 is an advanced high speed CMOS 2-input NOR gate fabricated with silicon gate CMOS technology.

The internal circuit is composed of multiple stages, including a buffer output which provides high noise immunity and stable output.

The MC74VHC1G02 input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the MC74VHC1G02 to be used to interface 5 V circuits to 3 V circuits.

#### **Features**

- High Speed:  $t_{PD} = 3 \text{ ns (Typ)}$  at  $V_{CC} = 5 \text{ V}$
- Low Power Dissipation:  $I_{CC} = 1.0 \mu A$  (Max) at  $T_A = 25^{\circ}C$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FETs = 56
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

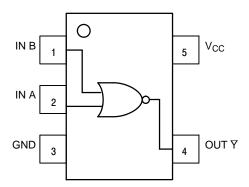


Figure 1. Pinout (Top View)

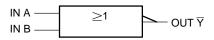


Figure 2. Logic Symbol



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MARKING DIAGRAMS

SC70-5/SC-88A/SOT-353 DF SUFFIX CASE 419A



SOT23-5/TSOP-5/SC59-5 DT SUFFIX CASE 483



V3 = Device Code M = Date Code\* • = Pb-Free Package

(Note: Microdot may be in either location)
\*Date Code orientation and/or position may vary depending upon manufacturing location.

	PIN ASSIGNMENT					
1	IN B					
2	IN A					
3	GND					
4	OUT $\overline{Y}$					
5	V <sub>CC</sub>					

#### **FUNCTION TABLE**

uts	Output
В	Y
L	Н
Н	L
L	L
Н	L
	B L H L

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

#### **MAXIMUM RATINGS**

Symbol	Charact	eristics	Value	Unit
V <sub>CC</sub>	DC Supply Voltage		-0.5 to +7.0	V
V <sub>IN</sub>	DC Input Voltage		-0.5 to +7.0	V
V <sub>OUT</sub>	DC Output Voltage	V <sub>CC</sub> = 0 High or Low State	-0.5 to 7.0 -0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input Diode Current		-20	mA
I <sub>OK</sub>	Output Diode Current	V <sub>OUT</sub> < GND; V <sub>OUT</sub> > V <sub>CC</sub>	+20	mA
I <sub>OUT</sub>	DC Output Current, per Pin		+25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND		+50	mA
P <sub>D</sub>	Power Dissipation in Still Air at 85°C	SC70-5/SC-88A TSOP-5	150 200	mW
$\theta_{JA}$	Thermal Resistance	SC70-5/SC-88A (Note 1) TSOP-5	350 230	°C/W
TL	Lead Temperature, 1 mm from Case for 10	Seconds	260	°C
TJ	Junction Temperature Under Bias		+ 150	°C
T <sub>STG</sub>	Storage Temperature Range		-65 to +150	°C
V <sub>ESD</sub>	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V
I <sub>LATCHUP</sub>	Latchup Performance Ab	ove V <sub>CC</sub> and Below GND at 125°C (Note 5)	±500	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
- 2. Tested to EIA/JESD22-A114-A.
- 3. Tested to EIA/JESD22-A115-A.
- 4. Tested to JESD22-C101-A.
- 5. Tested to EIA/JESD78.

## **RECOMMENDED OPERATING CONDITIONS**

Symbol	Characteristics	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	2.0	5.5	V
V <sub>IN</sub>	DC Input Voltage	0.0	5.5	V
V <sub>OUT</sub>	DC Output Voltage	0.0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature Range	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time $ \begin{array}{c} \rm V_{CC} = 3.3~V~\pm~0.3~V \\ \rm V_{CC} = 5.0~V~\pm~0.5~V \end{array} $	0	100 20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

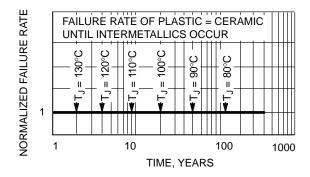


Figure 3. Failure Rate vs. Time Junction Temperature

#### DC ELECTRICAL CHARACTERISTICS

			V <sub>CC</sub>	Т	A = 25°	С	<b>T</b> <sub>A</sub> ≤	85°C	-55 ≤ T <sub>A</sub>	≤ 125°C	
Symbol	Parameter	Test Conditions	(V)	Min	Тур	Max	Min	Max	Min	Max	Unit
V <sub>IH</sub>	Minimum High–Level Input Voltage		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V <sub>IL</sub>	Maximum Low–Level Input Voltage		2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	V
V <sub>OH</sub>	Minimum High-Level Output Voltage V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -50  \mu\text{A}$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		$V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OH} = -4$ mA $I_{OH} = -8$ mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V <sub>OL</sub>	Maximum Low–Level Output Voltage V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 50  \mu\text{A}$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OL} = 4$ mA $I_{OL} = 8$ mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> = 5.5 V or GND	0 to 5.5			± 0.1		±1.0		±1.0	μΑ
Icc	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			1.0		10		40	μΑ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

#### AC ELECTRICAL CHARACTERISTICS Input $t_f = t_f = 3.0 \text{ ns}$

				Т	A = 25°	С	T <sub>A</sub> ≤	85°C	-55 ≤ T <sub>A</sub>	≤ 125°C	
Symbol	Parameter	Test Condit	ions	Min	Тур	Max	Min	Max	Min	Max	Unit
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A or B to Y	$V_{CC} = 3.3 \pm 0.3 \text{ V}$	$C_L = 15 pF$ $C_L = 50 pF$		4.0 5.4	7.9 11.4		9.5 13.0		11.0 15.5	ns
	input A of B to 1	$V_{CC} = 5.0 \pm 0.5 \text{ V}$	$C_L = 15 pF$ $C_L = 50 pF$		3.0 3.8	5.5 7.5		6.5 8.5		8.0 10.0	
C <sub>IN</sub>	Maximum Input Capacitance				5.5	10		10		10	pF

		Typical @ 25°C, V <sub>CC</sub> = 5.0 V	
$C_{PD}$	Power Dissipation Capacitance (Note 6)	11	pF

<sup>6.</sup> C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC} \cdot C_{PD}$  is used to determine the no–load dynamic power consumption;  $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$ .

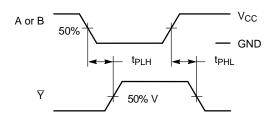
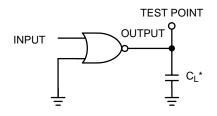


Figure 4. Switching Waveforms



\*Includes all probe and jig capacitance

Figure 5. Test Circuit

#### **ORDERING INFORMATION**

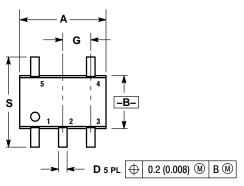
Device	Package	Shipping <sup>†</sup>		
MC74VHC1G02DFT1G				
MC74VHC1G02DFT2G	SC-88A (Pb-Free)	3000/Tape & Reel		
NLVVHC1G02DFT2G*	( 2 )			
MC74VHC1G02DTT1G	TSOP-5 (Pb-Free)	3000/Tape & Reel		

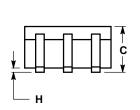
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
\*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP

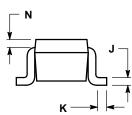
Capable.

#### **PACKAGE DIMENSIONS**

### SC-88A/SOT-353/SC-70 **DF SUFFIX** CASE 419A-02 ISSUE K



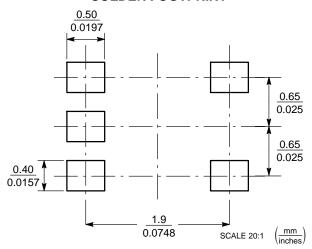




- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
  4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

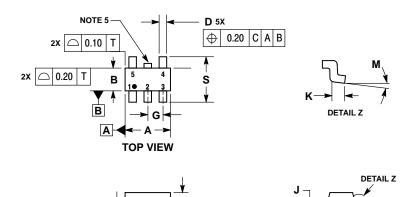
	INC	HES	MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.071	0.087	1.80	2.20	
В	0.045	0.053	1.15	1.35	
C	0.031	0.043	0.80	1.10	
D	0.004	0.012	0.10	0.30	
G	0.026	BSC	0.65 BSC		
Н		0.004		0.10	
J	0.004	0.010	0.10	0.25	
K	0.004	0.012	0.10	0.30	
N	0.008	REF	0.20	REF	
S	0.079	0.087	2.00	2.20	

# **SOLDER FOOTPRINT**



#### PACKAGE DIMENSIONS

#### TSOP-5 DT SUFFIX CASE 483-02 ISSUE L



C SEATING

#### NOTES:

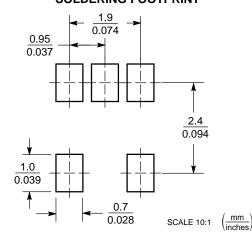
- DIMENSIONING AND TOLERANCING PER ASME
- Y14.5M, 1994. 2. CONTROLLING DIMENSION: MILLIMETERS.
- MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH
  THICKNESS. MINIMUM LEAD THICKNESS IS THE
  MINIMUM IM THICKNESS OF BASE MATERIAL
- MINIMUM THICKNESS OF BASE MATERIAL.

  4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
- OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS					
DIM	MIN MAX					
Α	3.00	BSC				
В	1.50	BSC				
O	0.90	1.10				
D	0.25	0.50				
G	0.95	BSC				
Η	0.01	0.10				
7	0.10	0.26				
K	0.20	0.60				
М	0 °	10°				
S	2.50	3.00				

#### **SOLDERING FOOTPRINT\***

**END VIEW** 



\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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