2-Input OR Gate/CMOS Logic Level Shifter

The MC74VHC1GT32 is an advanced high speed CMOS 2-input OR gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The device input is compatible with TTL-type input thresholds and the output has a full 5 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic-level translator from 3 V CMOS logic to 5 V CMOS Logic or from 1.8 V CMOS logic to 3 V CMOS Logic while operating at the high-voltage power supply.

The MC74VHC1GT32 input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the MC74VHC1GT32 to be used to interface 5 V circuits to 3 V circuits. The output structures also provide protection when $V_{CC} = 0$ V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

Features

- High Speed: $t_{PD} = 3.5 \text{ ns (Typ)}$ at $V_{CC} = 5 \text{ V}$
- Low Power Dissipation: $I_{CC} = 2 \mu A \text{ (Max)}$ at $T_A = 25 \text{°C}$
- TTL-Compatible Inputs: $V_{IL} = 0.8 \text{ V}$; $V_{IH} = 2 \text{ V}$
- CMOS–Compatible Outputs: $V_{OH} > 0.8 V_{CC}$; $V_{OL} < 0.1 V_{CC}$ @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FETs = 65; Equivalent Gates = 15
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

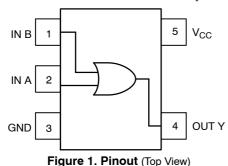




Figure 2. Logic Symbol



ON Semiconductor®

http://onsemi.com

MARKING DIAGRAMS



SC-88A / SC70-5 / SOT-353 DF SUFFIX CASE 419A





TSOP-5 / SOT23-5 / SC59-5 DT SUFFIX CASE 483



VN = Device Code M = Date Code* ■ = Pb-Free Package

(Note: Microdot may be in either location)
*Date Code orientation and/or position may vary
depending upon manufacturing location.

PIN ASSIGNMENT				
1 IN B				
2	IN A			
3	GND			
4	OUT Y			
5	V _{CC}			

FUNCTION TABLE

Inp	uts	Output
Α	В	Υ
L	L	L
L	Н	Н
Н	L	н
Н	Н	н

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MAXIMUM RATINGS

Symbol	Characteristics	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _{IN}	DC Input Voltage	-0.5 to +7.0	V
V _{OUT}	DC Output Voltage V _{CC} = 0 High or Low State	-0.5 to 7.0 -0.5 to V _{CC} + 0.5	V
I _{IK}	Input Diode Current	-20	mA
I _{OK}	Output Diode Current $V_{OUT} < GND; V_{OUT} > V_{CC}$	+20	mA
I _{OUT}	DC Output Current, per Pin	+25	mA
I _{CC}	DC Supply Current, V _{CC} and GND	+50	mA
P_{D}	Power dissipation in still air SC-88A, TSOP-5	200	mW
$\theta_{\sf JA}$	Thermal resistance SC-88A, TSOP-5	333	°C/W
T_L	Lead temperature, 1 mm from case for 10 s	260	°C
TJ	Junction temperature under bias	+150	°C
T _{stg}	Storage temperature	-65 to +150	°C
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	> 2000 > 200 N/A	V
I _{Latchup}	Latchup Performance Above V _{CC} and Below GND at 125°C (Note 4)	±500	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- 1. Tested to EIA/JESD22-A114-A
- 2. Tested to EIA/JESD22-A115-A
- 3. Tested to JESD22-C101-A
- 4. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
V _{CC}	DC Supply Voltage	3.0	5.5	V
V _{IN}	DC Input Voltage	0.0	5.5	V
V _{OUT}	DC Output Voltage $V_{CC} = 0 \\ \text{High or Low State}$	0.0 0.0	5.5 V _{CC}	٧
T _A	Operating Temperature Range	-55	+125	°C
t _r , t _f	Input Rise and Fall Time $ V_{CC} = 3.3 \ V \pm 0.3 \ V \\ V_{CC} = 5.0 \ V \pm 0.5 \ V $	0 0	100 20	ns/V

Device Junction Temperature versus Time to 0.1% Bond Failures

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

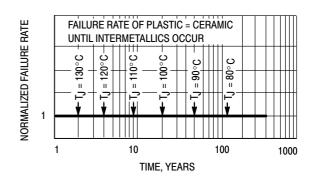


Figure 3. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

			Vcc	Т	A = 25°	С	T _A ≤	85°C	-55 ≤ T _A	≤ 125°C	
Symbol	Parameter	Test Conditions	(V)	Min	Тур	Max	Min	Max	Min	Max	Unit
V _{IH}	Minimum High-Level Input Voltage		3.0 4.5 5.5	1.4 2.0 2.0			1.4 2.0 2.0		1.4 2.0 2.0		V
V _{IL}	Maximum Low-Level Input Voltage		3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
V _{OH}	Minimum High-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50 \mu A$	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
	$V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4$ mA $I_{OH} = -8$ mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V _{OL}	Maximum Low-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50 \mu A$	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
	$V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 4$ mA $I_{OL} = 8$ mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I _{IN}	Maximum Input Leakage Current	V _{IN} = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	μА
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			2.0		20		40	μΑ
I _{CCT}	Quiescent Supply Current	Input: V _{IN} = 3.4 V	5.5			1.35		1.50		1.65	mA
I _{OPD}	Output Leakage Current	V _{OUT} = 5.5 V	0.0			0.5		5.0		10	μΑ

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input t_r = t_f = 3.0ns)

				Т	A = 25°	С	T _A ≤	85°C	-55 ≤ T _A	≤ 125°C	
Symbol	Parameter	Test Condi	tions	Min	Тур	Max	Min	Max	Min	Max	Unit
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A or B to Y	$V_{CC} = 3.3 \pm 0.3 \text{ V}$	C _L = 15 pF C _L = 50 pF		4.8 6.1	7.9 11.4		9.5 13.0		11.5 15.5	ns
	Input A or B to Y	$V_{CC} = 5.0 \pm 0.5 \text{ V}$	$C_L = 15 pF$ $C_L = 50 pF$		3.7 4.4	5.5 7.5		6.5 8.5		8.0 10.0	
C _{IN}	Maximum Input Capacitance				5.5	10		10		10	pF

		Typical @ 25°C, V _{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 5)	11	pF

^{5.} C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC} \cdot C_{PD}$ is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

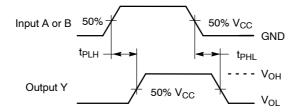
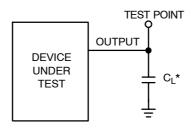


Figure 4. Switching Waveforms



*Includes all probe and jig capacitance

Figure 5. Test Circuit

ORDERING INFORMATION

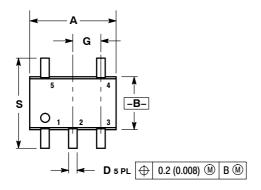
Device	Package	Shipping [†]
M74VHC1GT32DFT1G		
NLVVHC1GT32DFT1G*	SC-88A / SOT-353 / SC-70-5	0000 /T
M74VHC1GT32DFT2G	(Pb-Free)	3000 / Tape & Reel
NLVVHC1GT32DFT2G*		
M74VHC1GT32DTT1G	TSOP-5 / SOT-23 / SC-59 (Pb-Free)	3000 / Tape & Reel

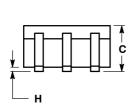
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

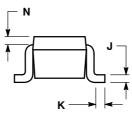
^{*}NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

PACKAGE DIMENSIONS

SC-88A (SC-70-5/SOT-353) CASE 419A-02 ISSUE K





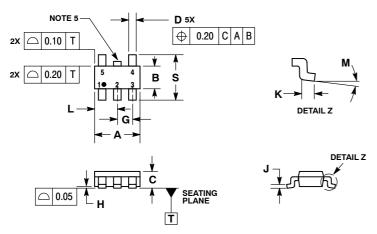


- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
 4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INC	HES	MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.071	0.087	1.80	2.20	
В	0.045	0.053	1.15	1.35	
С	0.031	0.043	0.80	1.10	
D	0.004	0.012	0.10	0.30	
G	0.026	BSC	0.65	BSC	
Н		0.004		0.10	
J	0.004	0.010	0.10	0.25	
K	0.004	0.012	0.10	0.30	
N	0.008	REF	0.20 REF		
S	0.079	0.087	2.00	2.20	

PACKAGE DIMENSIONS

TSOP-5 CASE 483-02 ISSUE H

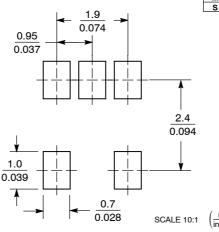


NOTES

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: MILLIMETERS.
- CONTROLLING DIMENSION: MILLIMETERS
 MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD
- LEAD FINISH THICKNESS INCLUDES
 THICKNESS IS THE MINIMUM THICKNESS
 OF BASE MATERIAL.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURBS
- 5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS					
DIM	MIN MAX					
Α	3.00	BSC				
В	1.50	BSC				
С	0.90	1.10				
D	0.25	0.50				
G	0.95	BSC				
Н	0.01	0.10				
J	0.10	0.26				
K	0.20	0.60				
L	1.25	1.55				
М	0 °	10°				
S	2.50	3.00				

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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