NCS2551

500 MHz Voltage Feedback Op Amp

NCS2551 is a 500 MHz voltage feedback monolithic operational amplifier featuring high slew rate and low differential gain and phase error. The voltage feedback architecture allows for a superior bandwidth and low power consumption.

Features

- −3.0 dB Small Signal BW (A_V = +2.0, V_O = 0.5 V_{p-p}) 500 MHz Typ
- Slew Rate 1400 V/μs
- Supply Current 5.5 mA
- Input Referred Voltage Noise 6.0 nV/$\sqrt{Hz}$
- THD −62 dBc (f = 5.0 MHz, V_O = 2.0 V_{p-p})
- Output Current 100 mA
- Pin Compatible with AD8055, TSH341
- This is a Pb−Free Device

Applications

- Line Drivers
- Radar/Communication Receivers

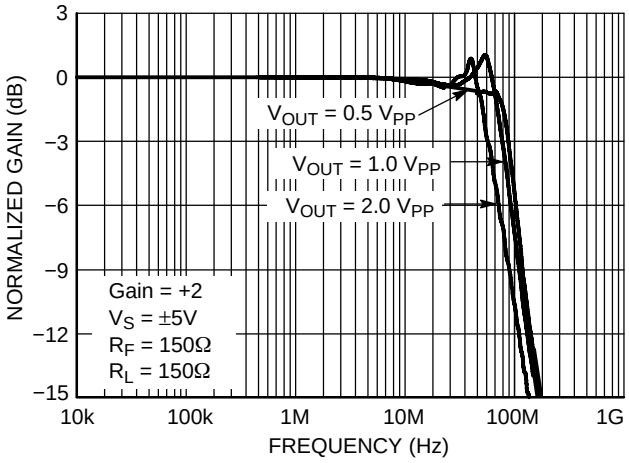
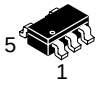


Figure 1. Frequency Response: Gain (dB) vs. Frequency Av = +2.0

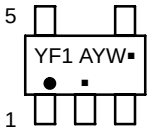
ON Semiconductor®

http://onsemi.com



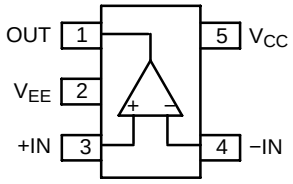
SOT23−5
(TSOP−5)
SN SUFFIX
CASE 483

MARKING DIAGRAM



YF1 = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

SOT23−5 PINOUT

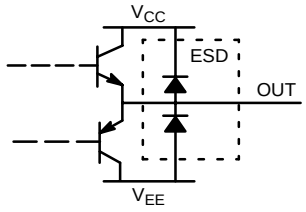
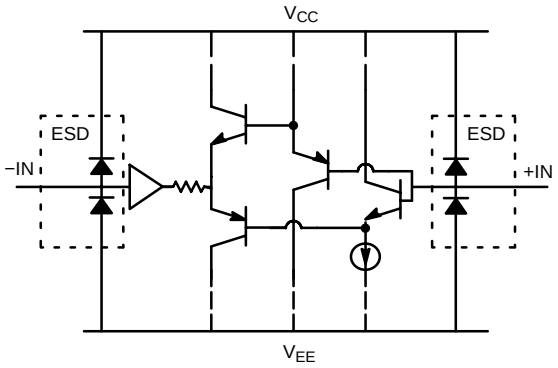


(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

PIN FUNCTION DESCRIPTION

Pin (SOT23−5/SC70)	Symbol	Function	Equivalent Circuit
1	OUT	Output	
2	V_{EE}	Negative Power Supply	
3	+IN	Non−inverted Input	
4	−IN	Inverted Input	See Above
5	V_{CC}	Positive Power Supply	

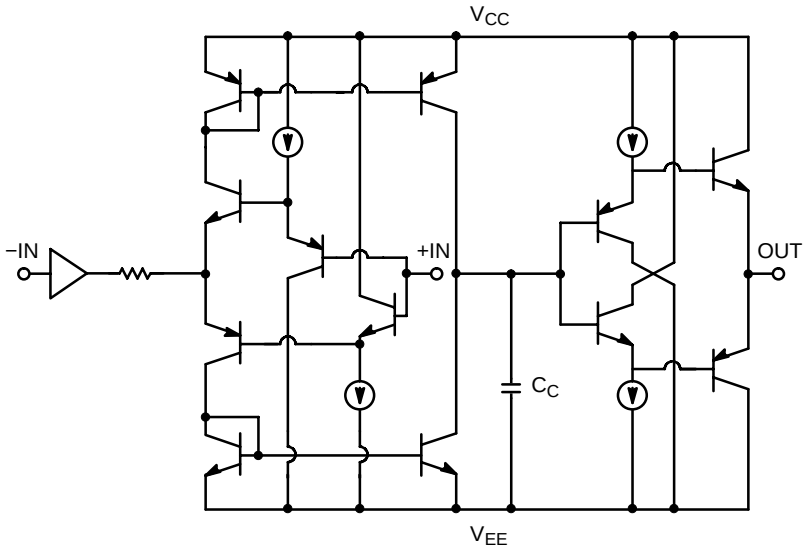


Figure 2. Simplified Device Schematic

ATTRIBUTES

Characteristics	Value
ESD Human Body Model Machine Model Charged Device Model	 2.0 kV 200 V 1.0 kV
Moisture Sensitivity (Note 1)	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in

1. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_S	11	Vdc
Input Voltage Range	V_I	$\leq V_S$	Vdc
Input Differential Voltage Range	V_{ID}	$\leq V_S$	Vdc
Output Current	I_O	100	mA
Maximum Junction Temperature (Note 2)	T_J	150	°C
Operating Ambient Temperature	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−60 to +150	°C
Power Dissipation	P_D	(See Graph)	mW
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	158	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated is limited by the associated rise in junction temperature. For the plastic packages, the maximum safe junction temperature is 150°C. If the maximum is exceeded momentarily, proper circuit operation will be restored as soon as the die temperature is reduced. Leaving the device in the “overheated’’ condition for an extended period can result in device damage.

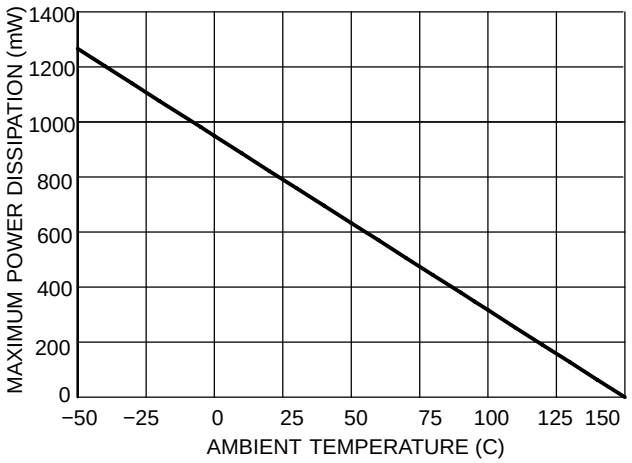


Figure 3. Power Dissipation vs. Temperature

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = −5.0 V, T_A = −40°C to +85°C, R_L = 150 Ω to GND, R_F = 150 Ω, A_V = +2.0, Enable is left open, unless otherwise specified).

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
FREQUENCY DOMAIN PERFORMANCE						
BW	Bandwidth 3.0 dB Small Signal 3.0 dB Large Signal	 A_V = +2.0, V_O = 0.5 V_{p-p} A_V = +2.0, V_O = 2.0 V_{p-p}		 500 300		MHz
$GF_{0.1dB}$	0.1 dB Gain Flatness Bandwidth	A_V = +2.0		15		MHz
dG	Differential Gain	A_V = +2.0, R_L = 150 Ω, f = 3.58 MHz		0.06		%
dP	Differential Phase	A_V = +2.0, R_L = 150 Ω, f = 3.58 MHz		0.06		°
TIME DOMAIN RESPONSE						
SR	Slew Rate	A_V = +2.0, V_{step} = 2.0 V		1400		V/μs
t_s	Settling Time 0.1%	 A_V = +2.0, V_{step} = 2.0 V		 10		ns
t_r t_f	Rise and Fall Time	(10%−90%) A_V = +2.0, V_{step} = 2.0 V		2.4		ns
HARMONIC/NOISE PERFORMANCE						
THD	Total Harmonic Distortion	f = 5.0 MHz, V_O = 2.0 V_{p-p}		−62		dB
HD2	2nd Harmonic Distortion	f = 5.0 MHz, V_O = 2.0 V_{p-p}		−68		dBc
HD3	3rd Harmonic Distortion	f = 5.0 MHz, V_O = 2.0 V_{p-p}		−63		dBc
IP3	Third−Order Intercept	f = 10 MHz, V_O = 1.0 V_{p-p}		40		dBm
SFDR	Spurious−Free Dynamic Range	f = 5.0 MHz, V_O = 2.0 V_{p-p}		63		dBc
e_N	Input Referred Voltage Noise	f = 1.0 MHz		6.0		$nV/\sqrt{Hz}$
i_N	Input Referred Current Noise	f = 1.0 MHz		3.0		$pA/\sqrt{Hz}$

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = −5.0 V, T_A = −40°C to +85°C, R_L = 150 Ω to GND, R_F = 150 Ω, A_V = +2.0, Enable is left open, unless otherwise specified).

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
DC PERFORMANCE						
V_{IO}	Input Offset Voltage		−10	0	+10	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Coefficient			6.0		μV/°C
I_{IB}	Input Bias Current	V_O = 0 V		±3.2	±20	μA
$\Delta I_{IB}/\Delta T$	Input Bias Current Temperature Coefficient	V_O = 0 V		±40		nA/°C
INPUT CHARACTERISTICS						
V_{CM}	Input Common Mode Voltage Range (Note 3)		±3.0	±4.0		V
CMRR	Common Mode Rejection Ratio	(See Graph)	40	50		dB
R_{IN}	Input Resistance			4.5		MΩ
C_{IN}	Differential Input Capacitance			1.0		pF
OUTPUT CHARACTERISTICS						
R_{OUT}	Output Resistance	Closed Loop Open Loop		0.1 17		Ω
V_O	Output Voltage Range		±3.0	±4.0		V
I_O	Output Current		±50	±100		mA
POWER SUPPLY						
V_S	Operating Voltage Supply			10		V
I_S	Power Supply Current		2.0	5.5	10	mA
PSRR	Power Supply Rejection Ratio	(See Graph)	40	60		dB

3. Guaranteed by design and/or characterization.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +2.5 V, V_{EE} = −2.5 V, T_A = −40°C to +85°C, R_L = 150 Ω to GND, R_F = 150 Ω, A_V = +2.0, Enable is left open, unless otherwise specified).

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
FREQUENCY DOMAIN PERFORMANCE						
BW	Bandwidth 3.0 dB Small Signal 3.0 dB Large Signal	 A_V = +2.0, V_O = 0.5 V_{p-p} A_V = +2.0, V_O = 1.0 V_{p-p}		 400 200		MHz
$GF_{0.1dB}$	0.1 dB Gain Flatness Bandwidth	A_V = +2.0		10		MHz
dG	Differential Gain	A_V = +2.0, R_L = 150 Ω, f = 3.58 MHz		0.07		%
dP	Differential Phase	A_V = +2.0, R_L = 150 Ω, f = 3.58 MHz		0.06		°
TIME DOMAIN RESPONSE						
SR	Slew Rate	A_V = +2.0, V_{step} = 1.0 V		800		V/μs
t_s	Settling Time 0.1%	 A_V = +2.0, V_{step} = 1.0 V		 10		ns
t_r t_f	Rise and Fall Time	(10%−90%) A_V = +2.0, V_{step} = 1.0 V		2.2		ns
HARMONIC/NOISE PERFORMANCE						
THD	Total Harmonic Distortion	f = 5.0 MHz, V_O = 1.0 V_{p-p}		−59		dB
HD2	2nd Harmonic Distortion	f = 5.0 MHz, V_O = 1.0 V_{p-p}		−60		dBc
HD3	3rd Harmonic Distortion	f = 5.0 MHz, V_O = 1.0 V_{p-p}		−67		dBc
IP3	Third−Order Intercept	f = 10 MHz, V_O = 0.5 V_{p-p}		35		dBm
SFDR	Spurious−Free Dynamic Range	f = 5.0 MHz, V_O = 1.0 V_{p-p}		60		dBc
e_N	Input Referred Voltage Noise	f = 1.0 MHz		6.0		$nV/\sqrt{Hz}$
i_N	Input Referred Current Noise	f = 1.0 MHz		3.0		$pA/\sqrt{Hz}$

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +2.5 V, V_{EE} = −2.5 V, T_A = −40°C to +85°C, R_L = 150 Ω to GND, R_F = 150 Ω, A_V = +2.0, Enable is left open, unless otherwise specified).

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
DC PERFORMANCE						
V_{IO}	Input Offset Voltage		−10	0	+10	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Coefficient			6.0		μV/°C
I_{IB}	Input Bias Current	V_O = 0 V		±3.2	±20	μA
$\Delta I_{IB}/\Delta T$	Input Bias Current Temperature Coefficient	V_O = 0 V		±40		nA/°C
INPUT CHARACTERISTICS						
V_{CM}	Input Common Mode Voltage Range (Note 3)		±0.9	±1.5		V
CMRR	Common Mode Rejection Ratio	(See Graph)	40	50		dB
R_{IN}	Input Resistance			4.5		MΩ
C_{IN}	Differential Input Capacitance			1.0		pF
OUTPUT CHARACTERISTICS						
R_{OUT}	Output Resistance	Closed Loop Open Loop		0.1 17		Ω
V_O	Output Voltage Range		±0.9	±1.5		V
I_O	Output Current		±50	±100		mA
POWER SUPPLY						
V_S	Operating Voltage Supply			5.0		V
I_S	Power Supply Current		2.0	5.2	10	mA
PSRR	Power Supply Rejection Ratio	(See Graph)	40	60		dB

4. Guaranteed by design and/or characterization.

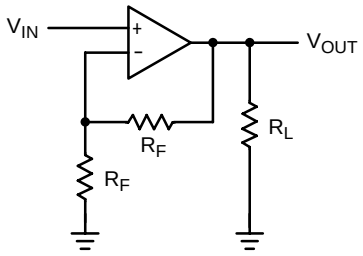


Figure 4. Typical Test Setup
(A_V = +2.0, R_F = 150 kΩ, R_L = 150 Ω)

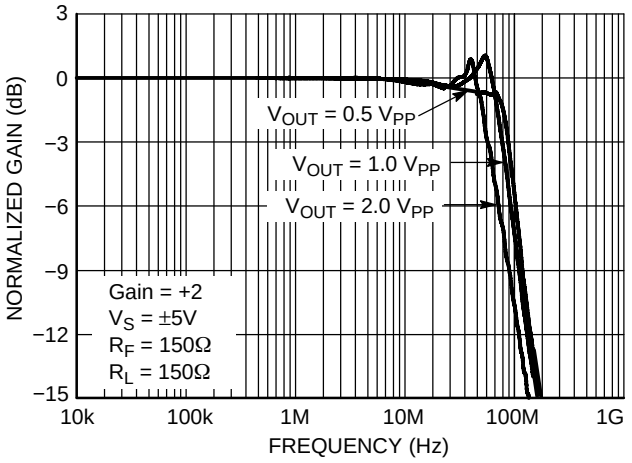


Figure 5. Frequency Response:
Gain (dB) vs. Frequency
Av = +2.0

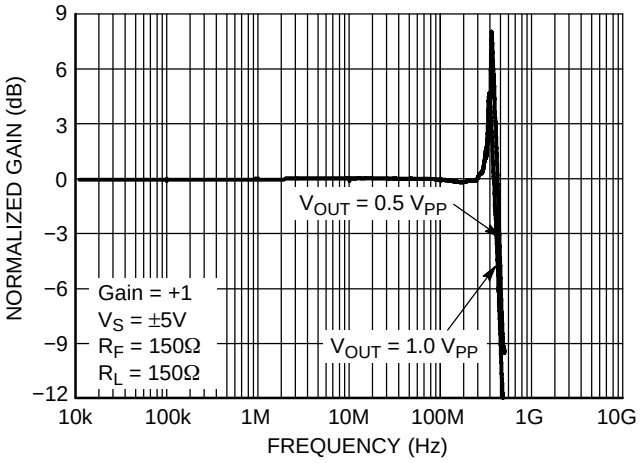


Figure 6. Frequency Response:
Gain (dB) vs. Frequency
Av = +1.0

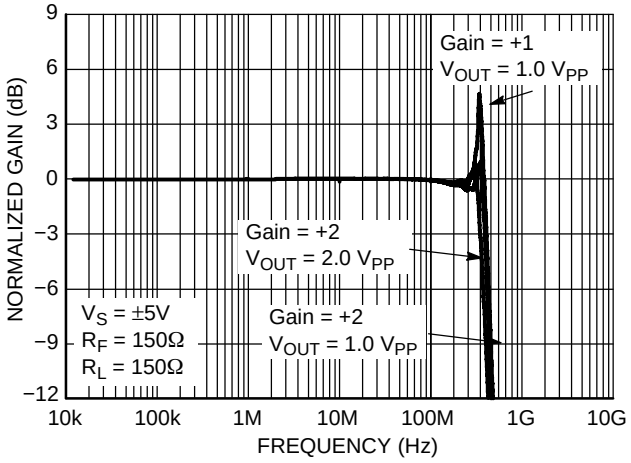


Figure 7. Large Signal Frequency Response
Gain (dB) vs. Frequency

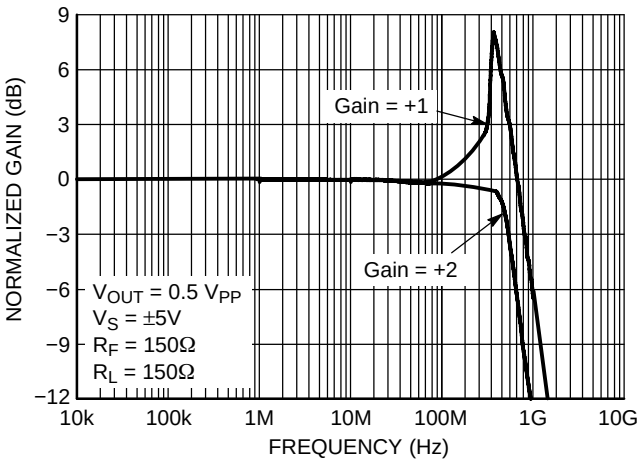


Figure 8. Small Signal Frequency Response
Gain (dB) vs. Frequency

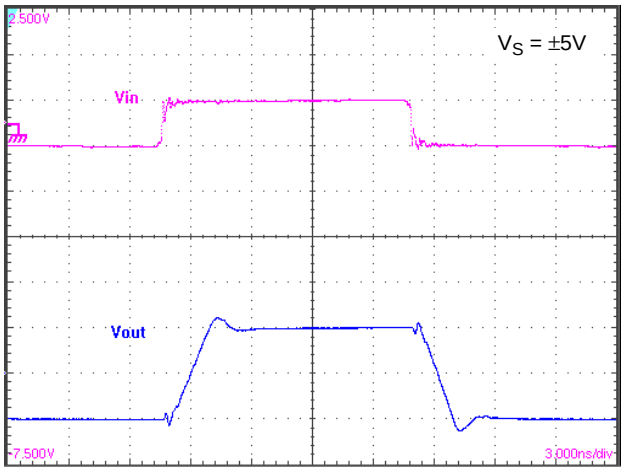


Figure 9. Small Signal Step Response
Vertical: 500 mV/div
Horizontal: 10 ns/div

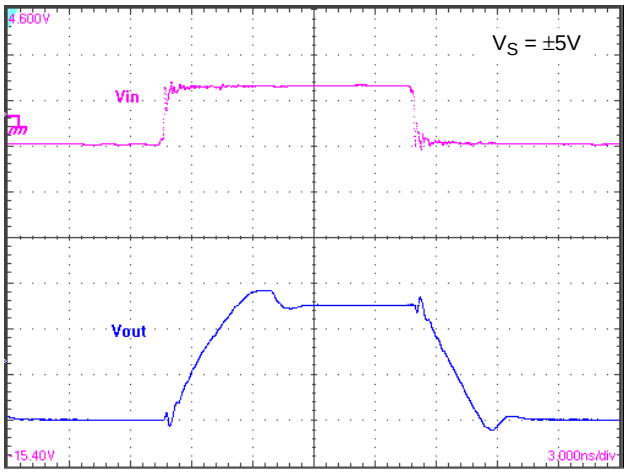


Figure 10. Large Signal Step Response
Vertical: 2V/div
Horizontal: 10 ns/div

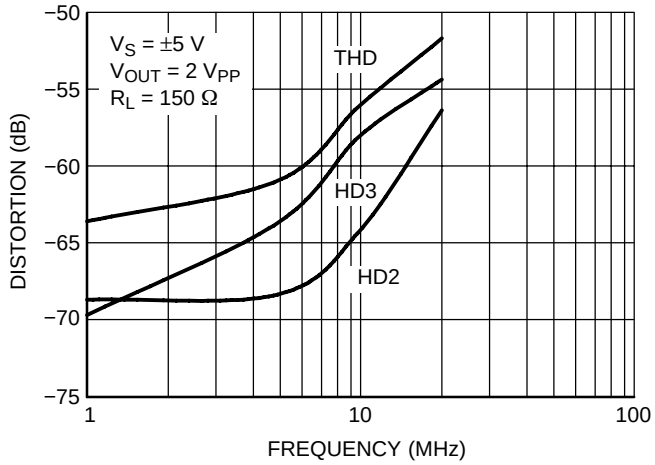


Figure 11. THD, HD2, HD3 vs. Frequency

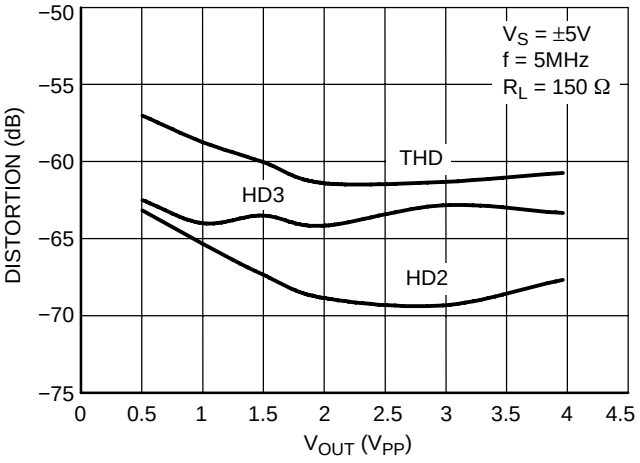


Figure 12. THD, HD2, HD3 vs. Output Voltage

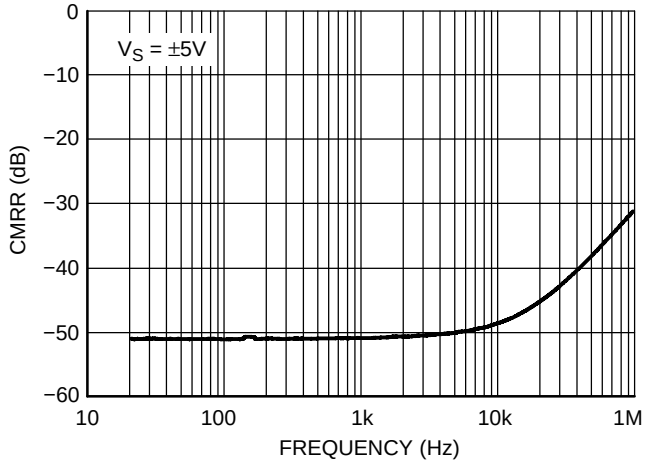


Figure 13. CMRR vs. Frequency

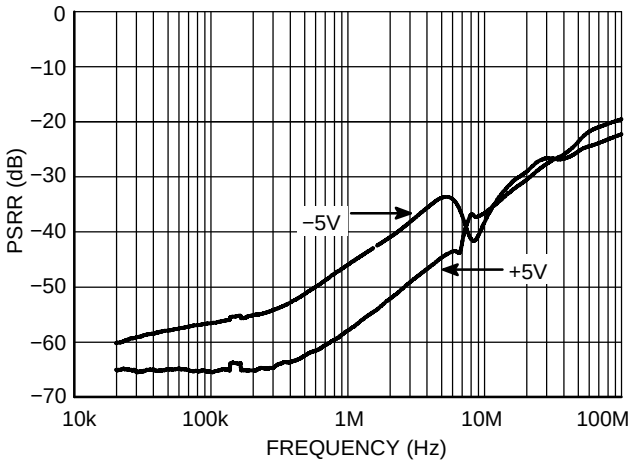


Figure 14. PSRR vs. Frequency

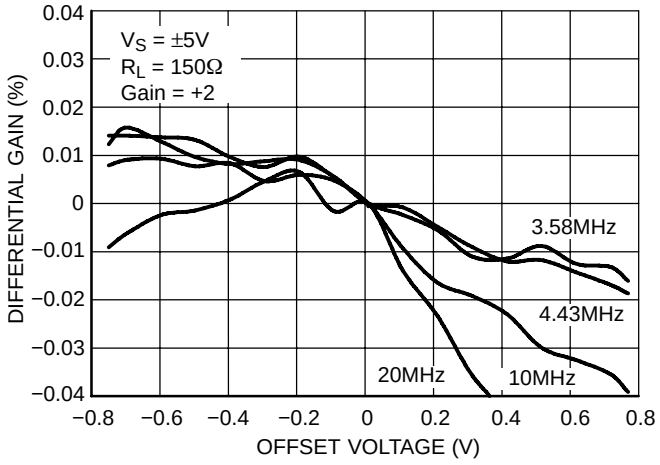


Figure 15. Differential Gain

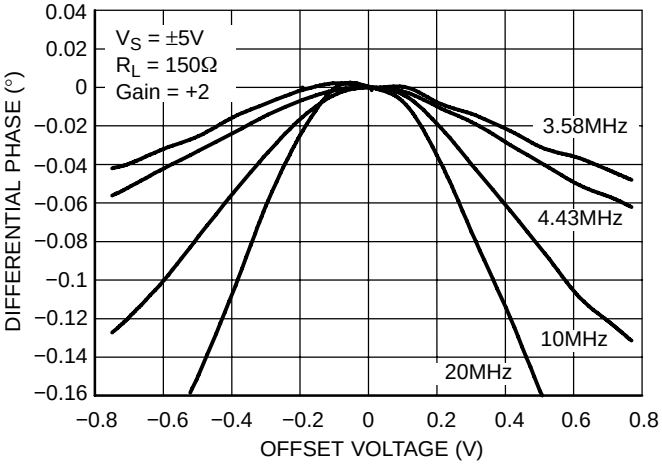


Figure 16. Differential Phase

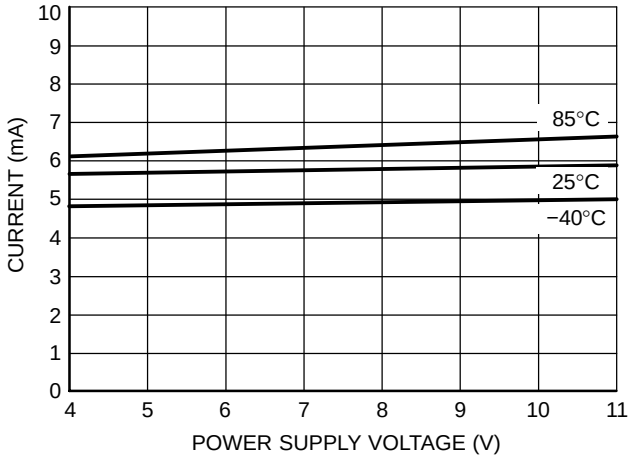


Figure 17. Supply Current vs. Power Supply

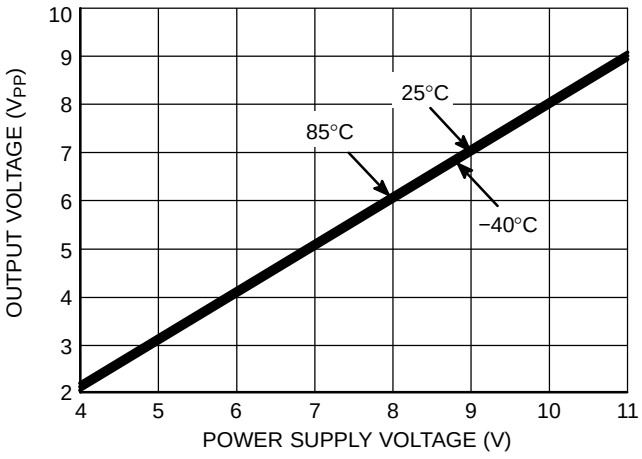


Figure 18. Output Voltage Swing vs. Supply Voltage

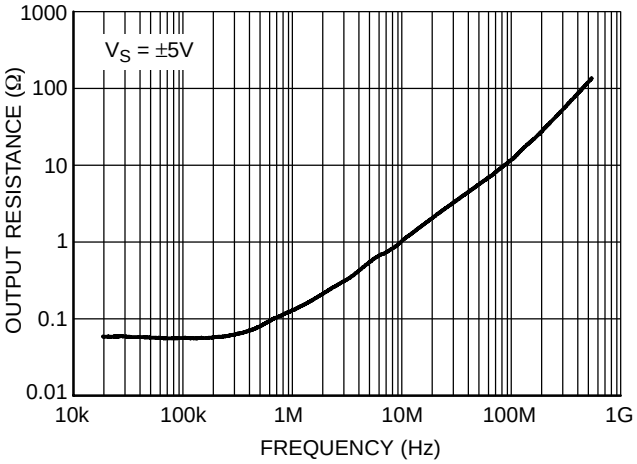


Figure 19. Closed Loop Output Resistance vs. Frequency

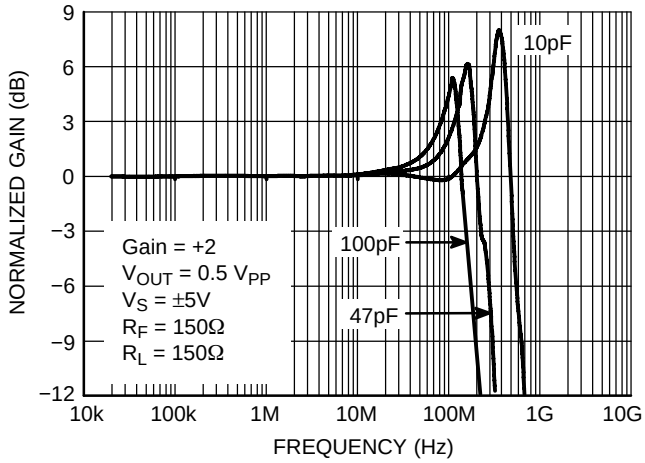


Figure 20. Frequency Response vs. Capacitive Load

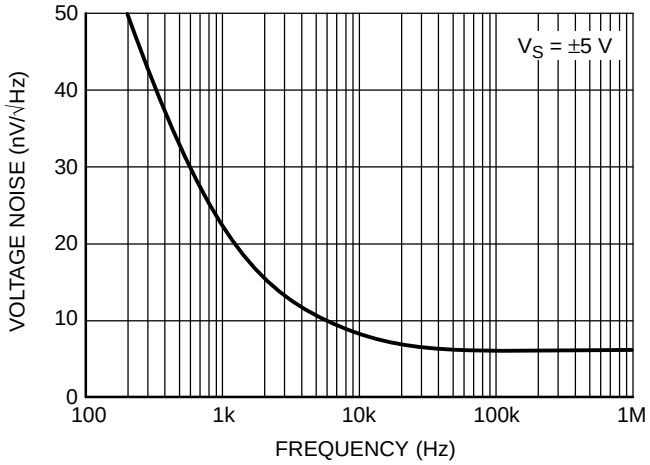


Figure 21. Input Referred Voltage Noise vs. Frequency

Printed Circuit Board Layout Techniques

Proper high speed PCB design rules should be used for all wideband amplifiers as the PCB parasitics can affect the overall performance. Most important are stray capacitances at the output and inverting input nodes as it can effect peaking and bandwidth. A space (3/16″ is plenty) should be left around the signal lines to minimize coupling. Also, signal lines connecting the feedback and gain resistors should be short enough so that their associated inductance does not cause high frequency gain errors. Line lengths less than 1/4″ are recommended.

Video Performance

This device designed to provide good performance with NTSC, PAL, and HDTV video signals. Best performance is obtained with back terminated loads as performance is degraded as the load is increased. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage.

ESD Protection

All device pins have limited ESD protection using internal diodes to power supplies as specified in the attributes table (see Figure 22). These diodes provide moderate protection to input overdrive voltages above the supplies. The ESD diodes can support high input currents with current limiting series resistors. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response. Under closed−loop operation, the ESD diodes have no effect on circuit performance. However, under certain conditions the ESD diodes will be evident. If the device is driven into a slewing condition, the ESD diodes will clamp large differential voltages until the feedback loop restores closed−loop operation. Also, if the device is powered down and a large input signal is applied, the ESD diodes will conduct.

NOTE: Human Body Model for +IN and –IN pins are rated at 0.8kV while all other pins are rated at 2.0kV.

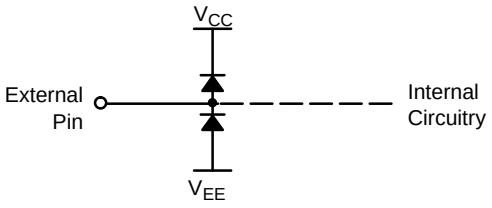


Figure 22. Internal ESD Protection

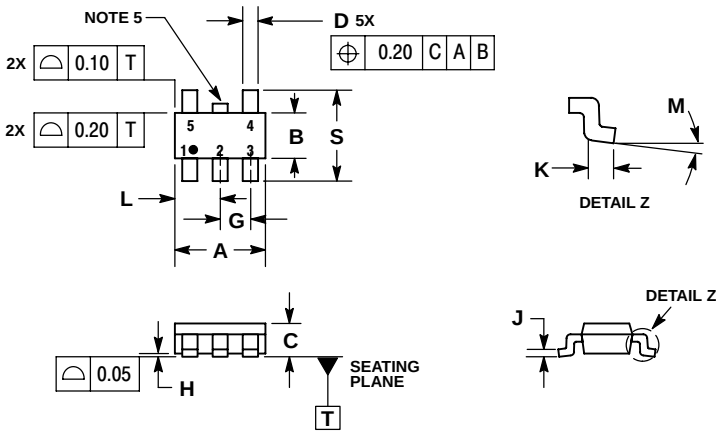
ORDERING INFORMATION

Device	Package	Shipping†
NCS2551SNT1G	SOT23−5 (TSOP−5) (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

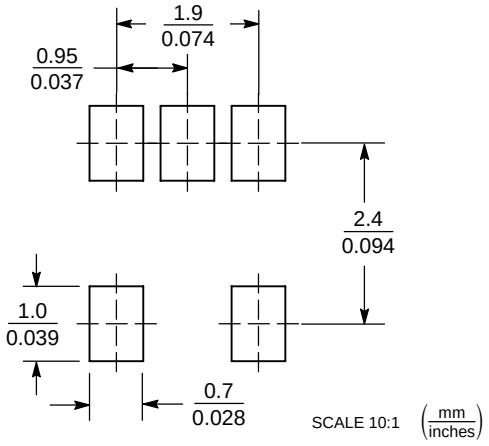
TSOP−5
CASE 483−02
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	3.00 BSC	
B	1.50 BSC	
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
L	1.25	1.55
M	0 °	10 °
S	2.50	3.00

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

NCS2551/D