

NDBA100N10B

Power MOSFET 100V, 6.9mΩ, 100A, N-Channel



ON Semiconductor®

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Features

- Low On-Resistance
- Low Gate Charge
- High Speed Switching
- 100% Avalanche Tested
- Pb-Free, Halogen Free and RoHS Compliance

Specifications

Absolute Maximum Ratings at $T_a = 25^{\circ}\text{C}$

Parameter	Symbol	Value	Unit
Drain to Source Voltage	V_{DS}	100	V
Gate to Source Voltage	V_{GS}	± 20	V
Drain Current (DC)	I_D	100	A
Drain Current (Pulse) $PW \leq 10\mu\text{s}$, duty cycle $\leq 1\%$	I_{DP}	400	A
Power Dissipation $T_c = 25^{\circ}\text{C}$	P_D	110	W
Junction Temperature	T_J	175	$^{\circ}\text{C}$
Storage Temperature	T_{stg}	-55 to $+175$	$^{\circ}\text{C}$
Source Current (Body Diode)	I_S	100	A
Avalanche Energy (Single Pulse) *1	E_{AS}	147	mJ
Lead Temperature for Soldering Purposes, 3mm from Case for 10 Seconds	T_L	260	$^{\circ}\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Value	Unit
Junction to Case Steady State	$R_{\theta JC}$	1.36	$^{\circ}\text{C/W}$
Junction to Ambient *2	$R_{\theta JA}$	62.5	

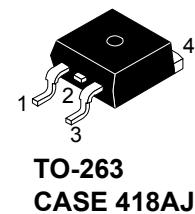
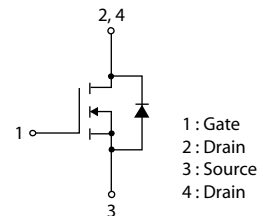
Note : *1 $V_{DD} = 48\text{V}$, $L = 100\mu\text{H}$, $I_{AV} = 40\text{A}$ (Fig.1)

*2 Surface mounted on FR4 board using recommended footprint

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

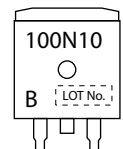
V_{DS}	$R_{DS(on)}$ Max	I_D Max
100V	6.9 mΩ@15V	100A
	8.2 mΩ@10V	

Electrical Connection N-Channel

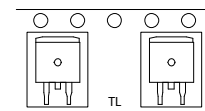


TO-263
CASE 418AJ

Marking



Packing Type : TL



ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

NDBA100N10B

Electrical Characteristics at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D=10\text{mA}$, $V_{GS}=0\text{V}$	100			V
Zero-Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100\text{V}$, $V_{GS}=0\text{V}$			10	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0\text{V}$			± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=10\text{V}$, $I_D=1\text{mA}$	2		4	V
Forward Transconductance	g_{FS}	$V_{DS}=10\text{V}$, $I_D=50\text{A}$		75		S
Static Drain to Source On-State Resistance	$R_{DS(on)1}$	$I_D=50\text{A}$, $V_{GS}=15\text{V}$		5.7	6.9	$\text{m}\Omega$
	$R_{DS(on)2}$	$I_D=50\text{A}$, $V_{GS}=10\text{V}$		6.3	8.2	$\text{m}\Omega$
Input Capacitance	C_{iss}	$V_{DS}=50\text{V}$, $f=1\text{MHz}$		2,950		pF
Output Capacitance	C_{oss}			1,250		pF
Reverse Transfer Capacitance	C_{rss}			20		pF
Turn-ON Delay Time	$t_d(on)$	See Fig.2		40		ns
Rise Time	t_r			385		ns
Turn-OFF Delay Time	$t_d(off)$			68		ns
Fall Time	t_f			52		ns
Total Gate Charge	Q_g	$V_{DS}=48\text{V}$, $V_{GS}=10\text{V}$, $I_D=100\text{A}$		35		nC
Gate to Source Charge	Q_{gs}			13		nC
Gate to Drain "Miller" Charge	Q_{gd}			10		nC
Forward Diode Voltage	V_{SD}	$I_S=100\text{A}$, $V_{GS}=0\text{V}$		1.1	1.5	V
Reverse Recovery Time	t_{rr}	See Fig.3		130		ns
Reverse Recovery Charge	Q_{rr}	$I_S=100\text{A}$, $V_{GS}=0\text{V}$, $V_{DD}=50\text{V}$, $di/dt=100\text{A}/\mu\text{s}$		400		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Fig.1 Unclamped Inductive Switching Test Circuit

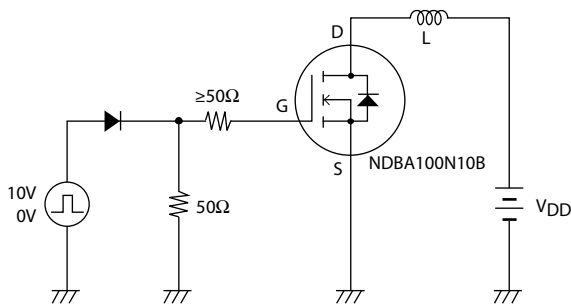


Fig.2 Switching Time Test Circuit

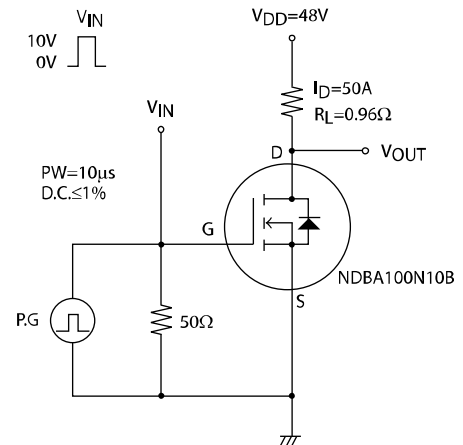
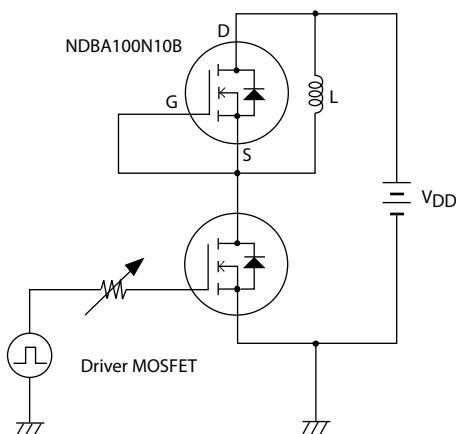
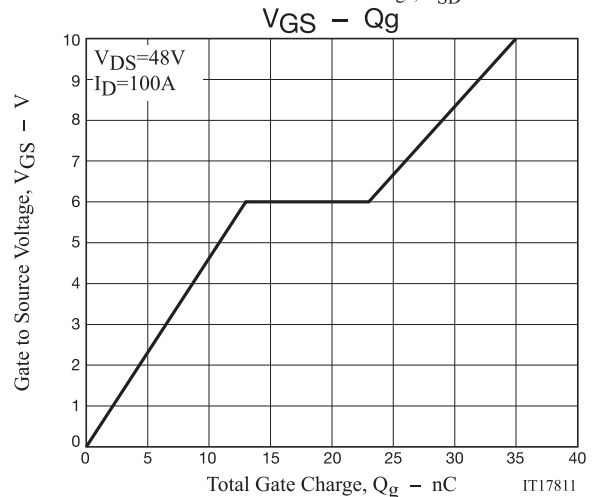
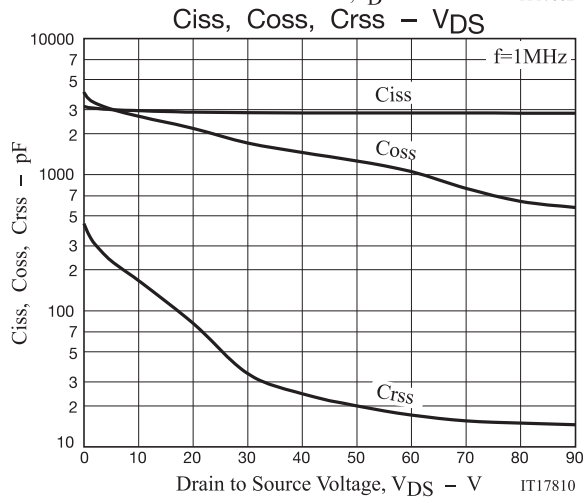
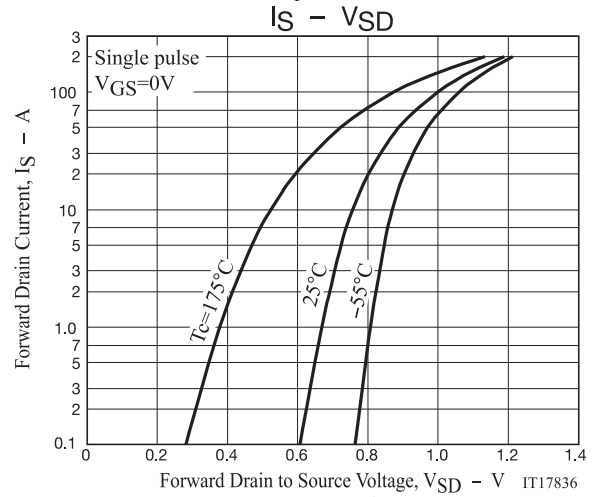
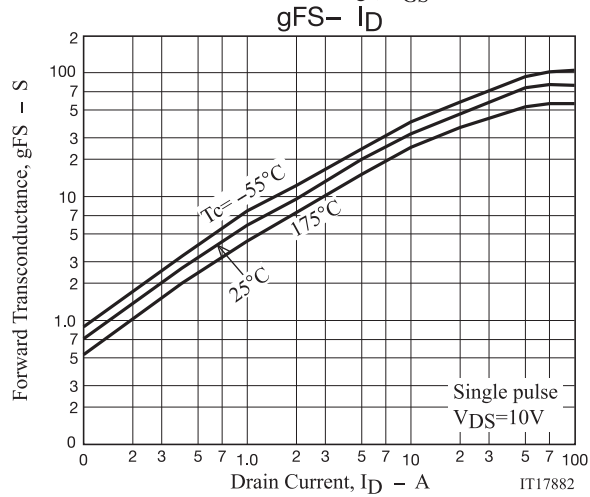
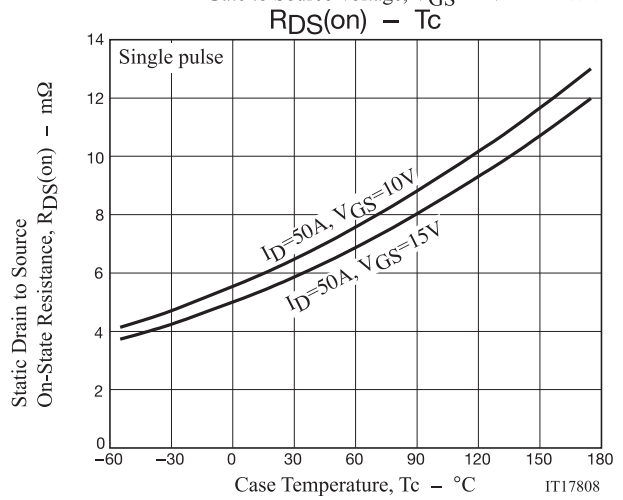
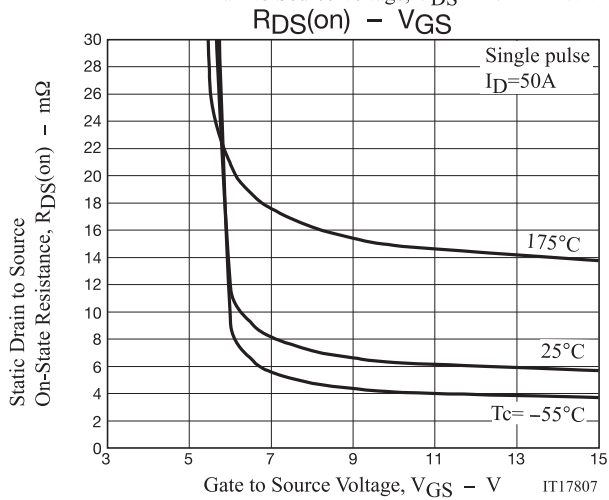
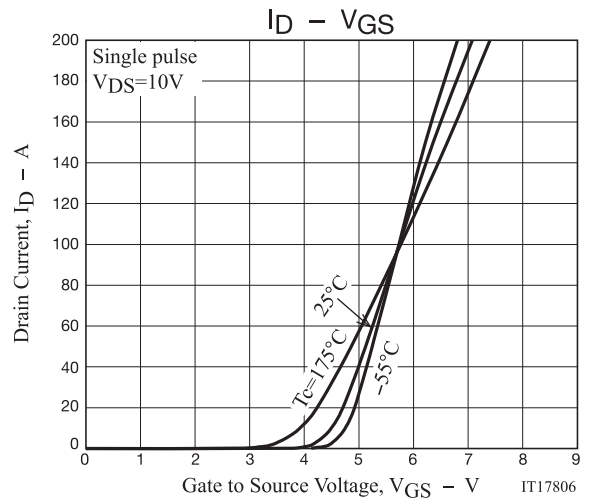
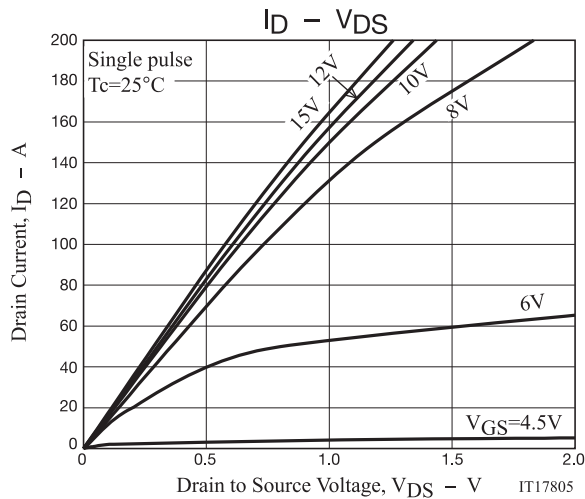
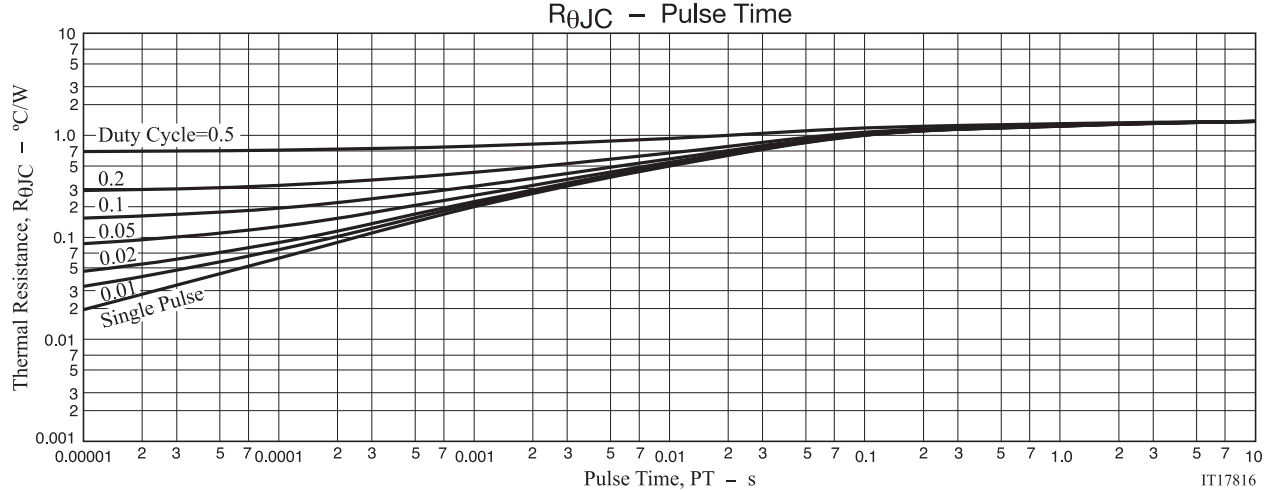
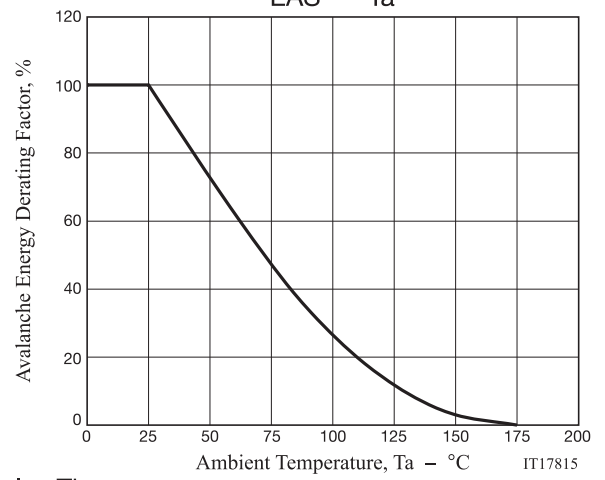
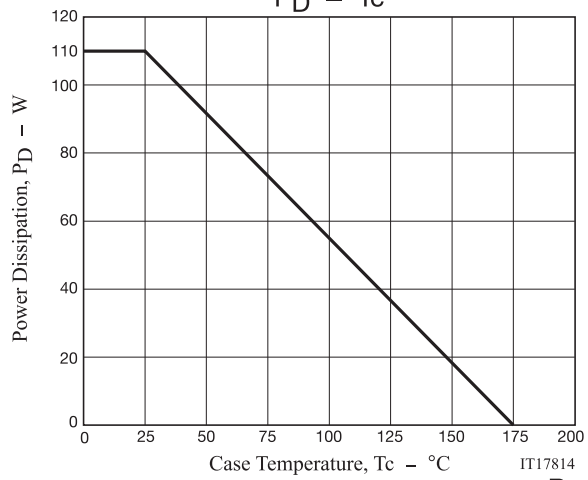
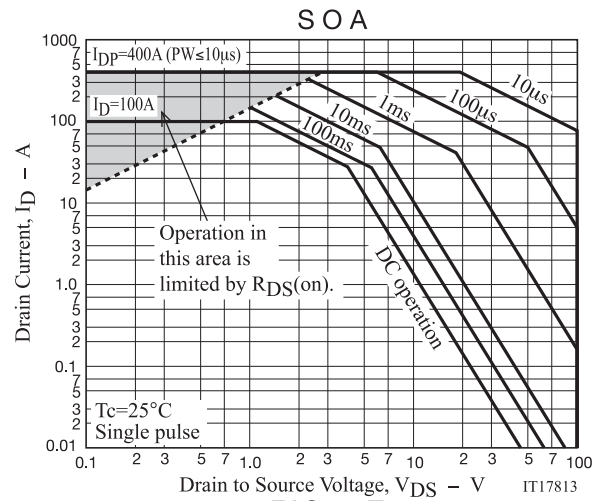
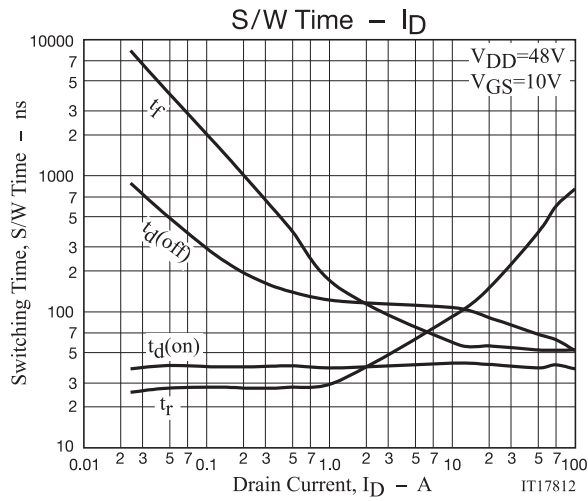


Fig.3 Reverse Recovery Time Test Circuit







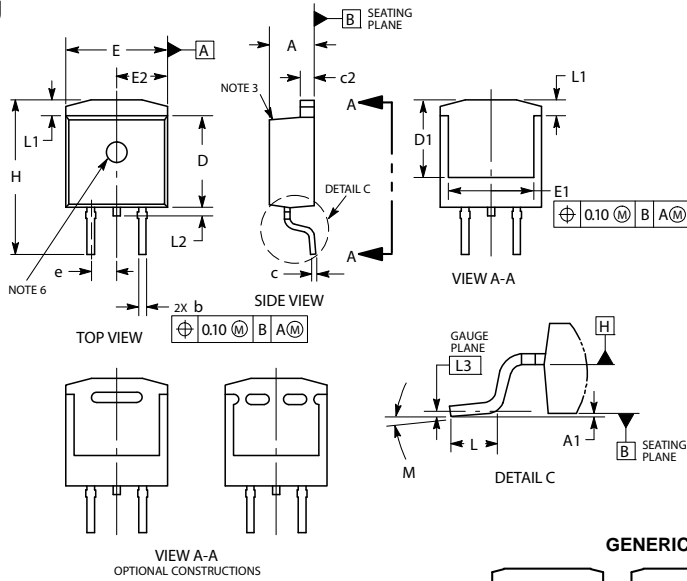
Package Dimensions

NDBA100N10BT4H

D²PAK-3 (TO-263, 3-LEAD)

CASE 418AJ

ISSUE B

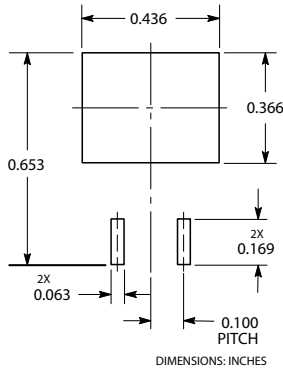


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: INCHES.
 3. CHAMFER OPTIONAL.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
 5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1 AND E1.
 6. OPTIONAL MOLD FEATURE

	INCHES		MILLIMETERS	
DIM.	MIN	MAX	MIN	MAX
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	—	6.60	—
E	0.380	0.420	9.65	10.67
E1	0.245	—	6.22	—
e	0.100 BSC	—	2.54 BSC	—
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	—	0.066	—	1.68
L2	—	0.070	—	1.78
L3	0.010 BSC	—	0.25 BSC	—
M	0°	8°	0°	8°

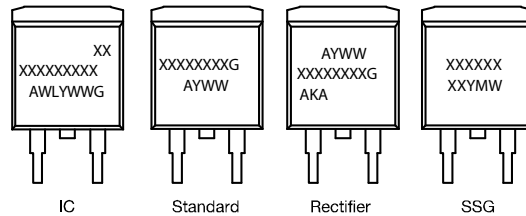
VIEW A-A
OPTIONAL CONSTRUCTIONS

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAMS*



XXXXXX = Specific Device Code
 A = Assembly Location
 WL = Wafer Lot
 Y = Year
 WW = Work Week
 W = Week Code (SSG)
 M = Month Code (SSG)
 G = Pb-Free Package
 AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

ORDERING INFORMATION

Device	Package	Shipping	note
NDBA100N10BT4H	D ² PAK-3 (TO-263, 3-LEAD)	800 pcs. / Tape & Reel	Pb-Free and Halogen Free

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

Note on usage : Since the NDBA100N10B is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

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