

NDBA180N10B

Power MOSFET 100V, 2.8mΩ, 180A, N-Channel



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Features

- Ultra Low On-Resistance
- Low Gate Charge
- High Speed Switching
- 100% Avalanche Tested
- Pb-Free, Halogen Free and RoHS compliance

Specifications

Absolute Maximum Ratings at Ta = 25°C (Note 1)

Parameter	Symbol	Value	Unit
Drain to Source Voltage	V _{DSS}	100	V
Gate to Source Voltage	V _{GSS}	±20	V
Drain Current (DC)	I _D	180	A
Drain Current (DC) Limited by Package	I _{DL}	100	A
Drain Current (Pulse) PW≤10μs, duty cycle≤1%	I _{DP}	600	A
Power Dissipation Tc=25°C	P _D	200	W
Junction Temperature	T _j	175	°C
Storage Temperature	T _{stg}	-55 to +175	°C
Source Current (Body Diode)	I _S	100	A
Avalanche Energy (Single Pulse) (Note 2)	E _{AS}	451	mJ
Lead Temperature for Soldering Purposes, 3mm from Case for 10 Seconds	T _L	260	°C

Note 1 : Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2 : V_{DD}=48V, L=100μH, I_{AV}=70A (Fig.1)

Thermal Resistance Ratings

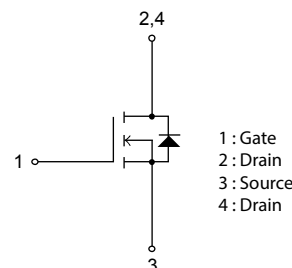
Parameter	Symbol	Value	Unit
Junction to Case Steady State	R _{θJC}	0.75	°C/W
Junction to Ambient (Note 3)	R _{θJA}	62.5	

Note 3 : Surface mounted on FR4 board using recommended footprint

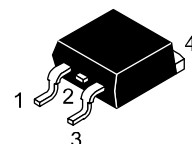
V _{DSS}	R _{DS(on)} Max	I _D Max
100V	2.8mΩ@ 15V	180A
	3.3mΩ@ 10V	

Electrical Connection

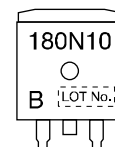
N-Channel



Marking



**TO-263
CASE 418AJ**



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

NDBA180N10B

Electrical Characteristics at Ta = 25°C (Note 4)

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D=10mA, V_{GS}=0V$	100			V
Zero-Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$			10	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			± 200	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=10V, I_D=1mA$	2		4	V
Forward Transconductance	g_{FS}	$V_{DS}=10V, I_D=50A$		150		S
Static Drain to Source On-State Resistance	$R_{DS(on)1}$	$I_D=50A, V_{GS}=15V$		2.3	2.8	$m\Omega$
	$R_{DS(on)2}$	$I_D=50A, V_{GS}=10V$		2.5	3.3	$m\Omega$
Input Capacitance	C_{iss}	$V_{DS}=50V, f=1MHz$		6,950		pF
Output Capacitance	C_{oss}			3,000		pF
Reverse Transfer Capacitance	C_{rss}			15		pF
Turn-ON Delay Time	$t_{d(on)}$	See Fig.2		95		ns
Rise Time	t_r			320		ns
Turn-OFF Delay Time	$t_{d(off)}$			185		ns
Fall Time	t_f			130		ns
Total Gate Charge	Q_g	$V_{DS}=48V, V_{GS}=10V, I_D=100A$		95		nC
Gate to Source Charge	Q_{gs}			31		nC
Gate to Drain "Miller" Charge	Q_{gd}			26		nC
Forward Diode Voltage	V_{SD}	$I_S=100A, V_{GS}=0V$		0.9	1.5	V
Reverse Recovery Time	t_{rr}	See Fig.3		150		ns
Reverse Recovery Charge	Q_{rr}	$I_S=100A, V_{GS}=0V, V_{DD}=50V, di/dt=100A/\mu s$		580		nC
Reverse Recovery Charge	Q_{rr}	$I_S=100A, V_{GS}=0V, V_{DD}=50V, di/dt=100A/\mu s$		580		nC

Note 4 : Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Fig.1 Unclamped Inductive Switching Test Circuit

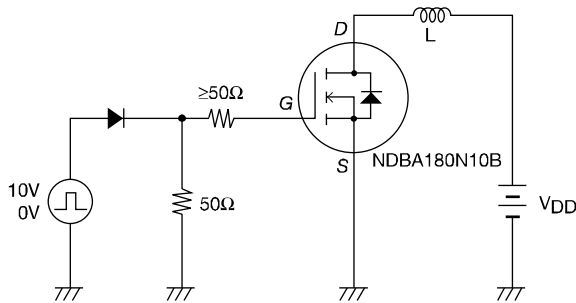


Fig.2 Switching Time Test Circuit

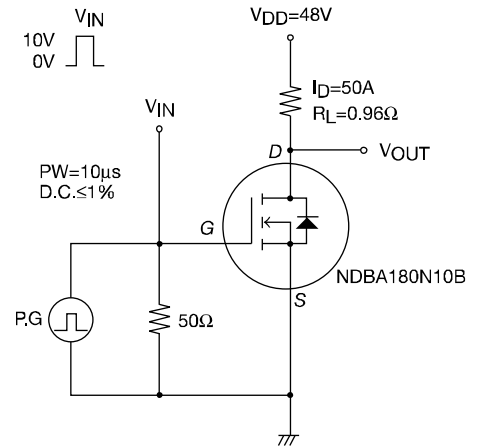
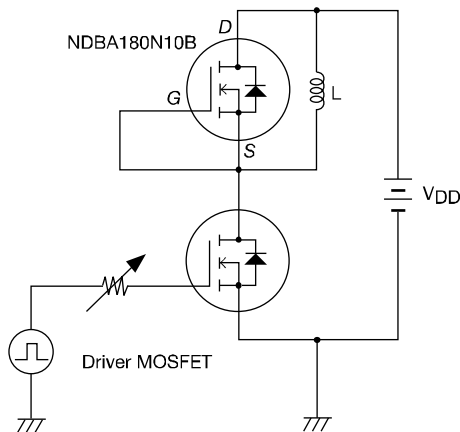
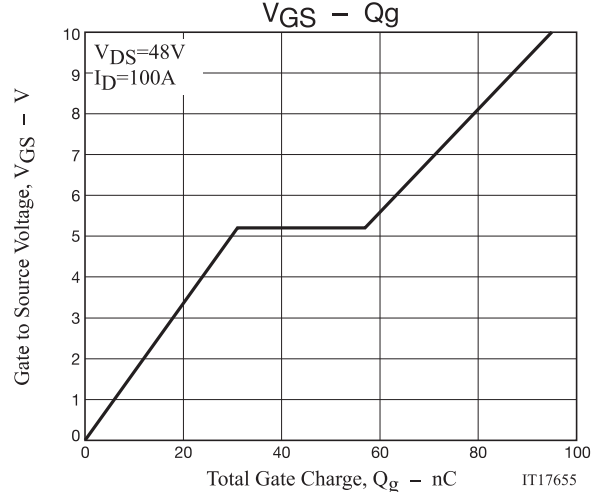
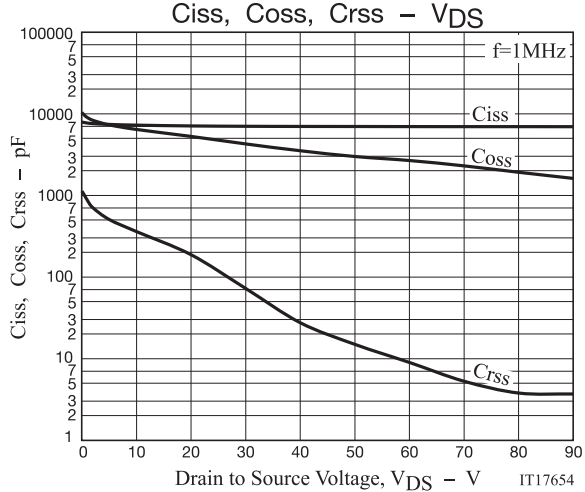
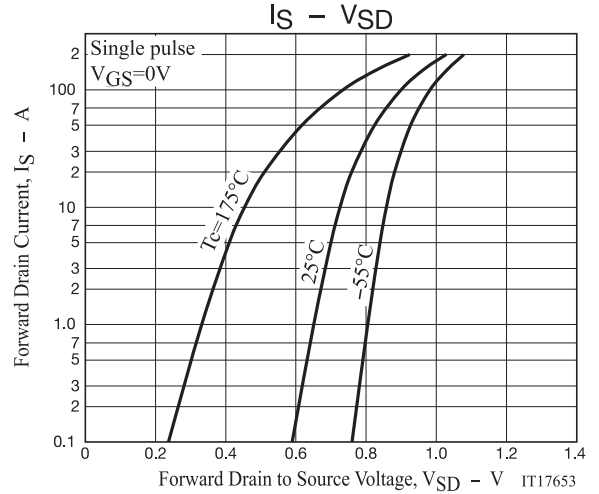
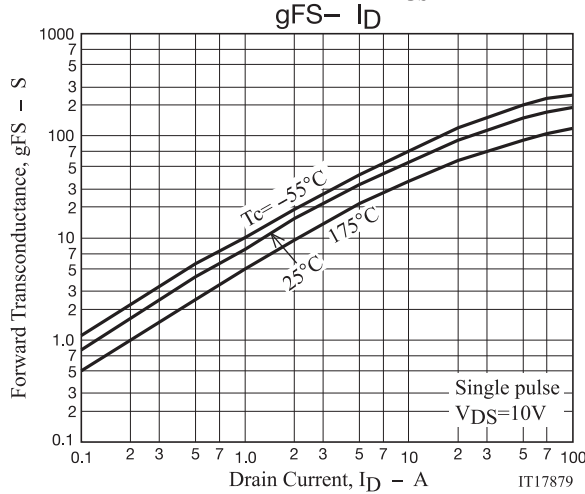
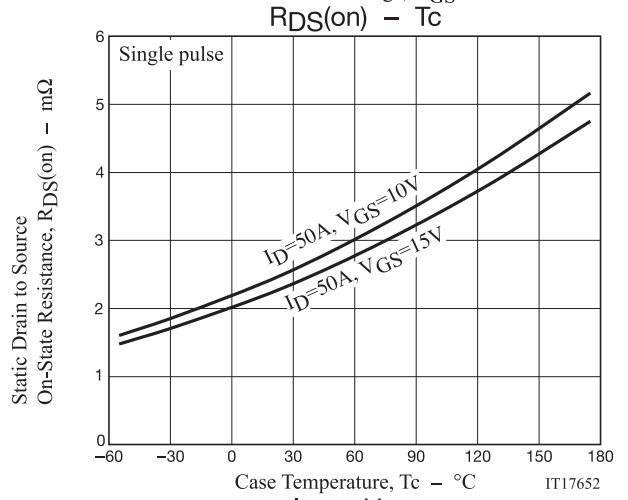
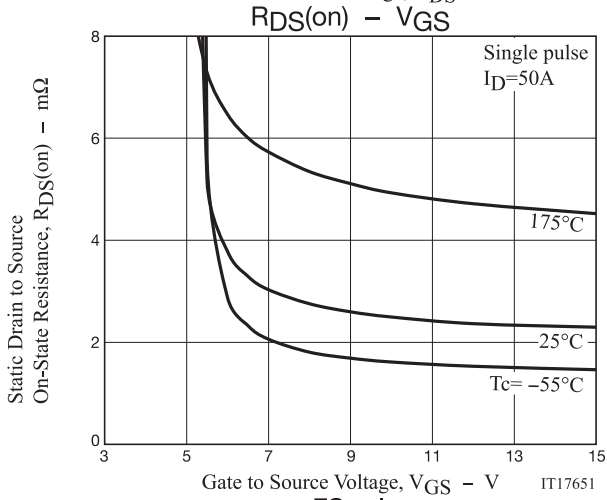
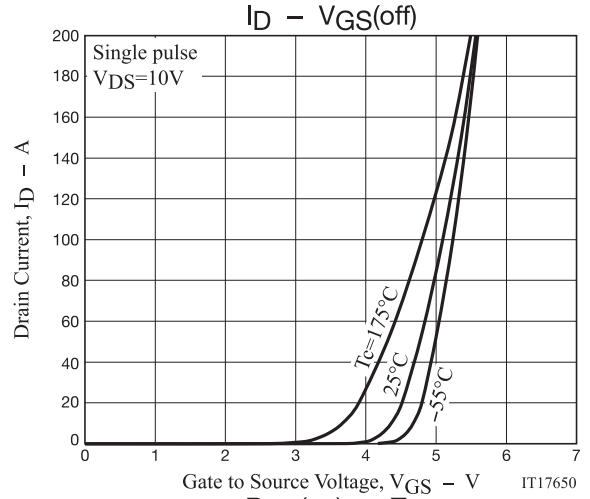
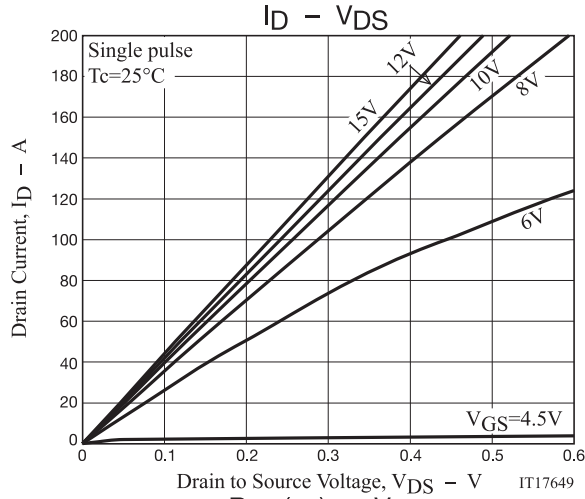


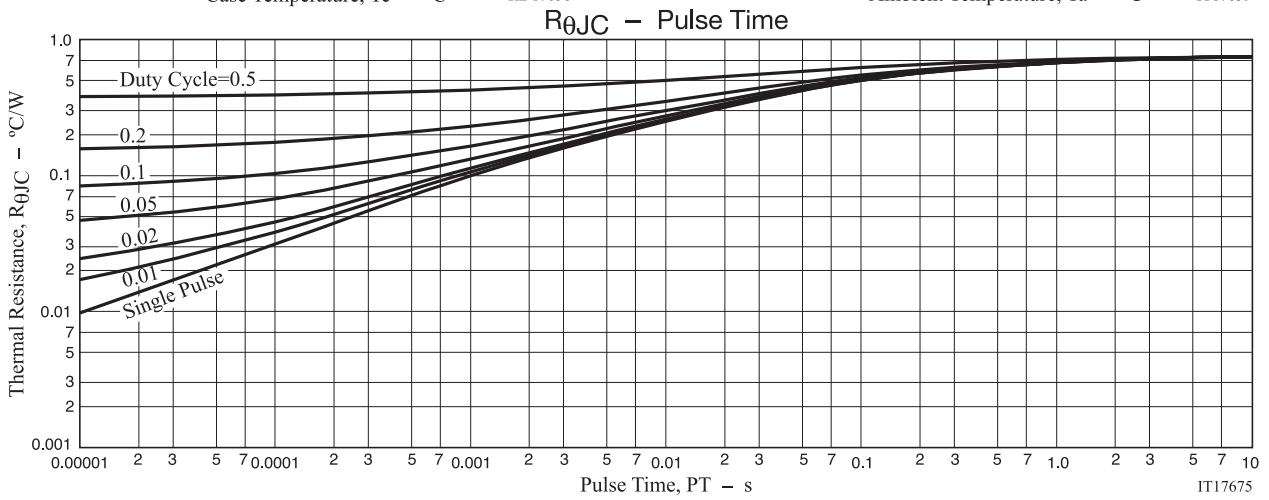
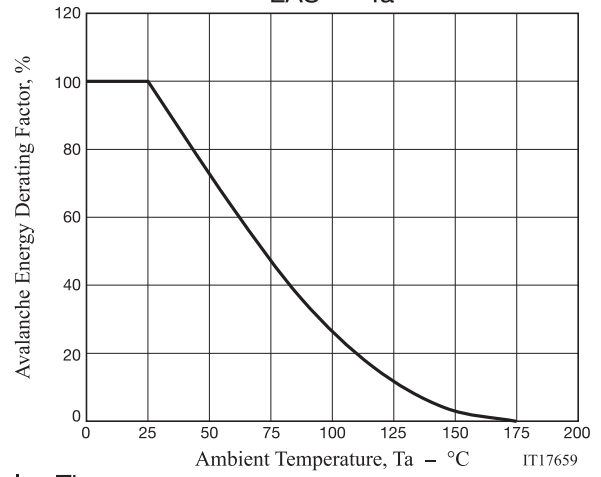
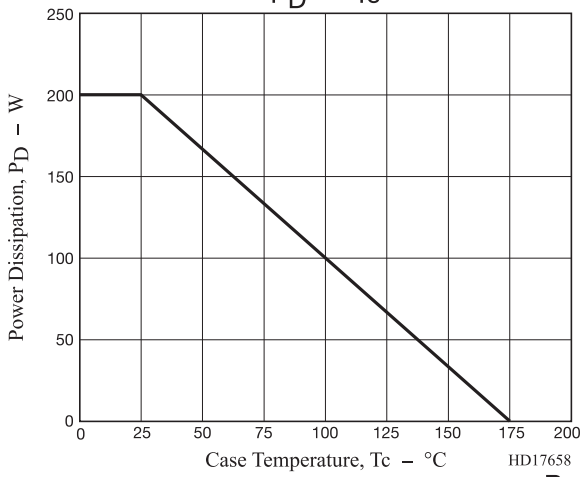
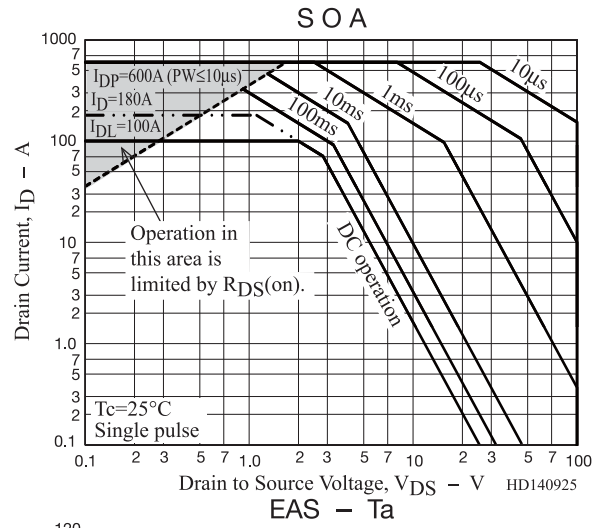
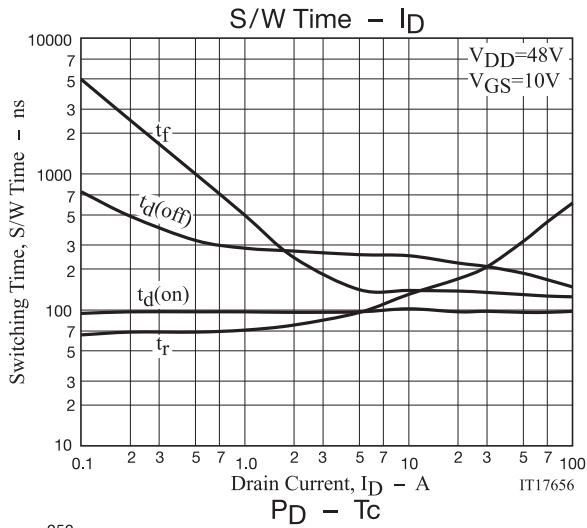
Fig.3 Reverse Recovery Time Test Circuit



NDBA180N10B



NDBA180N10B



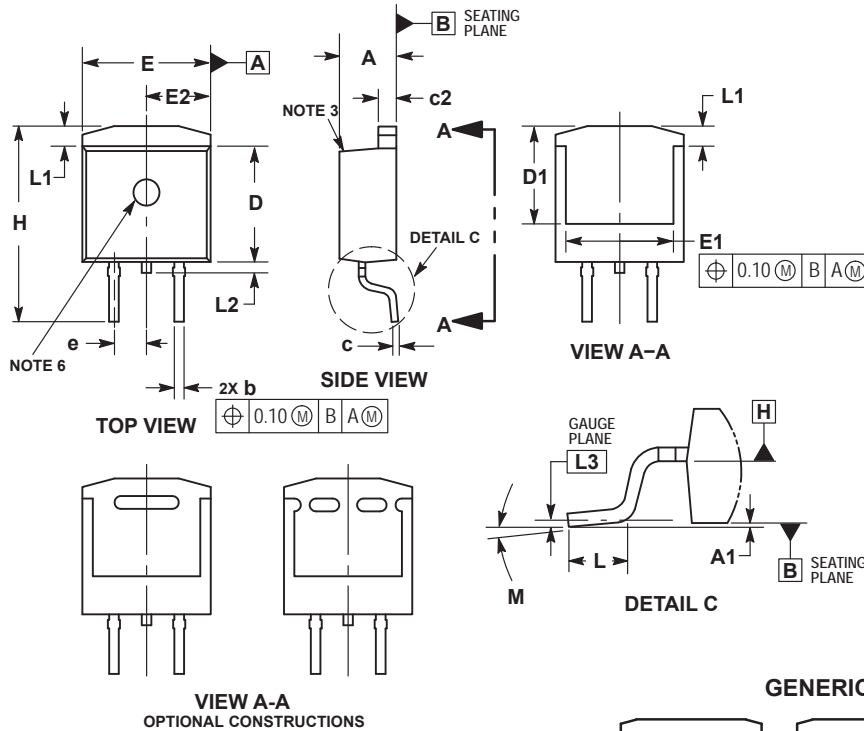
Package Dimensions

unit : mm

D²PAK-3 (TO-263, 3-LEAD)

CASE 418AJ

ISSUE B

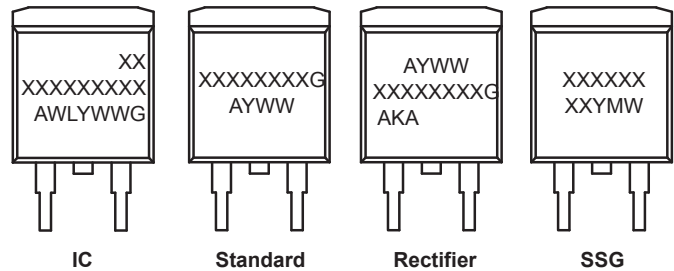


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. CHAMFER OPTIONAL
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1 AND E1.
6. OPTIONAL MOLD FEATURE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100 BSC		2.54 BSC	
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010 BSC		0.25 BSC	
M	0°		8°	

GENERIC MARKING DIAGRAMS*



XXXXXX = Specific Device Code

A = Assembly Location

WL = Wafer Lot

Y = Year

WW = Work Week

W = Week Code (SSG)

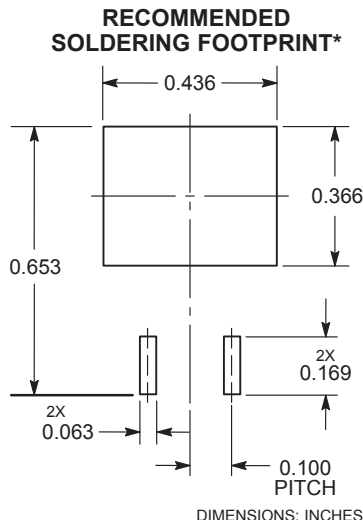
M = Month Code (SSG)

G = Pb-Free Package

AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



NDBA180N10B

ORDERING INFORMATION

Device	Package	Shipping	Note
NDBA180N10BT4H	D ² PAK-3 (TO-263, 3-LEAD)	800 pcs. / Tape & Reel	Pb-Free and Halogen Free

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

Note on usage : Since the NDBA180N10B is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

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