

NTB90N02, NTP90N02

Power MOSFET 90 Amps, 24 Volts N-Channel D²PAK and TO-220

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

Features

- Pb-Free Packages are Available

Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V _{DSS}	24	Vdc
Gate-to-Source Voltage – Continuous	V _{GS}	±20	Vdc
Drain Current – Continuous @ T _A = 25°C – Single Pulse (t _p = 10 μs)	I _D I _{DM}	90* 200	A A
Total Power Dissipation @ T _A = 25°C Derate above 25°C	P _D	85 0.66	W W/°C
Operating and Storage Temperature	T _J , T _{stg}	–55 to +150	°C
Single Pulse Drain-to-Source Avalanche Energy – Starting T _J = 25°C (V _{DD} = 28 Vdc, V _{GS} = 10 Vdc, L = 5.0 mH, I _{L(pk)} = 17 A, R _G = 25 Ω)	E _{AS}	733	mJ
Thermal Resistance Junction-to-Case Junction-to-Ambient (Note 1)	R _{θJC} R _{θJA}	1.55 70	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T _L	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using 1" pad size, (Cu Area 1.127 in²).
2. When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 in²).

*Chip current capability limited by package.

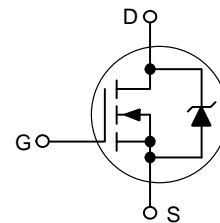


ON Semiconductor®

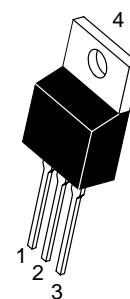
<http://onsemi.com>

V _{(BR)DSS}	R _{DS(on)} TYP	I _D MAX
24 V	5.0 mΩ @ 10 V	90 A
	7.5 mΩ @ 4.5 V	

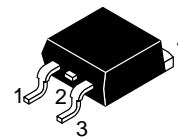
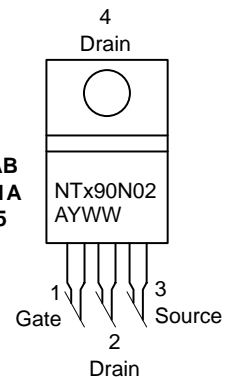
N-Channel



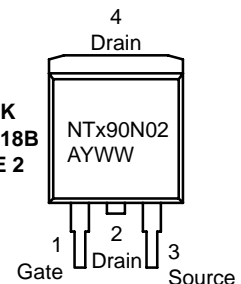
MARKING DIAGRAMS



**TO-220AB
CASE 221A
STYLE 5**



**D²PAK
CASE 418B
STYLE 2**



NTx90N02 = Device Code

x = P or B

A = Assembly Location

Y = Year

WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

NTB90N02, NTP90N02

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) (V _{GS} = 0 Vdc, I _D = 250 μAdc) Temperature Coefficient (Positive)	V _{(BR)DSS}	24 -	27 25	- -	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{DS} = 24 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 24 Vdc, V _{GS} = 0 Vdc, T _J = 150°C)	I _{DSS}	- -	- -	1.0 10	μAdc
Gate-Body Leakage Current (V _{GS} = ± 20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	-	-	±100	nAdc

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) (V _{DS} = V _{GS} , I _D = 250 μAdc) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	1.0 -	1.9 -3.8	3.0 -	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V _{GS} = 10 Vdc, I _D = 90 Adc) (V _{GS} = 4.5 Vdc, I _D = 40 Adc) (V _{GS} = 10 Vdc, I _D = 20 Adc) (V _{GS} = 4.5 Vdc, I _D = 20 Adc)	R _{DS(on)}	- - - -	5.0 7.5 5.0 7.5	5.8 9.0 5.8 9.0	mΩ
Forward Transconductance (Note 3) (V _{DS} = 15 Vdc, I _D = 10 Adc)	g _{FS}	-	25	-	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 20 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{ISS}	-	2120	-	pF
Output Capacitance		C _{OSS}	-	900	-	
Transfer Capacitance		C _{RSS}	-	360	-	

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	(V _{DD} = 20 Vdc, I _D = 20 Adc, V _{GS} = 4.5 Vdc, R _G = 2.5 Ω)	t _{d(on)}	-	16	-	ns
Rise Time		t _r	-	90	-	
Turn-Off Delay Time		t _{d(off)}	-	28	-	
Fall Time		t _f	-	60	-	
Gate Charge	(V _{DS} = 20 Vdc, I _D = 20 Adc, V _{GS} = 4.5 Vdc) (Note 3)	Q _T	-	29	-	nC
		Q ₁	-	8.0	-	
		Q ₂	-	20	-	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I _S = 2.3 Adc, V _{GS} = 0 Vdc) (I _S = 40 Adc, V _{GS} = 0 Vdc) (Note 3) (I _S = 2.3 Adc, V _{GS} = 0 Vdc, T _J = 150°C)	V _{SD}	- - -	0.75 1.2 0.65	1.0 - -	Vdc
Reverse Recovery Time	(I _S = 2.3 Adc, V _{GS} = 0 Vdc, di _S /dt = 100 A/μs) (Note 3)	t _{rr}	-	40	-	ns
		t _a	-	21	-	
		t _b	-	18	-	
Reverse Recovery Stored Charge		Q _{RR}	-	0.036	-	μC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

NTB90N02, NTP90N02

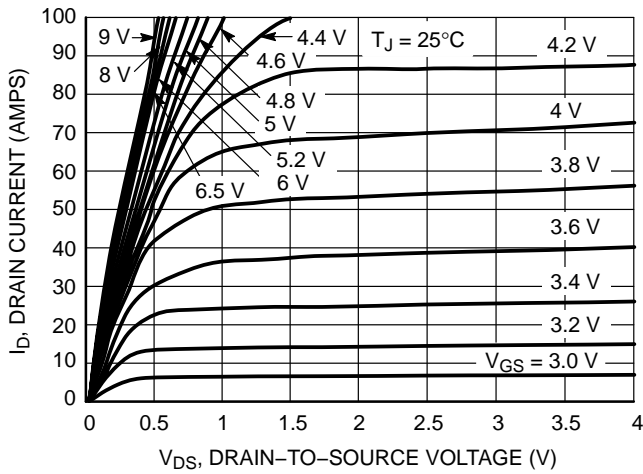


Figure 1. On-Region Characteristics

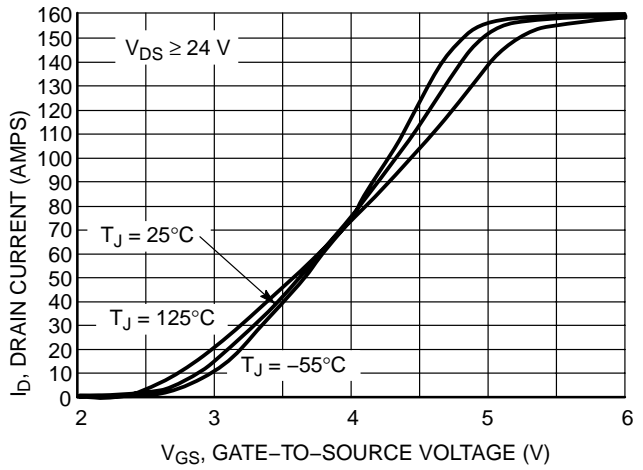


Figure 2. Transfer Characteristics

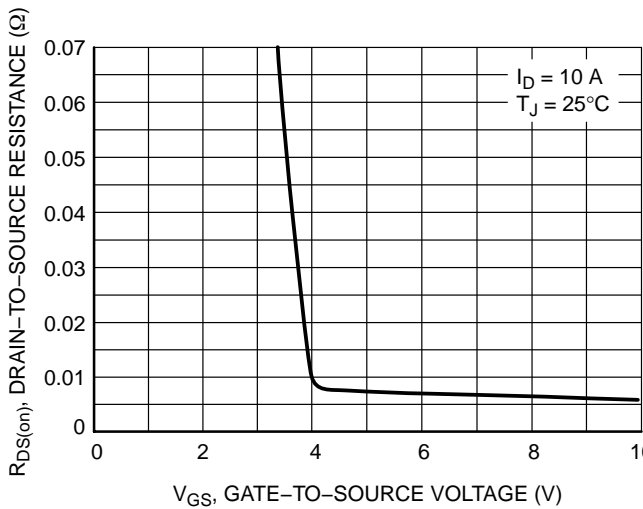


Figure 3. On-Resistance versus Gate-to-Source Voltage

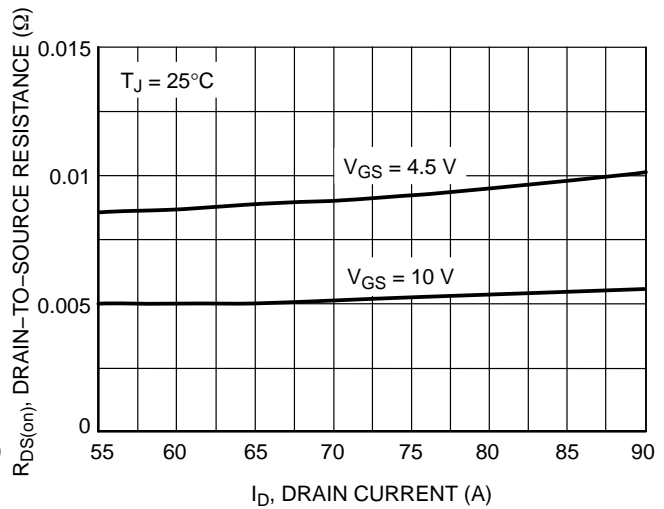


Figure 4. On-Resistance versus Drain Current and Gate Voltage

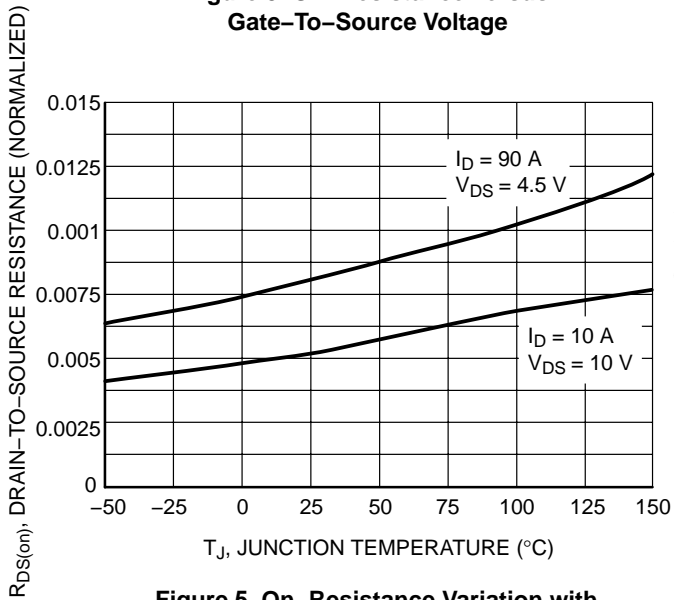


Figure 5. On-Resistance Variation with Temperature

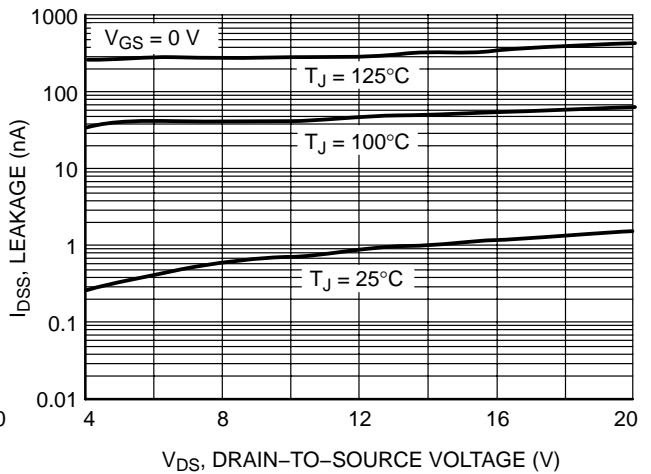


Figure 6. Drain-to-Source Leakage Current versus Voltage

NTB90N02, NTP90N02

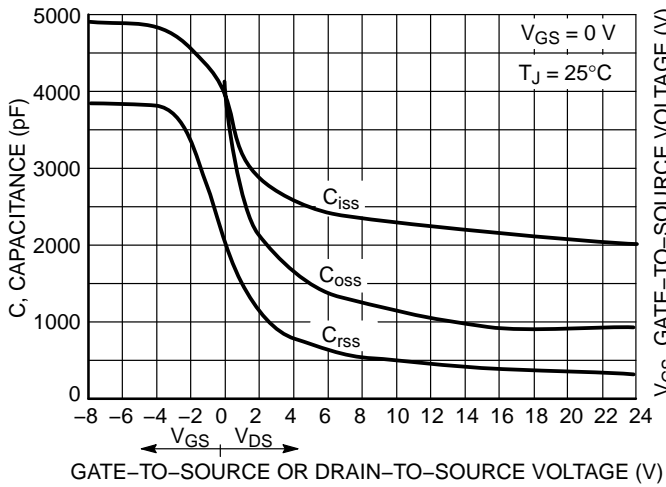


Figure 7. Capacitance Variation

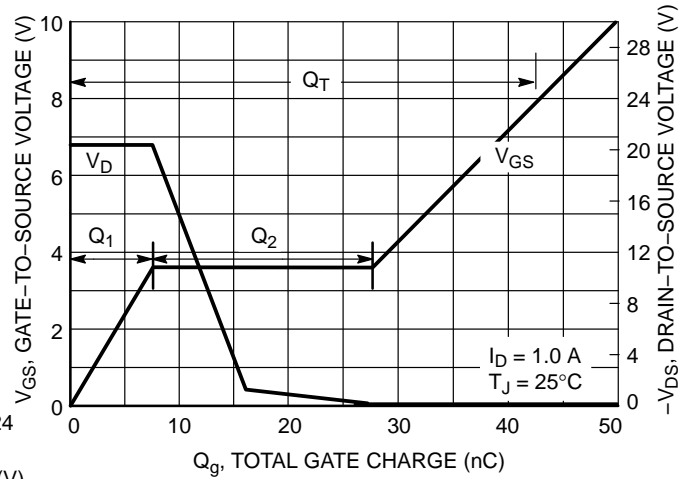


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

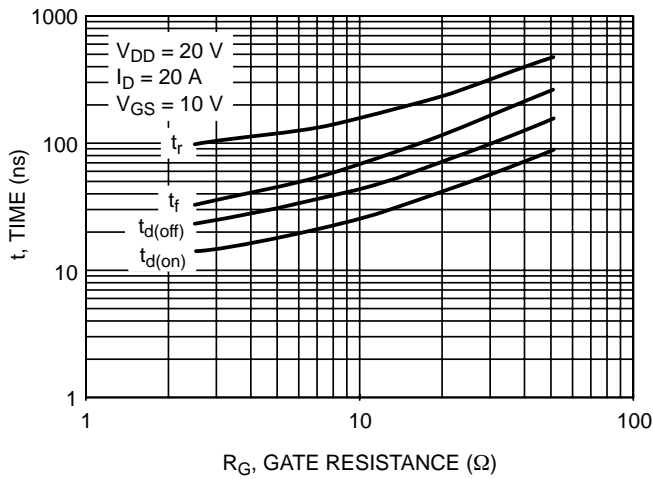


Figure 9. Resistive Switching Time Variation versus Gate Resistance

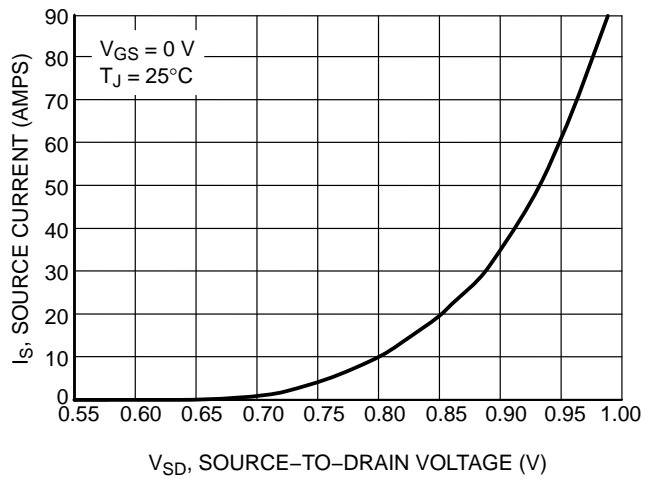


Figure 10. Diode Forward Voltage versus Current

ORDERING INFORMATION

Device	Package	Shipping†
NTP90N02	TO-220AB	50 Units / Rail
NTP90N02G	TO-220AB (Pb-Free)	50 Units / Rail
NTB90N02	D ² PAK	50 Units / Rail
NTB90N02G	D ² PAK (Pb-Free)	50 Units / Rail
NTB90N02T4	D ² PAK	800 Tape & Reel
NTB90N02T4G	D ² PAK (Pb-Free)	800 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain-gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$$t = Q/I_{G(AV)}$$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP} . Therefore, rise and fall times may be approximated by the following:

$$t_r = Q_2 \times R_2 / 10(V_{GG} - V_{GSP})$$

$$t_f = Q_2 \times R_2 / V_{GSP}$$

where:

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn-on and turn-off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network.

The equations are:

$$t_{d(on)} = R_G C_{iss} \ln [V_{GG} / (V_{GG} - V_{GSP})]$$

$$t_{d(off)} = R_G C_{iss} \ln (V_{GG} / V_{GSP})$$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off-state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on-state when calculating $t_{d(off)}$.

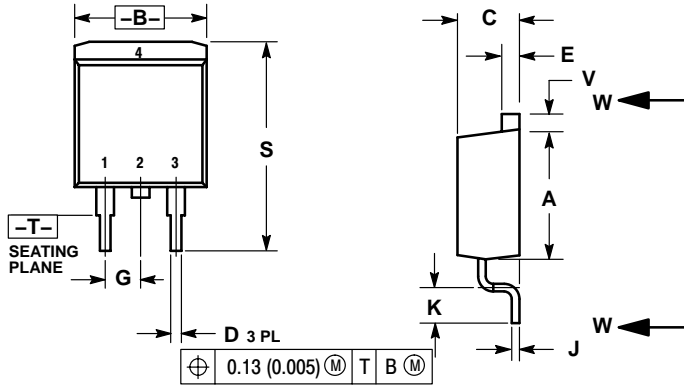
At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by $L di/dt$, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

NTB90N02, NTP90N02

PACKAGE DIMENSIONS

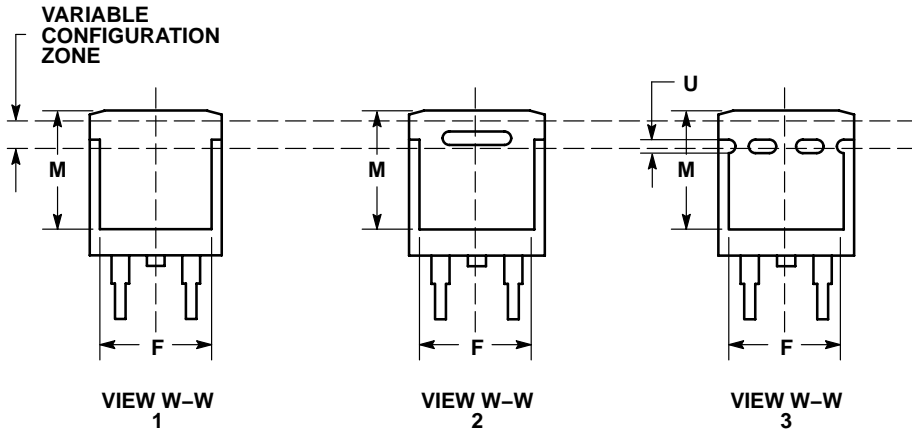
D²PAK
CASE 418AA-01
ISSUE O



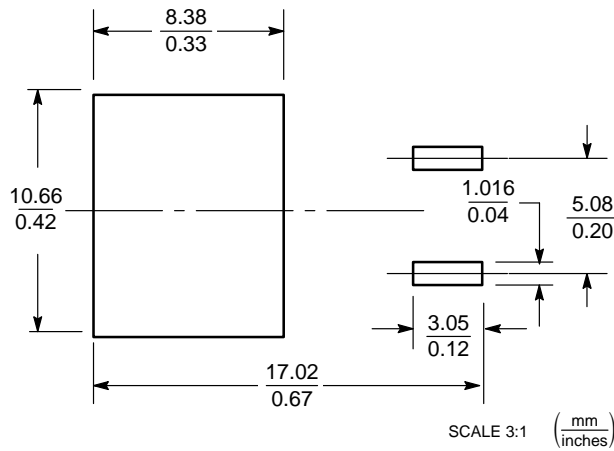
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.036	0.51	0.92
E	0.045	0.055	1.14	1.40
F	0.310	---	7.87	---
G	0.100 BSC		2.54 BSC	
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
M	0.280	---	7.11	---
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

- STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN



SOLDERING FOOTPRINT*

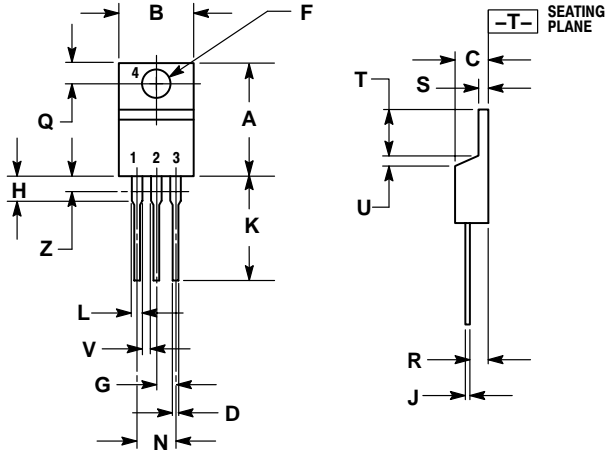


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NTB90N02, NTP90N02

PACKAGE DIMENSIONS

TO-220
CASE 221A-09
ISSUE AA



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

- STYLE 5:
1. GATE
 2. DRAIN
 3. SOURCE
 4. DRAIN

NTB90N02, NTP90N02

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA

Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada

Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada

Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your
local Sales Representative.