NTS4001N, NVS4001N

Small Signal MOSFET

30 V, 270 mA, Single N−Channel, SC−70

Features

- Low Gate Charge for Fast Switching
- Small Footprint − 30% Smaller than TSOP−6
- ESD Protected Gate
- AEC−Q101 Qualified and PPAP Capable − NVS4001N
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Low Side Load Switch
- Li−Ion Battery Supplied Devices − Cell Phones, PDAs, DSC
- Buck Converters
- Level Shifts

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Units
Drain−to−Source Voltage			V_{DSS}	30	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25 °C	I_D	270	mA
		T_A = 85 °C		200	
Power Dissipation (Note 1)	Steady State	T_A = 25 °C	P_D	330	mW
Pulsed Drain Current		t =10 μs	I_{DM}	800	mA
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Source Current (Body Diode)			I_S	270	mA
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface mounted on FR4 board using 1 in sq. pad size (Cu area = 1.127 in sq. [1 oz] including traces).

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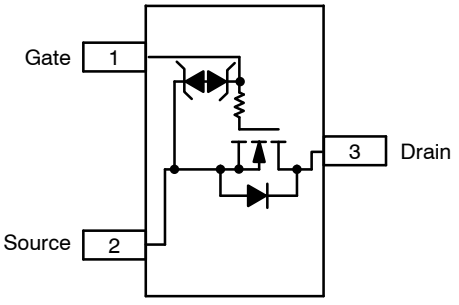
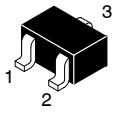
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D Max
30 V	1.0 Ω @ 4.0 V	270 mA
	1.5 Ω @ 2.5 V	

SC−70/SOT−323 (3 LEADS)

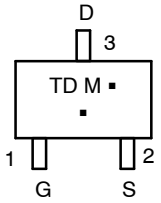


(Top View)



SC−70 / SOT−323
CASE 419
STYLE 8

MARKING DIAGRAM & PIN ASSIGNMENT



TD = Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
NTS4001NT1G	SC−70 (Pb−Free)	3000 / Tape & Reel
NVS4001NT1G	SC−70 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 100 μA	30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			60		mV/ °C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 30 V			1.0	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±10 V			±1.0	μA
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 100 μA	0.8	1.2	1.5	V
Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			−3.4		mV/ °C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 4.0 V, I_D = 10 mA		1.0	1.5	Ω
		V_{GS} = 2.5 V, I_D = 10 mA		1.5	2.0	
Forward Transconductance	g_{FS}	V_{DS} = 3.0 V, I_D = 10 mA		80		mS
CHARGES AND CAPACITANCES						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 5.0 V		20	33	pF
Output Capacitance	C_{OSS}			19	32	
Reverse Transfer Capacitance	C_{RSS}			7.25	12	
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 5.0 V, V_{DS} = 24 V, I_D = 0.1 A		0.9	1.3	nC
Threshold Gate Charge	$Q_{G(TH)}$			0.2		
Gate−to−Source Charge	Q_{GS}			0.3		
Gate−to−Drain Charge	Q_{GD}			0.2		
SWITCHING CHARACTERISTICS (Note 3)						
Turn−On Delay Time	$td_{(ON)}$	V_{GS} = 4.5 V, V_{DD} = 5.0 V, I_D = 10 mA, R_G = 50 Ω		17		ns
Rise Time	tr			23		
Turn−Off Delay Time	$td_{(OFF)}$			94		
Fall Time	tf			82		
DRAIN−SOURCE DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 10 mA, T_J = 25°C		0.65	0.7	V
		V_{GS} = 0 V, I_S = 10 mA, T_J = 125°C		0.43		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 8.0 A/μs, I_S = 10 mA		5.0		ns

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

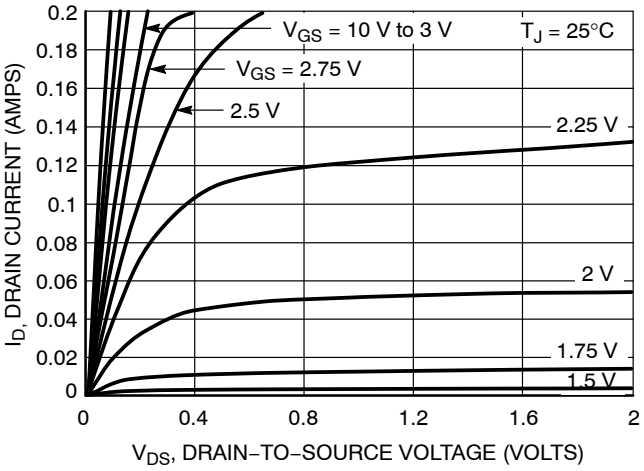


Figure 1. On−Region Characteristics

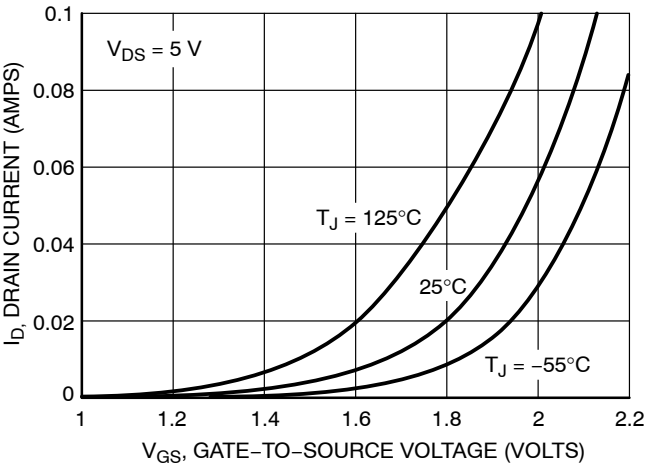


Figure 2. Transfer Characteristics

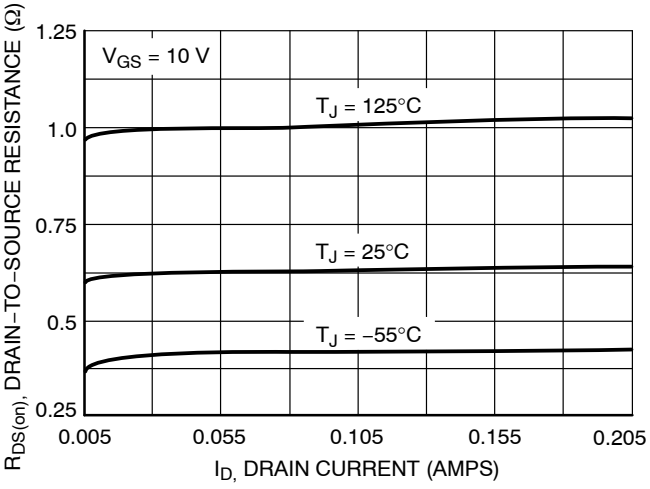


Figure 3. On−Resistance vs. Drain Current and Temperature

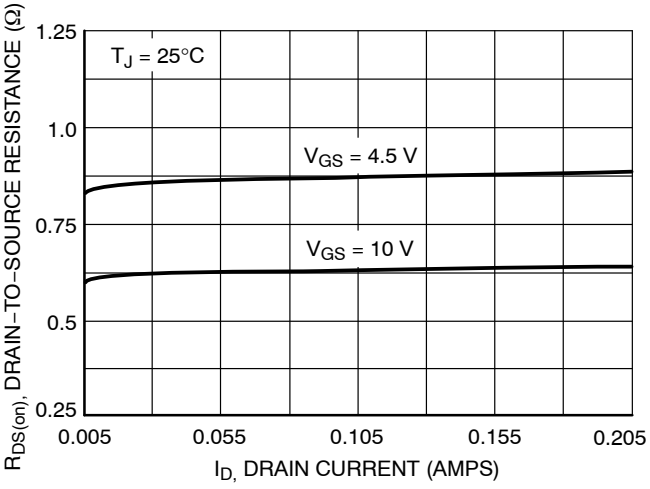


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

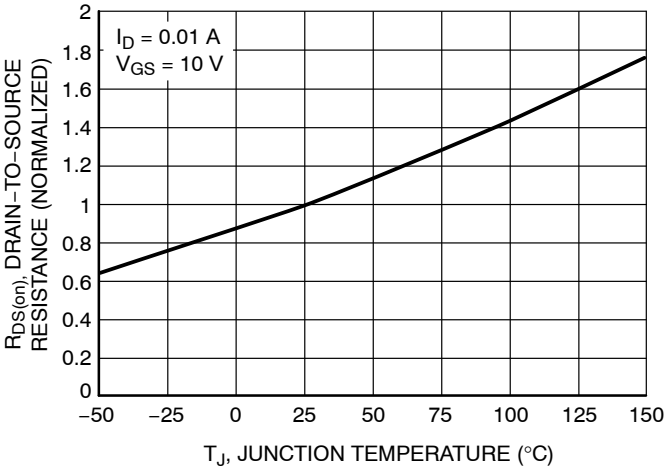


Figure 5. On−Resistance Variation with Temperature

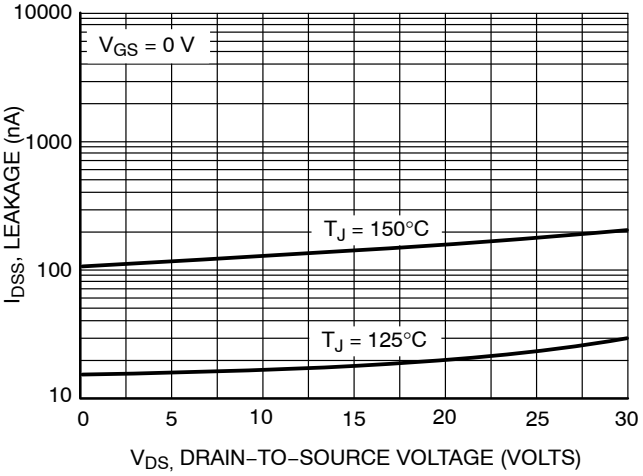


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

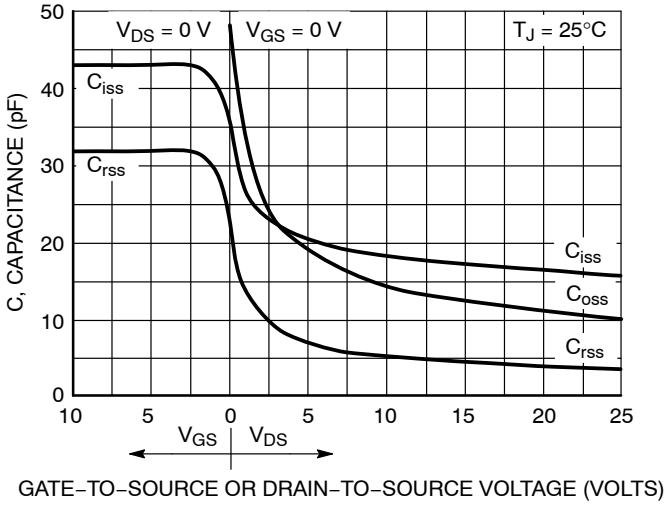


Figure 7. Capacitance Variation

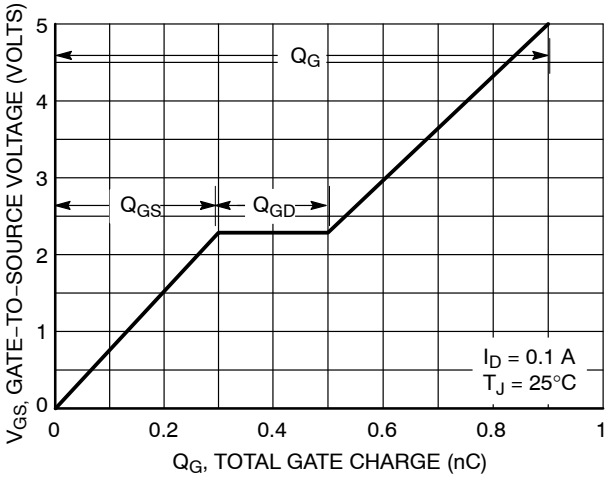


Figure 8. Gate−to−Source Voltage vs. Total Gate Charge

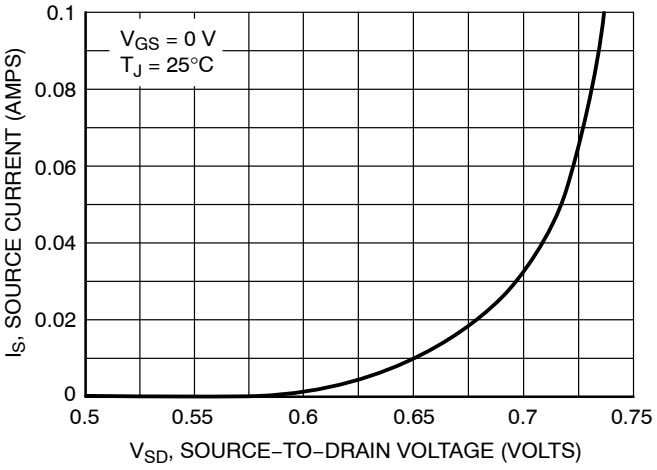
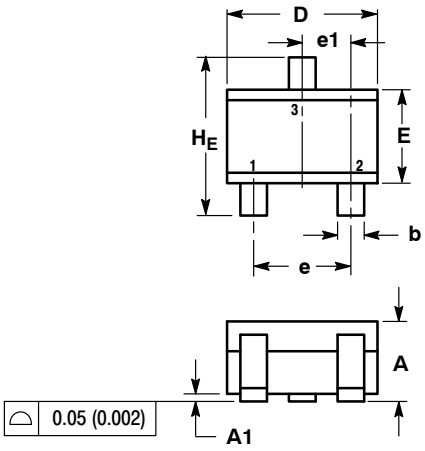
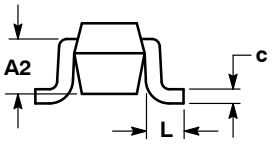


Figure 9. Diode Forward Voltage vs. Current

PACKAGE DIMENSIONS

SC−70 (SOT−323)
CASE 419−04
ISSUE N



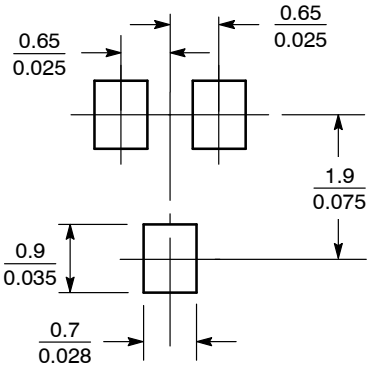


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2		0.70 REF			0.028 REF	
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.10	2.20	0.071	0.083	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1		0.65 BSC			0.026 BSC	
L	0.20	0.38	0.56	0.008	0.015	0.022
H_E	2.00	2.10	2.40	0.079	0.083	0.095

STYLE 8:
PIN 1. GATE
2. SOURCE
3. DRAIN

SOLDERING FOOTPRINT*



SCALE 10:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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