

# STK5F1U3E3D-E



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## Inverter Power IPM for 3-phase Motor Drive

### Overview

This “Inverter Power IPM” is highly integrated device containing all High Voltage (HV) control from HV-DC to 3-phase outputs in a single DIP module (Dual-In line Package). Output stage uses IGBT/FRD technology and implements Under Voltage Protection (UVP) and Over Current Protection (OCP) with a Fault Detection output flag. Internal Boost diodes are provided for high side gate boost drive.

### Function

- Single control power supply due to Internal bootstrap circuit for high side pre-driver circuit
- All control input and status output are at low voltage levels directly compatible with microcontrollers
- Built-in cross conduction prevention
- Externally accessible embedded thermistor for substrate temperature measurement
- The level of the over-current protection current is adjustable with the external resistor, “RSD”
- Low switching noise by optimized the gate resistor

### Certification

- UL1557 (File Number: E339285)

### Specifications

**Absolute Maximum Ratings** at  $T_c = 25^\circ\text{C}$

Parameter	Symbol	Remarks	Ratings	Unit
Supply voltage	$V_{CC}$	P to N, surge < 500V *1	450	V
Collector-emitter voltage	$V_{CE}$	P to U,V,W or U,V,W to N	600	V
Output current	$I_o$	P, N, U, V, W terminal current	$\pm 50$	A
		P, N, U, V, W terminal current, $T_c = 100^\circ\text{C}$	$\pm 25$	
Output peak current	$I_{op}$	P, N, U, V, W terminal current, $PW = 1\text{ms}$	$\pm 76$	A
Pre-driver supply voltage	$VD1,2,3,4$	VB1 to VS1, VB2 to VS2, VB3 to VS3, $V_{DD}$ to $V_{SS}$ *2	20	V
Input signal voltage	$V_{IN}$	HIN1, 2, 3, LIN1, 2, 3	-0.3 to $V_{DD}$	V
FAULT terminal voltage	$V_{FAULT}$	FAULT terminal	-0.3 to $V_{DD}$	V
Maximum loss	$P_d$	IGBT per channel	67.5	W
Junction temperature	$T_j$	IGBT, FRD	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-40 to +125	$^\circ\text{C}$
Operating temperature	$T_c$	IPM case	-20 to +100	$^\circ\text{C}$
Tightening torque	MT	A screw part at use M4 type screw *3	1.17	Nm
Withstand voltage	$V_{is}$	50Hz sine wave AC 1 minute *4	2000	VRMS

Reference voltage is N terminal =  $V_{SS}$  terminal voltage unless otherwise specified.

\*1: Surge voltage developed by the switching operation due to the wiring inductance between the P and N terminals.

\*2: Terminal voltage:  $VD1 = VB1 - VS1$ ,  $VD2 = VB2 - VS2$ ,  $VD3 = VB3 - VS3$ ,  $VD4 = V_{DD} - V_{SS}$ .

\*3: Flatness of the heat-sink should be 0.25mm and below.

\*4: Test conditions: AC 2500V, 1 second.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 16 of this data sheet.

# STK5F1U3E3D-E

**Electrical Characteristics** at Tc = 25°C, VD1, VD2, VD3, VD4=15V

Parameter	Symbol	Conditions		Test circuit	Ratings			Unit
					Min.	Typ.	Max.	
Power output section								
Collector to emitter cut-off current	I <sub>CE</sub>	V <sub>CE</sub> =600V		Fig.1	-	-	100	μA
Bootstrap diode reverse current	I <sub>R(BD)</sub>	V <sub>R(BD)</sub> =600V			-	-	100	μA
Collector to emitter saturation voltage	V <sub>CE(sat)</sub>	I <sub>c</sub> =50A	Upper side	Fig.2	-	1.7	2.6	V
			Lower side*1		-	2.3	3.2	
		I <sub>c</sub> =25A, T <sub>j</sub> =100°C	Upper side		-	1.35	-	
			Lower side*1		-	1.75	-	
Diode forward voltage	V <sub>F</sub>	I <sub>F</sub> =50A	Upper side	Fig.3	-	1.8	2.7	V
			Lower side*1		-	2.4	3.3	
		I <sub>F</sub> =25A, T <sub>j</sub> =100°C	Upper side		-	1.45	-	
			Lower side*1		-	1.85	-	
Junction to case thermal resistance	θ <sub>j-c</sub> (T)	IGBT		-	-	1.5	-	°C/W
	θ <sub>j-c</sub> (D)	FWD		-	-	1.8	-	°C/W
Control (Pre-driver) section								
Pre-drive power supply consumption current	I <sub>D</sub>	V <sub>D1, 2, 3</sub> =15V		Fig.4	-	0.05	0.4	mA
		V <sub>D4</sub> =15V			-	1.0	4.0	
High level input voltage	V <sub>in H</sub>	H <sub>IN1</sub> , H <sub>IN2</sub> , H <sub>IN3</sub> ,		-	2.5	-	-	V
Low level input voltage	V <sub>in L</sub>	L <sub>IN1</sub> , L <sub>IN2</sub> , L <sub>IN3</sub> to V <sub>SS</sub>		-	-	-	0.8	V
Logic 1 input leakage current	I <sub>IN+</sub>	V <sub>IN</sub> =+3.3V		-	-	100	195	μA
Logic 0 input leakage current	I <sub>IN-</sub>	V <sub>IN</sub> =0V		-	-	-	1	μA
Bootstrap limiting resistor	R <sub>Boot</sub>			-	-	39	-	Ω
Gate resistor	R <sub>b</sub>			-	-	1	-	Ω
	R <sub>g</sub>			-	-	36	-	Ω
Protection section								
Over-current protection current	I <sub>SD</sub>	P <sub>W</sub> =100μs,R <sub>SD</sub> =0Ω		Fig.5	57	-	76	A
Over-current protection noise filter time constant	I <sub>SDNF</sub>			-	-	2.0	-	us
V <sub>dd</sub> and V <sub>Bx</sub> supply undervoltage positive going input threshold	V <sub>ddUV+</sub> V <sub>BxUV+</sub>			-	10.6	11.1	11.6	V
V <sub>dd</sub> and V <sub>Bx</sub> supply undervoltage negative going input threshold	V <sub>ddUV-</sub> V <sub>BxUV-</sub>			-	10.4	10.9	11.4	V
V <sub>dd</sub> and V <sub>Bx</sub> supply undervoltage I <sub>lockout</sub> hysteresis	V <sub>ddUVH</sub> V <sub>BxUVH</sub>			-	-	0.2	-	V
FAULT terminal sink current	I <sub>OSD</sub>	V <sub>FAULT</sub> =0.1V		-	1	1.5	-	mA
FAULT clearance delay time	FL <sub>TCLR</sub>	From time fault condition clear		-	1.3	1.65	2.5	ms
Switching character								
Switching time	t <sub>ON</sub>	I <sub>o</sub> =50A, Inductive load		Fig.6	-	0.7	1.5	μs
	t <sub>OFF</sub>				-	1.1	2.1	μs
Turn-on switching loss	E <sub>on</sub>	I <sub>o</sub> =50A, V <sub>CC</sub> =300V, V <sub>D</sub> =15V, L=280μH			-	1870	-	μJ
Turn-off switching loss	E <sub>off</sub>				-	1870	-	μJ
Total switching loss	E <sub>tot</sub>				-	3740	-	μJ
Turn-on switching loss	E <sub>on</sub>	I <sub>o</sub> =25A, V <sub>CC</sub> =300V, V <sub>D</sub> =15V, L=280μH, T <sub>c</sub> =100°C			-	1075	-	μJ
Turn-off switching loss	E <sub>off</sub>				-	1300	-	μJ
Total switching loss	E <sub>tot</sub>				-	2375	-	μJ
Diode reverse recovery energy	E <sub>rec</sub>	I <sub>o</sub> =25A, V <sub>CC</sub> =300V, V <sub>D</sub> =15V, L=280μH, T <sub>c</sub> =100°C		-	-	135	-	μJ
Diode reverse recovery time	t <sub>rr</sub>				-	135	-	ns
Reverse bias safe operating area	R <sub>BSOA</sub>	I <sub>o</sub> = 76A, V <sub>CE</sub> =450V		-	Full square			-
Short circuit safe operating area	S <sub>CSOA</sub>	V <sub>CE</sub> =400V, T <sub>c</sub> =100°C		-	4	-	-	μs
Current output signal level	I <sub>SO</sub>	I <sub>o</sub> =50A		-	0.427	0.45	0.474	V

Reference voltage is VSS terminal voltage unless otherwise specified.

\*1: The lower side's VCE(sat) and VF include a loss by the shunt resistance.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## Notes

1. When the internal protection circuit operates, a Fault signal is turned ON (When the Fault terminal is low level, Fault signal is ON state : output form is open DRAIN) but the Fault signal does not latch. After protection operation ends, it returns automatically within about 18ms to 80ms and resumes operation beginning condition. So, after Fault signal detection, set all input signals to OFF (Low) at once. However, the operation of pre-drive power supply low voltage protection (UVLO: with hysteresis about 0.2V) is as follows.

Upper side:

The gate is turned off and will return to regular operation when recovering to the normal voltage, but the latch will continue till the input signal will turn 'low'.

Lower side:

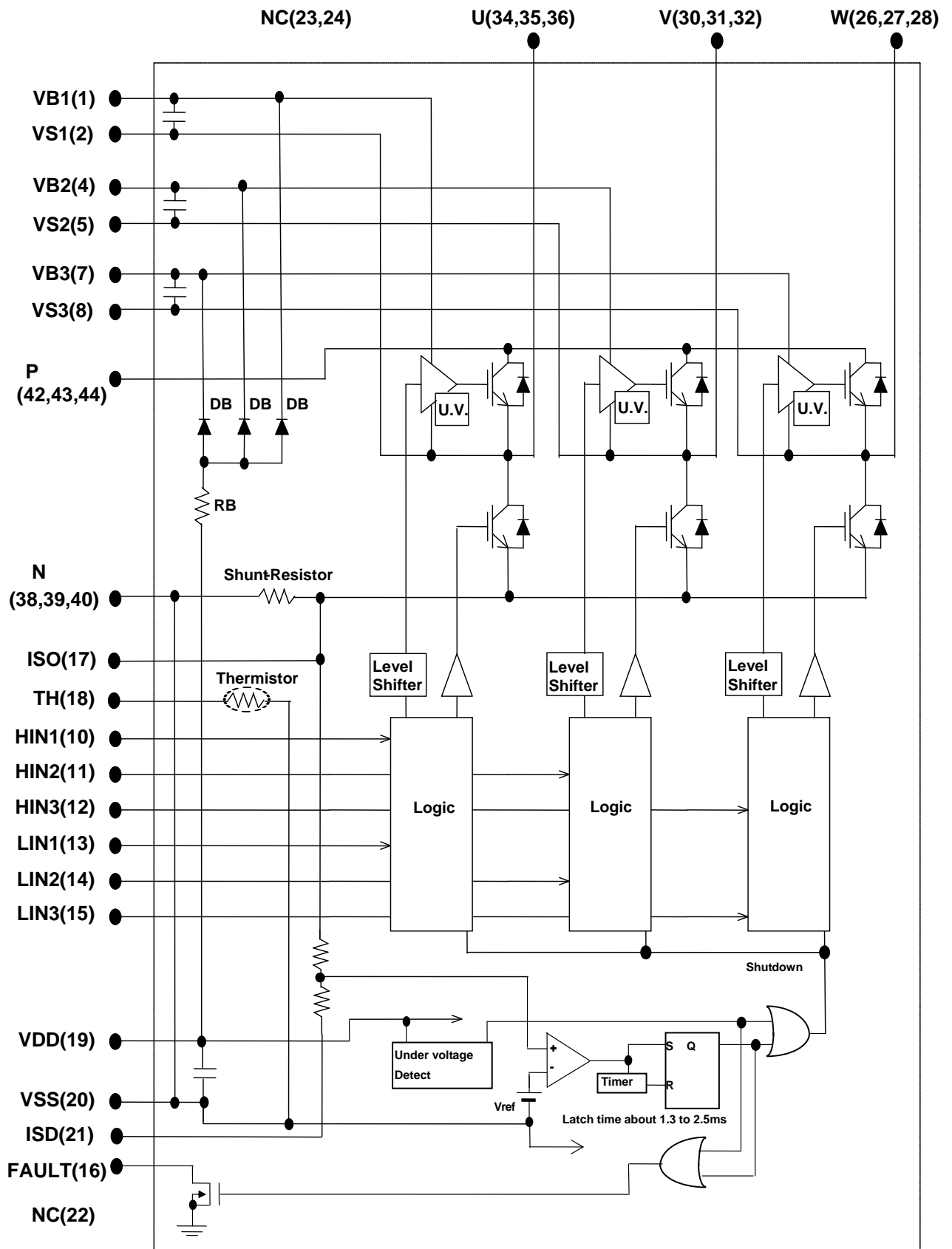
The gate is turned off and will automatically reset when recovering to normal voltage. It does not depend on input signal voltage.

2. When assembling the IPM on the heat sink with M4 type screw, tightening torque range is 0.79 Nm to 1.17 Nm.
3. The pre-drive low voltage protection is the feature to protect devices when the pre-driver supply voltage falls due to an operating malfunction.

## Pin Assignment

Pin No.	Name	Description	Pin No.	Name	Description
1	VB1	High side floating supply voltage 1	44	P	Positive bus input voltage
2	VS1	High side floating supply offset voltage	43	P	Positive bus input voltage
3	-	Without pin	42	P	Positive bus input voltage
4	VB2	High side floating supply voltage 2	41	-	Without pin
5	VS2	High side floating supply offset voltage	40	N	Negative bus input voltage
6	-	Without pin	39	N	Negative bus input voltage
7	VB3	High side floating supply voltage 3	38	N	Negative bus input voltage
8	VS3	High side floating supply offset voltage	37	-	Without pin
9	-	Without pin	36	U	U-phase output
10	HIN1	Logic input high side driver-Phase1	35	U	U-phase output
11	HIN2	Logic input high side driver-Phase2	34	U	U-phase output
12	HIN3	Logic input high side driver-Phase3	33	-	Without pin
13	LIN1	Logic input low side driver-Phase1	32	V	V-phase output
14	LIN2	Logic input low side driver-Phase2	31	V	V-phase output
15	LIN3	Logic input low side driver-Phase3	30	V	V-phase output
16	FAULT	Fault out (open drain)	29	-	Without pin
17	ISO	Current monitor pin	28	W	W-phase output
18	TH	Thermistor out	27	W	W-phase output
19	VDD	+15V main supply	26	W	W-phase output
20	VSS	Negative main supply	25	-	Without pin
21	ISD	Over-current protection level setting pin	24	NC	-
22	NC	-	23	NC	-

# Block Diagram



## Test Circuit

(The tested phase: U+ shows the upper side of the U phase and U- shows the lower side of the U phase.)

### ■ $I_{CE}$ / $I_R(BD)$

	U+	V+	W+	U-	V-	W-
M	42	42	42	34	30	26
N	34	30	26	38	38	38

	U(BD)	V(BD)	W(BD)
M	1	4	7
N	20	20	20

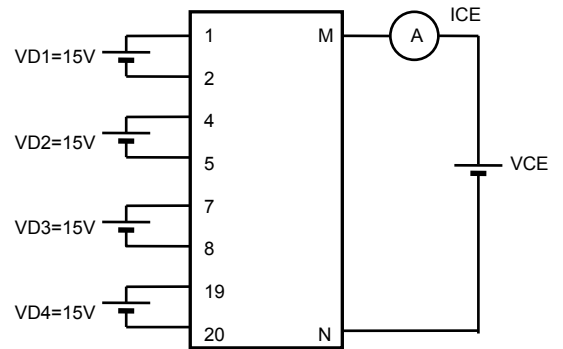


Fig.1

### ■ $V_{CE(SAT)}$ (Test by pulse)

	U+	V+	W+	U-	V-	W-
M	42	42	42	34	30	26
N	34	30	26	17	19	21
m	10	11	12	13	14	15

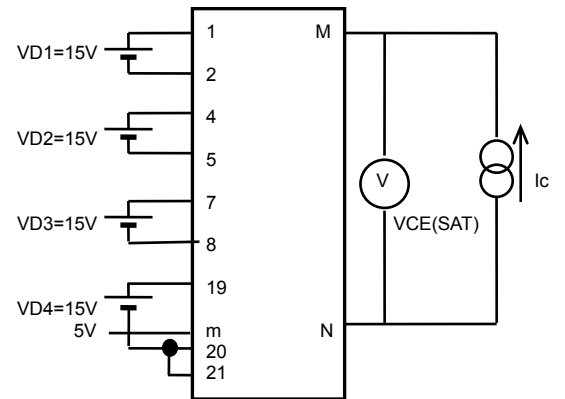


Fig.2

### ■ $V_F$ (Test by pulse)

	U+	V+	W+	U-	V-	W-
M	42	42	42	34	30	26
N	34	30	26	38	38	38

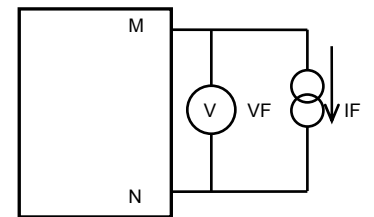


Fig.3

### ■ $I_D$

	VD1	VD2	VD3	VD4
M	1	4	7	19
N	2	5	8	20

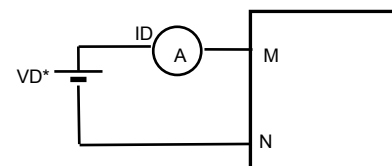


Fig.4

■ ISD

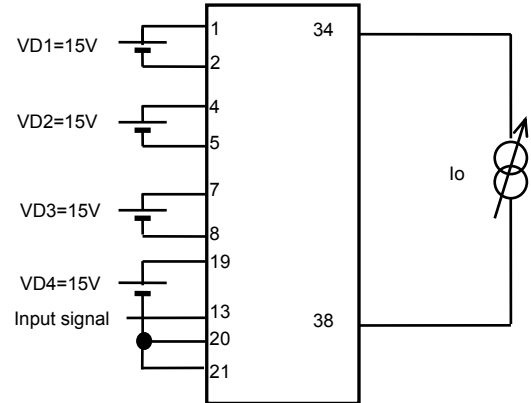
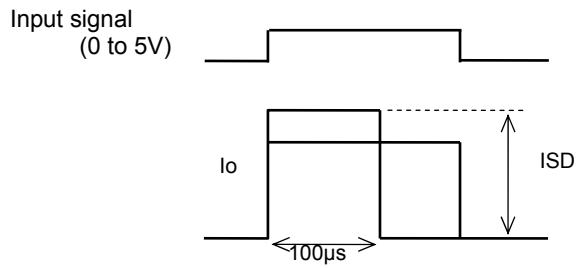


Fig.5

■ Switching time (The circuit is a representative example of the lower side U phase.)

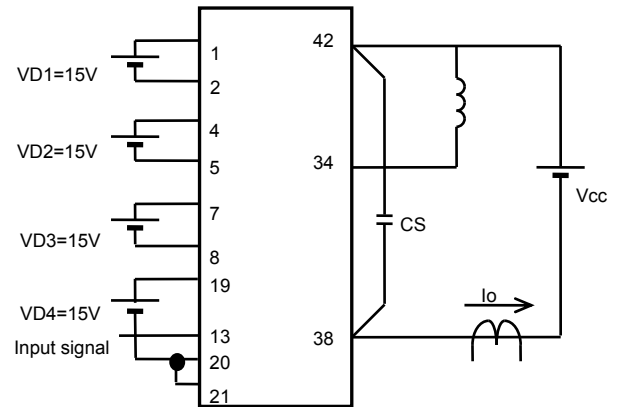
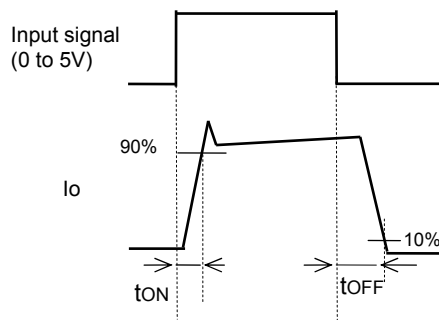


Fig.6

■ RB-SOA (The circuit is a representative example of the lower side U phase.)

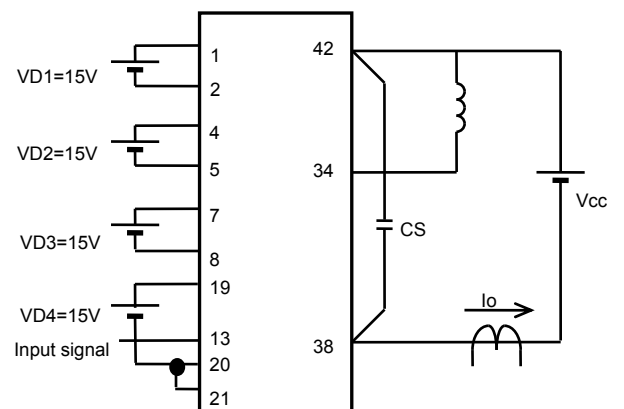
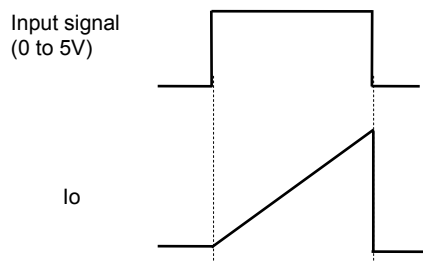


Fig.7

# Logic Timing Chart

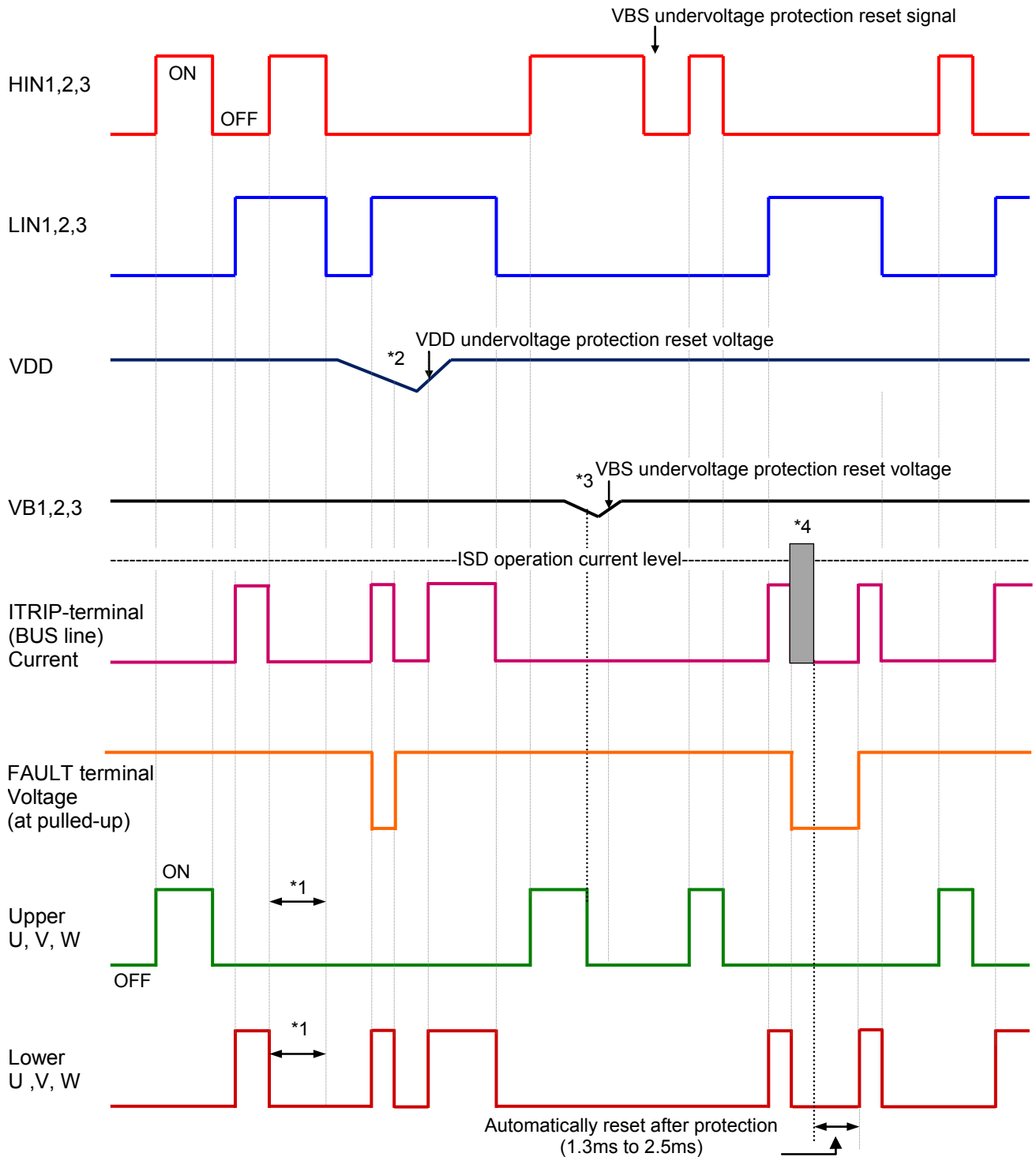


Fig. 8

## Notes

- \*1 : Diagram shows the prevention of shoot-through via control logic. More dead time to account for switching delay needs to be added externally.
- \*2 : When V<sub>DD</sub> decreases all gate output signals will go low and cut off all of 6 IGBT outputs. part. When V<sub>DD</sub> rises the operation will resume immediately.
- \*3 : When the upper side gate voltage at VB1, VB2 and VB3 drops only, the corresponding upper side output is turned off. The outputs return to normal operation immediately after the upper side gat voltage rises.
- \*4 : In case of over current detection, all IGBT's are turned off and the FAULT output is asserted. Normal operation resumes in 1.3 to 2.5ms after the over current condition is removed.

Logic level table

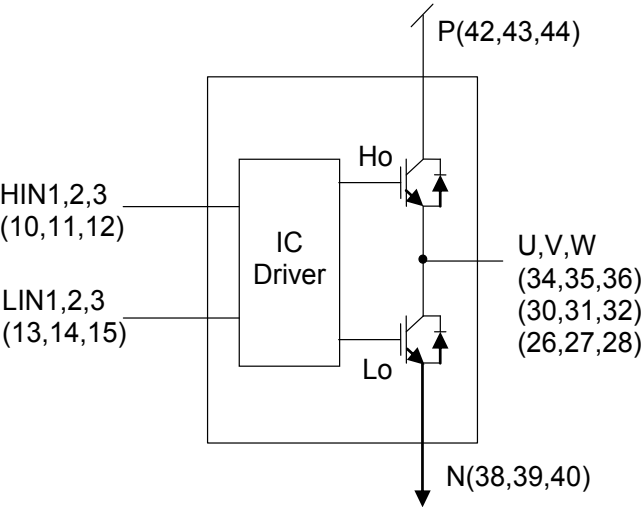


Fig.9

INPUT			OUTPUT			
HIN	LIN	OCP	Ho	Lo	U,V,W	FAULT
H	L	OFF	H	L	P	OFF
L	H	OFF	L	H	N	OFF
L	L	OFF	L	L	High Impedance	OFF
H	H	OFF	L	L	High Impedance	OFF
X	X	ON	L	L	High Impedance	ON

# Application Circuit Example

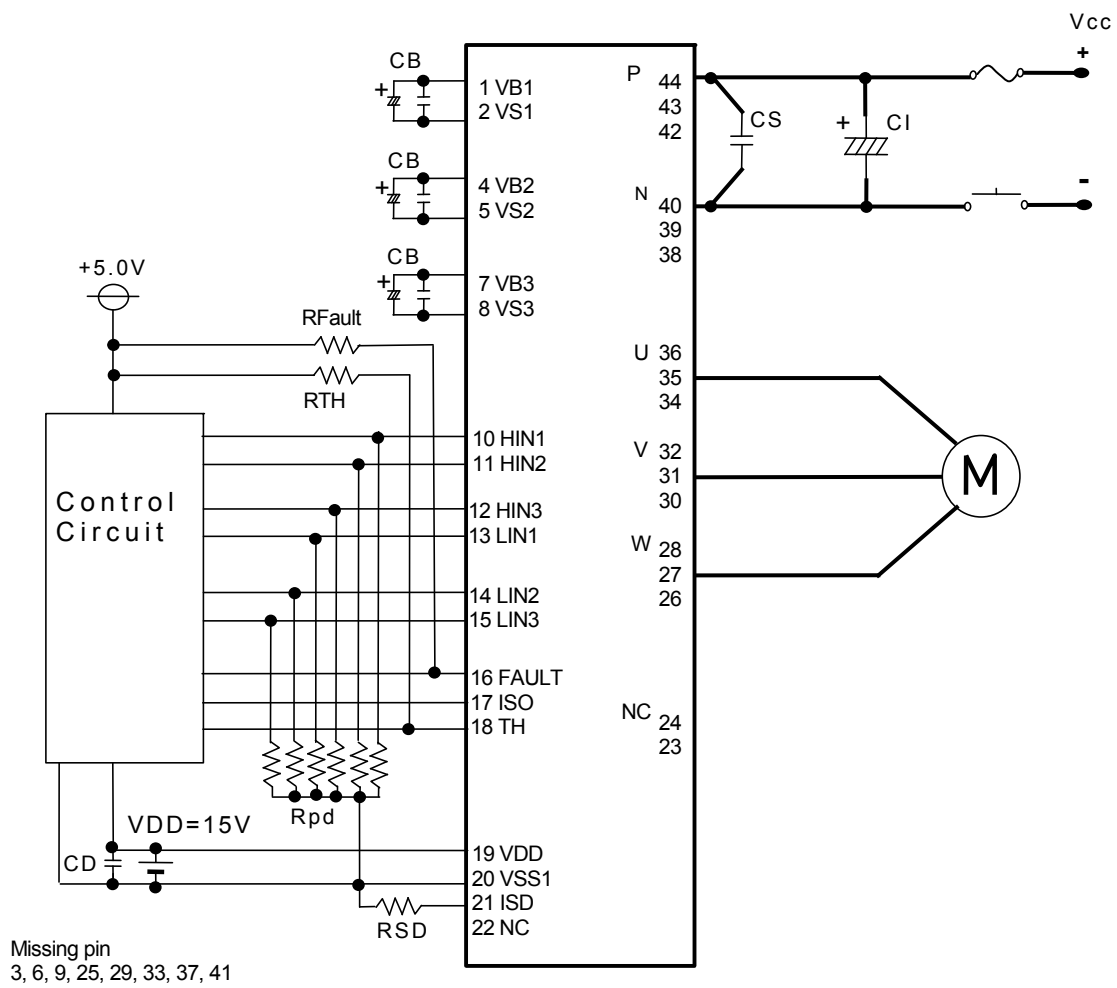


Fig.10

## Recommended Operating Conditions at T<sub>c</sub> = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ	Max	
Supply voltage	VCC	P to N	0	280	450	V
Pre-driver supply voltage	VD1,2,3	VB1 to VS1, VB2 to VS2, VB3 to VS3	12.5	15	17.5	V
	VD4	V <sub>DD</sub> to V <sub>SS</sub> *1	13.5	15	16.5	
Input ON voltage	VIN(ON)	HIN1,HIN2,HIN3, LIN1,LIN2,LIN3	3.0	-	5.0	V
Input OFF voltage	VIN(OFF)		0	-	0.8	
PWM frequency	fPWM		1	-	20	kHz
Dead time	DT	Turn-off to turn-on (external)	2	-	-	μs
Allowable input pulse width	PWIN	ON pulse width/OFF pulse width	1	-	-	μs
Tightening torque	MT	'M4' type screw	0.79	-	1.17	Nm

\*1 Pre-driver power supply (VD4=15±1.5V) must have the capacity of I<sub>o</sub>=20mA (DC), 0.5A (Peak).

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## Usage Precautions

1. This IPM includes bootstrap diode and resistors. Therefore, by adding a capacitor “CB”, a high side drive voltage is generated; each phase requires an individual bootstrap capacitor. The recommended value of CB is in the range of 1 to 47μF, however this value needs to be verified prior to production. If selecting the capacitance more than 47μF (±20%), connect a resistor (about 20Ω) in series between each 3-phase upper side power supply terminals (VB1,2,3) and each bootstrap capacitor. When not using the bootstrap circuit, each upper side pre-drive power supply requires an external independent power supply.
2. It is essential that wiring length between terminals in the snubber circuit be kept as short as possible to reduce the effect of surge voltages. Recommended value of “CS” is in the range of 0.1 to 10μF.
3. “ISO” (pin17) is terminal for current monitor.
4. “FAULT” (pin16) is open DRAIN output terminal. (Active Low). Pull up resistor is recommended more than 5.6kΩ.
5. Inside the IPM, a thermistor used as the temperature monitor for internal substrate is connected between V<sub>SS</sub> terminal and TH terminal, therefore, an external pull up resistor connected between the TH terminal and an external power supply should be used. The temperature monitor example application is as follows, please refer the Fig.11, and Fig.12 below.
6. The pull down resistor of 33kΩ is provided internally at the signal input terminals. An external resistor of 2.2k to 3.3kΩ should be added to reduce the influence of external wiring noise.
7. The over-current protection feature is not intended to protect in exceptional fault condition. An external fuse is recommended for safety.
8. When “N” and “V<sub>SS</sub>” terminal are short-circuited on the outside, level that over-current protection (ISD) might be changed from designed value as IPM. Please check it in your set (“N” terminal and “V<sub>SS</sub>” terminal are connected in IPM).
9. The over-current protection function operates normally when an external resistor RSD is connected between ISD and V<sub>SS</sub> terminals. Be sure to connect this resistor. The level of the overcurrent protection can be changed according to the RSD value.
10. When input pulse width is less than 1.0μs, an output may not react to the pulse. (Both ON signal and OFF signal)

This data shows the example of the application circuit, does not guarantee a design as the mass production set.

## The characteristic of thermistor

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Resistance	$R_{25}$	$T_c=25^{\circ}\text{C}$	97	100	103	$\text{k}\Omega$
Resistance	$R_{100}$	$T_c=100^{\circ}\text{C}$	4.93	5.38	5.88	$\text{k}\Omega$
B-Constant( $25\text{-}50^{\circ}\text{C}$ )	B		4165	4250	4335	K
Temperature Range			-40		+125	$^{\circ}\text{C}$

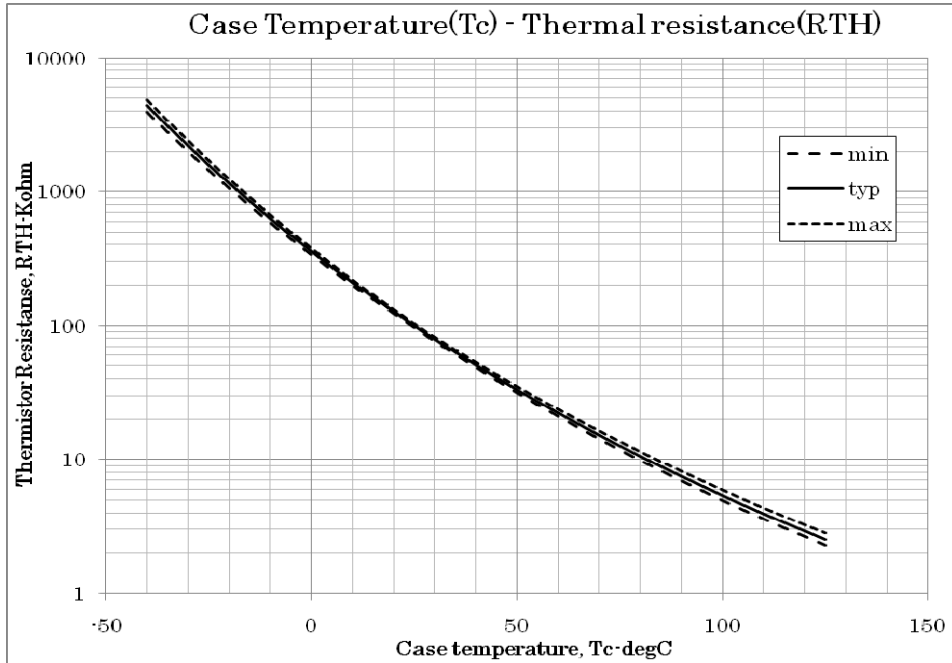


Fig.11 Variation of thermistor resistance with temperature

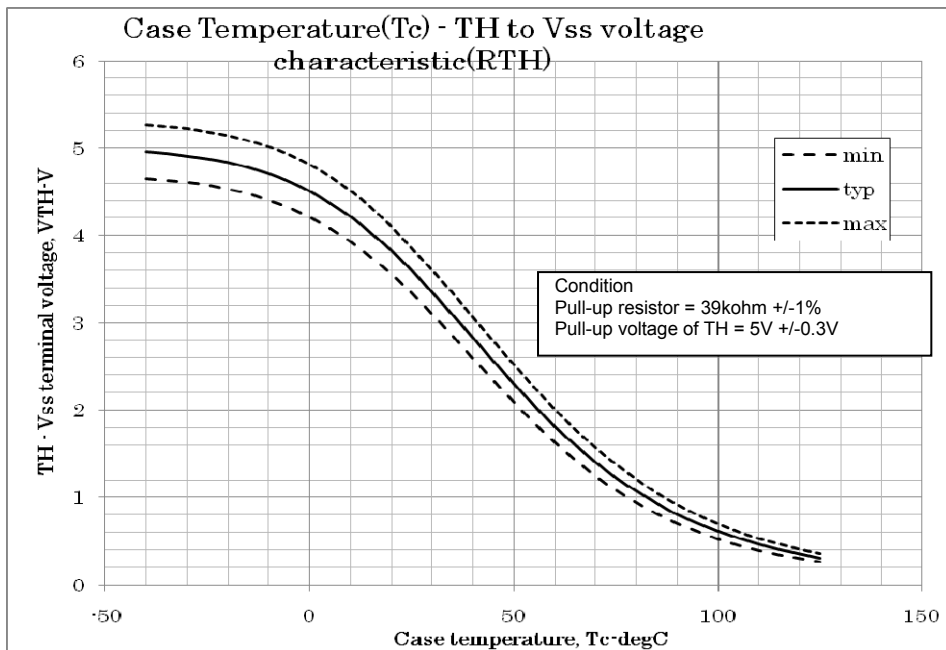


Fig.12 Variation of temperature sense voltage with thermistor temperature

## Maximum Phase current

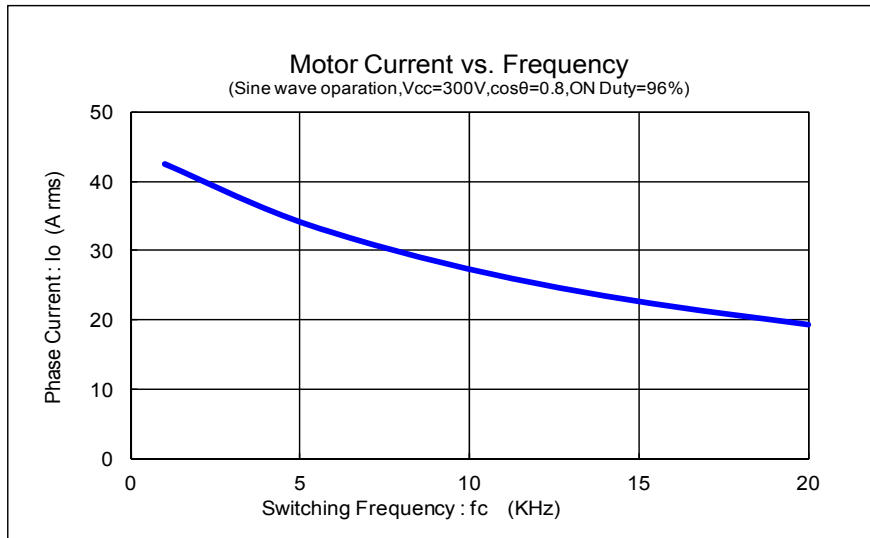


Fig.13 Maximum sinusoidal phase current as function of switching frequency at  $T_c=100^\circ C$ ,  $V_{CC}=300V$

## Switching waveform

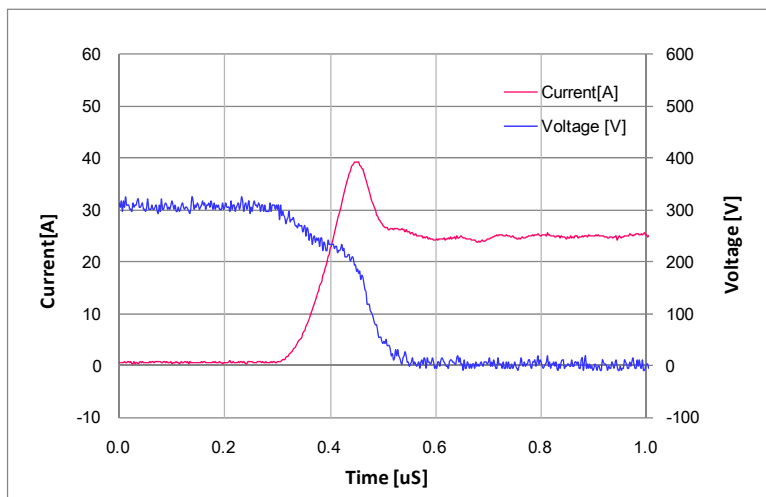


Fig. 14 IGBT Turn-on. Typical turn-on waveform at  $T_c=100^\circ C$ ,  $V_{CC}=300V$ ,  $I_c=25A$

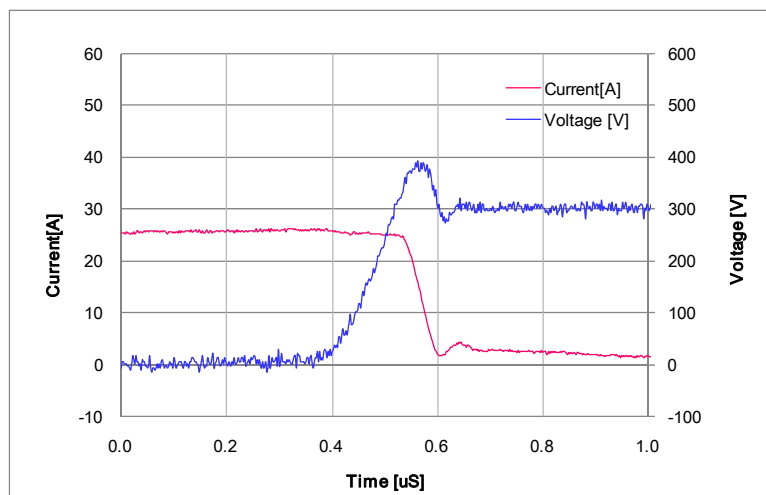


Fig. 15 IGBT Turn-off. Typical turn-off waveform  $T_c=100^\circ C$ ,  $V_{CC}=300V$ ,  $I_c=25A$

## CB capacitor value calculation for bootstrap circuit

### Calculate condition

Item	Symbol	Value	Unit
Upper side power supply	VBS	15	V
Total gate charge of output power IGBT at 15V.	Qg	0.47	μC
Upper side power supply low voltage protection.	UVLO	12	V
Upper side power dissipation.	IDmax	400	μA
ON time required for CB voltage to fall from 15V to UVLO	Ton-max	-	s

### Capacitance calculation formula

CB must not be discharged below to the upper limit of the UVLO - the maximum allowable on-time (Ton-max) of the upper side is calculated as follows:

$$VBS \times CB - Qg - IDmax \times Ton-max = UVLO \times CB$$

$$CB = (Qg + IDmax \times Ton-max) / (VD - UVLO)$$

The relationship between Ton-max and CB becomes as follows. CB is recommended to be approximately 3 times the value calculated above. The recommended value of CB is in the range of 1 to 47μF, however, the value needs to be verified prior to production.

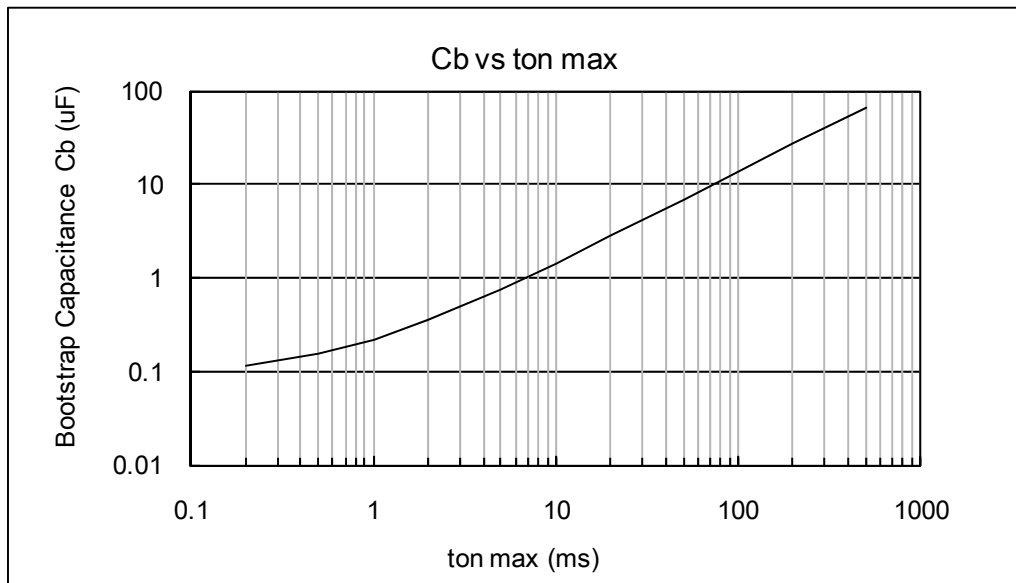


Fig.16 Ton-max vs CB characteristic

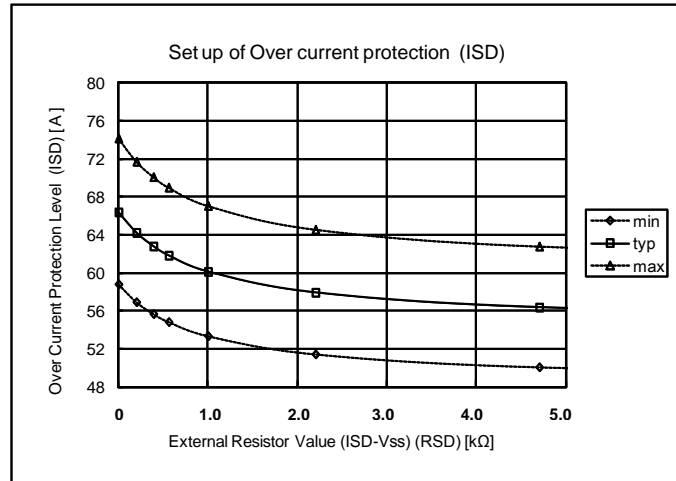
## ISD terminal

The over-current protection function operates normally when an external resistor RSD is connected between ISD and VSS terminals. Be sure to connect this resistor.

The OCP trip level is programmed within the default or lower levels by an external resistor (RSD) between the ISD and VSD pins. When the default level is used both terminals must be shorted e.g. by a  $0\Omega$  resistor.

## RSD values and resulting ISD curve

External Resistance (RSD) [k $\Omega$ ]	Over Current Protection (ISD) [A]		
	min	typ	max
0.0	58.8	66.4	74.2
0.2	57.0	64.3	71.7
0.39	55.7	62.8	70.1
0.56	54.9	61.9	69.0
1.0	53.4	60.1	67.1
2.2	51.5	57.9	64.6
4.7	50.1	56.4	62.8
10.0	49.3	55.4	61.7
Open	48.4	54.4	60.6



## Package Dimensions

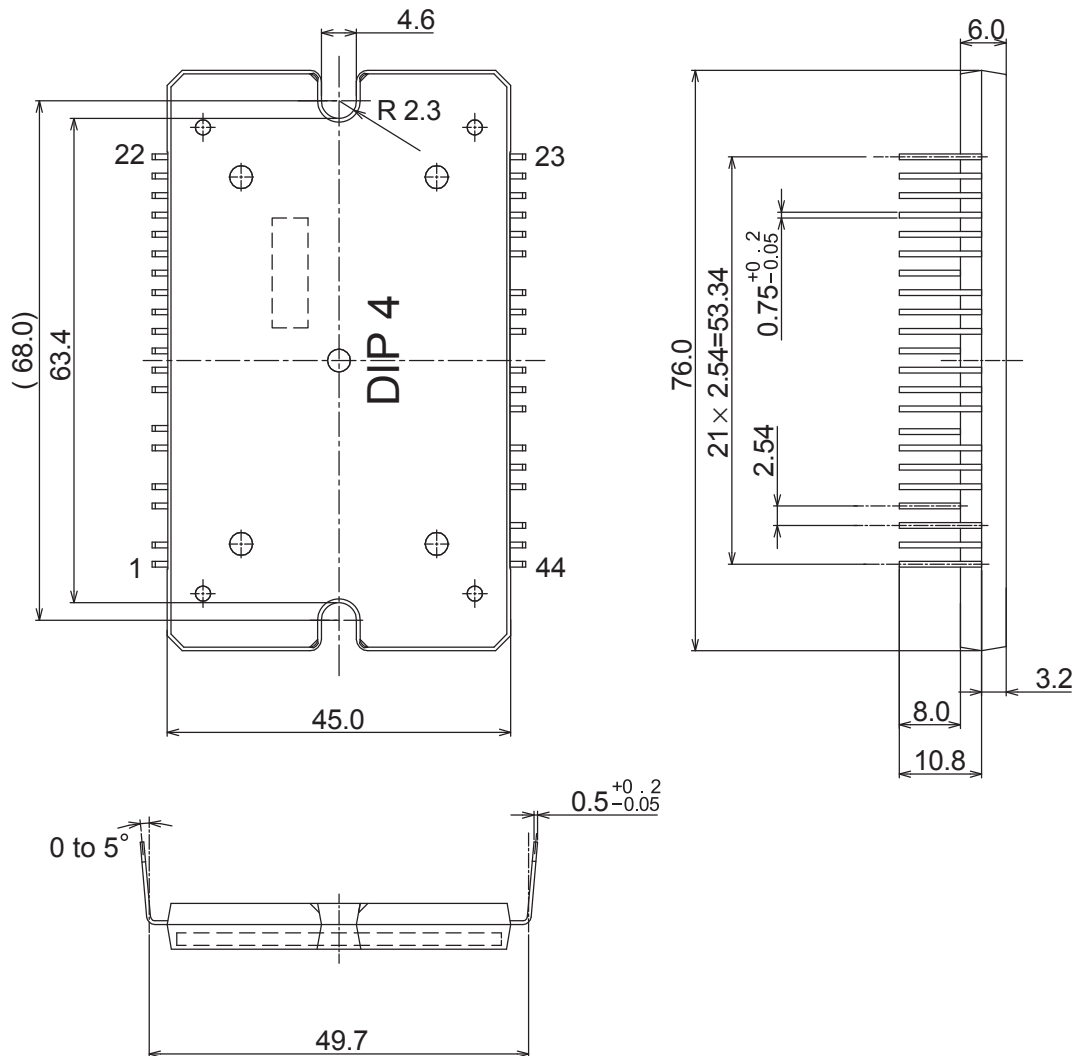
unit : mm

### HYBRID INTEGRATED MODULE

CASE MODAW

ISSUE 0

Missing Pin : 3, 6, 9, 29, 33, 37, 41



## ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
STK5F1U3E3D-E	MODAW, 610AC-DIP4-UL (Pb-Free)	6 / Tube

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