Low Skew, 1-to-18 LVPECL-to-LVCMOS/LVTTL Fanout Buffer

ICS83940

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General Description

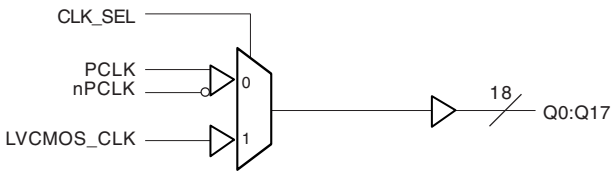
The ICS83940 is a low skew, 1-to-18 LVPECL-to-LVCMOS/LVTTL Fanout Buffer. The ICS83940 has twoselectable clock inputs. The PCLK, nPCLK pair can accept LVPECL, CML, or SSTL input levels. The LVCMOS_CLK can accept LVCMOS or LVTTL input levels. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines.

The ICS83940 is characterized at full 3.3V, full 2.5V and mixed 3.3V input and 2.5V output operating supply modes. Guaranteed output and part-to-part skew characteristics make the ICS83940 ideal for those clock distribution applications demanding well defined performance and repeatability.

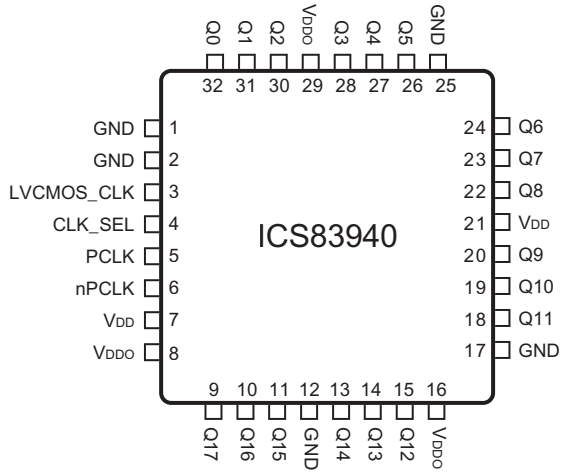
Features

- Eighteen LVCMOS/LVTTL outputs, 16Ω typical output impedance
- Selectable LVCMOS_CLK or LVPECL clock inputs
- PCLK, nPCLK supports the following input types: LVPECL, CML, SSTL
- LVCMOS_CLK accepts the following input levels: LVCMOS or LVTTL
- Maximum output frequency: 250MHz
- Output skew: 150ps (maximum)
- Part to part skew: 750ps (maximum)
- Full 3.3V or 2.5V supply modes
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Lead-Free package fully RoHS compliant
- For New Designs Use: 83940DYLF or 83940DYILF

Block Diagram



Pin Assignment



32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Pacakge
Top View

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TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2, 12, 17, 25	GND	Power		Power supply ground.
3	LVCMOS_CLK	Input	Pulldown	Clock input. LVCMOS / LVTTL interface levels.
4	CLK_SEL	Input	Pulldown	Clock select input. Selects LVCMOS / LVTTL clock input when HIGH. Selects PCLK, nPCLK inputs when LOW. LVCMOS / LVTTL interface levels.
5	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
6	nPCLK	Input	Pullup	Inverting differential LVPECL clock input.
7, 21	V_{DD}	Power		Core supply pins.
8, 16, 29	V_{DDO}	Power		Output supply pins.
9, 10, 11, 13, 14, 15, 18, 19, 20, 22, 23, 24, 26, 27, 28, 30, 31, 32	Q17, Q16, Q15, Q14, Q13, Q12, Q11, Q10, Q9, Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Output		Clock outputs. 16Ω typical output impedance. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldow*n refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDO} = 3.47		13		pF
		V_{DD}, V_{DDO} = 2.625		11		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
R_{OUT}	Output Impedance		11	16	21	Ω

TABLE 3A. CLOCK SELECT FUNCTION TABLE

Control Input	Clock	
CLK_SEL	PCLK, nPCLK	LVCMOS_CLK
0	Selected	De-selected
1	De-selected	Selected

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs				Outputs	Input to Output Mode	Polarity
CLK_SEL	LVCMOS_CLK	PCLK	nPCLK	Q0:Q17		
0	—	0	1	LOW	Differential to Single Ended	Non Inverting
0	—	1	0	HIGH	Differential to Single Ended	Non Inverting
0	—	0	Biased; NOTE 1	LOW	Single Ended to Single Ended	Non Inverting
0	—	1	Biased; NOTE 1	HIGH	Single Ended to Single Ended	Non Inverting
0	—	Biased; NOTE 1	0	HIGH	Single Ended to Single Ended	Inverting
0	—	Biased; NOTE 1	1	LOW	Single Ended to Single Ended	Inverting
1	0	—	—	LOW	Single Ended to Single Ended	Non Inverting
1	1	—	—	HIGH	Single Ended to Single Ended	Non Inverting

NOTE 1: Please refer to the Application Information section. "Wiring the Differential Input to Accept Single Ended Levels".

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Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°$ to $70°$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				25	mA
I_{DDO}	Output Supply Current				25	mA

Table 4B. DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°$ to $70°$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	LVCMOS_CLK		2.4		V_{DD}	V
V_{IL}	Input Low Voltage	LVCMOS_CLK				0.8	V
V_{PP}	Peak-to-Peak Input Voltage	PCLK, nPCLK		300			mV
V_{CMR}	Input Common Mode Voltage; NOTE 1, 2	PCLK, nPCLK		GND + 1.5		V_{DD}	V
I_{IN}	Input Current					±200	µA
V_{OH}	Output High Voltage		I_{OH} = -20mA	2.4			V
V_{OL}	Output Low Voltage		I_{OL} = 20mA			0.5	V

NOTE 1: For single ended applications, the maximum input voltage for PCLK, nPCLK is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

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TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°$ TO $70°$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					250	MHz
t_{pLH}	Propagation Delay;	PCLK, nPCLK; NOTE 1, 5	f ≤ 150MHz	2		3.4	ns
		LVCMOS_CLK; NOTE 2, 5	f ≤ 150MHz	2.6		3.8	ns
t_{pLH}	Propagation Delay;	PCLK, nPCLK; NOTE 1, 5	f > 150MHz	2		3.7	ns
		LVCMOS_CLK; NOTE 2, 5	f > 150MHz	2.6		4	ns
*t*sk(o)	Output Skew; NOTE 3, 5	PCLK, nPCLK	Measured on rising edge @$V_{DDO}/2$			150	ps
		LVCMOS_CLK				150	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 6	PCLK, nPCLK	f < 150MHz			1.4	ns
		LVCMOS_CLK	f < 150MHz			1.2	ns
*t*sk(pp)	Part-to-Part Skew; NOTE 6	PCLK, nPCLK	f > 150MHz			1.7	ns
		LVCMOS_CLK	f > 150MHz			1.4	ns
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 5	PCLK, nPCLK	Measured on rising edge @$V_{DDO}/2$			850	ps
		LVCMOS_CLK				750	ps
t_R	Output Rise Time		0.5 to 2.4V	0.3		1.2	ns
t_F	Output Fall Time		0.5 to 2.4V	0.3		1.2	ns
odc	Output Duty Cycle		f < 134MHz	45	50	55	%

All parameters measured at 200MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output $V_{DDO}/2$.
NOTE 2: Measured from $V_{DD}/2$ to $V_{DDO}/2$.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages, same temperature, and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 6: Defined as skew between outputs on different devices, across temperature and voltage ranges, and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.

TABLE 4C. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°$ TO $70°$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				25	mA
I_{DDO}	Output Supply Current				25	mA

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TABLE 4D. DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°$ TO $70°$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	LVCMOS_CLK		2		V_{DD}	V
V_{IL}	Input Low Voltage	LVCMOS_CLK				0.8	V
V_{PP}	Peak-to-Peak Input Voltage	PCLK, nPCLK		300			mV
V_{CMR}	Input Common Mode Voltage; NOTE 1, 2	PCLK, nPCLK		GND + 1.5		V_{DD}	V
I_{IN}	Input Current					±200	µA
V_{OH}	Output High Voltage		I_{OH} = -12mA	1.8			V
V_{OL}	Output Low Voltage		I_{OL} = 12mA			0.5	V

NOTE 1: For single ended applications, the maximum input voltage for PCLK, nPCLK is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°$ TO $70°$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					200	MHz
t_{pLH}	Propagation Delay;	PCLK, nPCLK; NOTE 1, 5	f ≤ 150MHz	2		4.6	ns
		LVCMOS_CLK; NOTE 2, 5	f ≤ 150MHz	2.7		4.4	ns
t_{pLH}	Propagation Delay;	PCLK, nPCLK; NOTE 1, 5	f > 150MHz	2.2		4.4	ns
		LVCMOS_CLK; NOTE 2, 5	f > 150MHz	2.7		4.4	ns
*t*sk(o)	Output Skew; NOTE 3, 5	PCLK, nPCLK	Measured on rising edge @V_{DDO}/2			200	ps
		LVCMOS_CLK				200	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 6	PCLK, nPCLK	f < 150MHz			2.6	ns
		LVCMOS_CLK	f < 150MHz			1.7	ns
*t*sk(pp)	Part-to-Part Skew; NOTE 6	PCLK, nPCLK	f > 150MHz			2.2	ns
		LVCMOS_CLK	f > 150MHz			1.7	ns
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 5	PCLK, nPCLK	Measured on rising edge @V_{DDO}/2			1.2	ns
		LVCMOS_CLK				1.0	ns
t_R	Output Rise Time		0.5 to 1.8V	0.3		1.2	ns
t_F	Output Fall Time		0.5 to 1.8V	0.3		1.2	ns
odc	Output Duty Cycle		f < 134MHz	45		55	%

All parameters measured at 200MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output V_{DDO}/2.
NOTE 2: Measured from V_{DD}/2 to V_{DDO}/2.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages, same temperature, and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 6: Defined as skew between outputs on different devices, across temperature and voltage ranges, and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.

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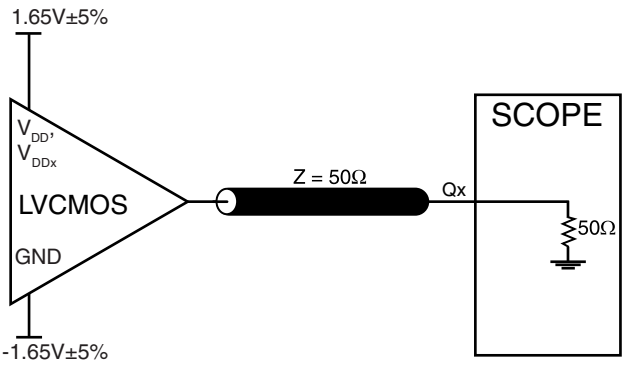
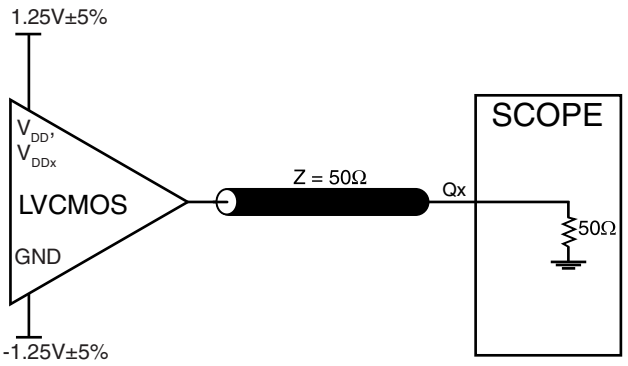
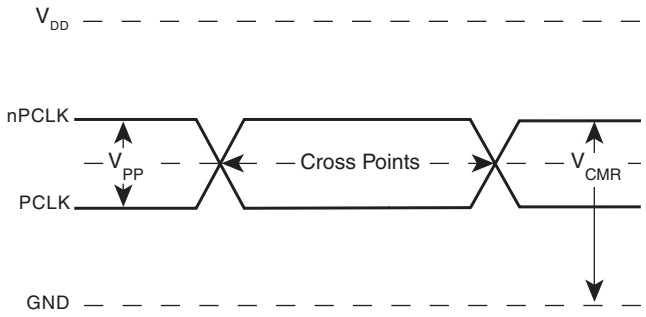
PARAMETER MEASUREMENT INFORMATION



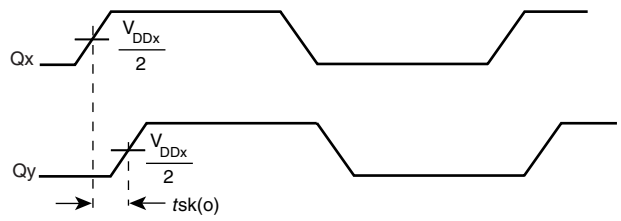
3.3V OUTPUT LOAD AC TEST CIRCUIT



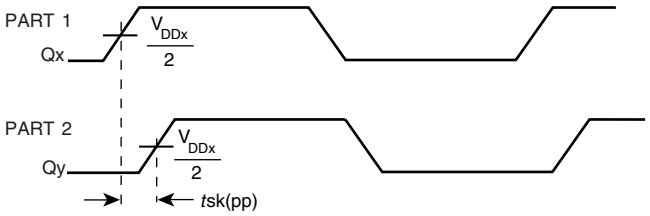
2.5V OUTPUT LOAD AC TEST CIRCUIT



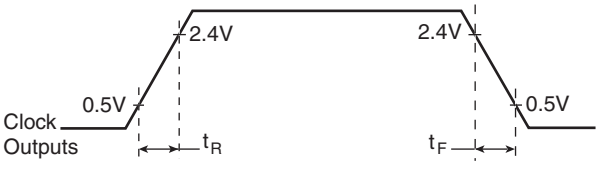
DIFFERENTIAL INPUT LEVEL



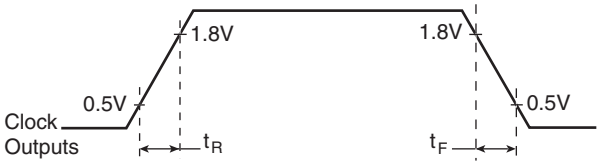
OUTPUT SKEW



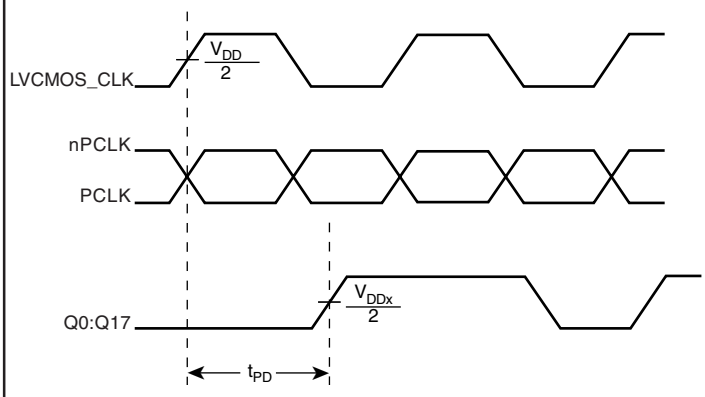
PART-TO-PART SKEW



3.3V OUTPUT RISE/FALL TIME



2.5V OUTPUT RISE/FALL TIME



PROPAGATION DELAY

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

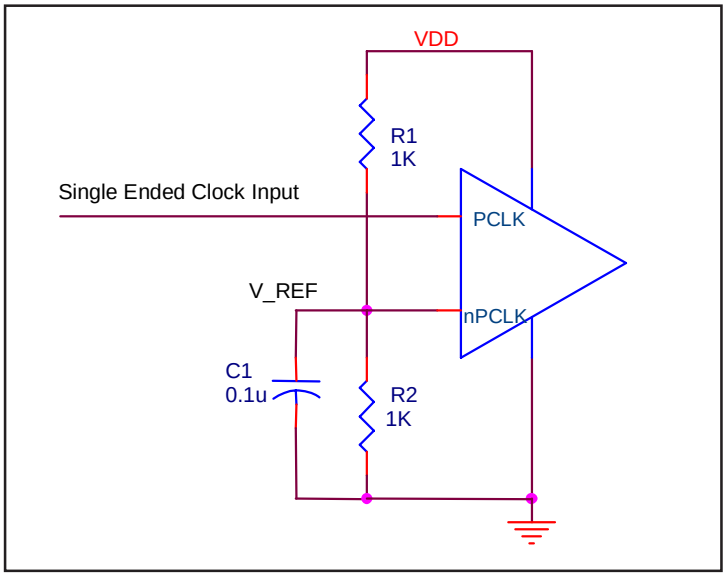


Figure 1. Single Ended Signal Driving Differential Input

LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

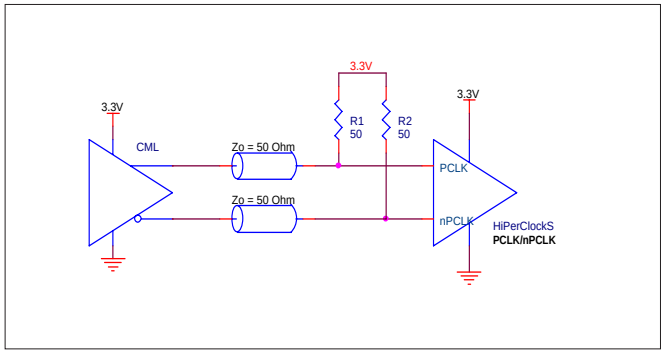


Figure 2A. PCLK/nPCLK Input Driven by a CML Driver

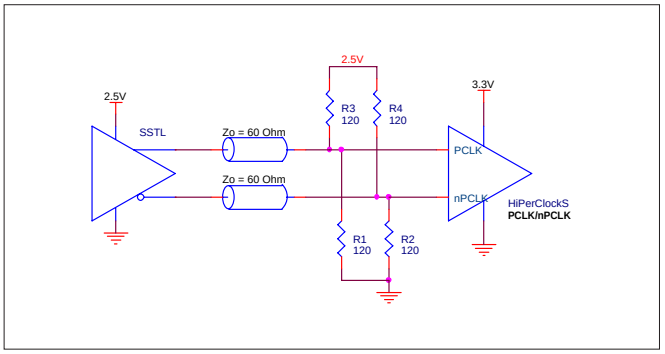


Figure 2B. PCLK/nPCLK Input Driven by an SSTL Driver

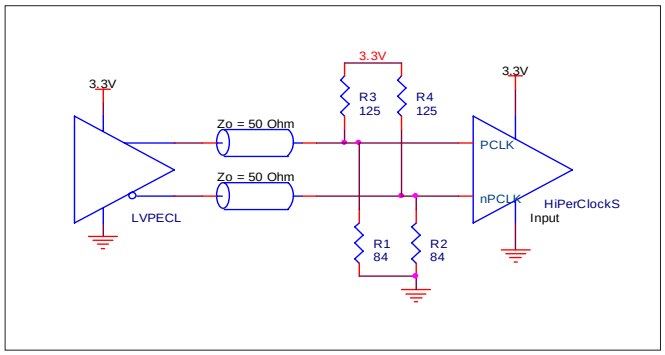


Figure 2C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

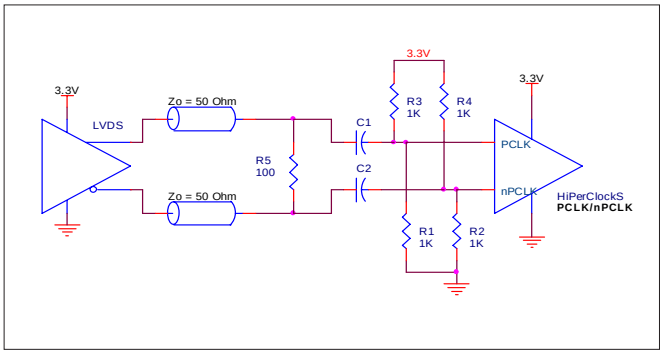


Figure 2D. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

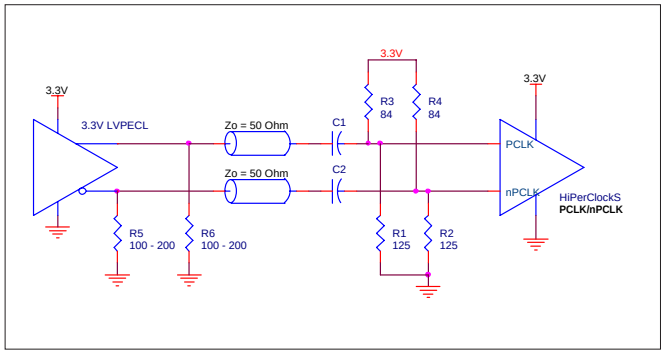


Figure 2E. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for 32 Lead LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for ICS83940 is: 820

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Package Outline - Y Suffix for 32 Lead LQFP

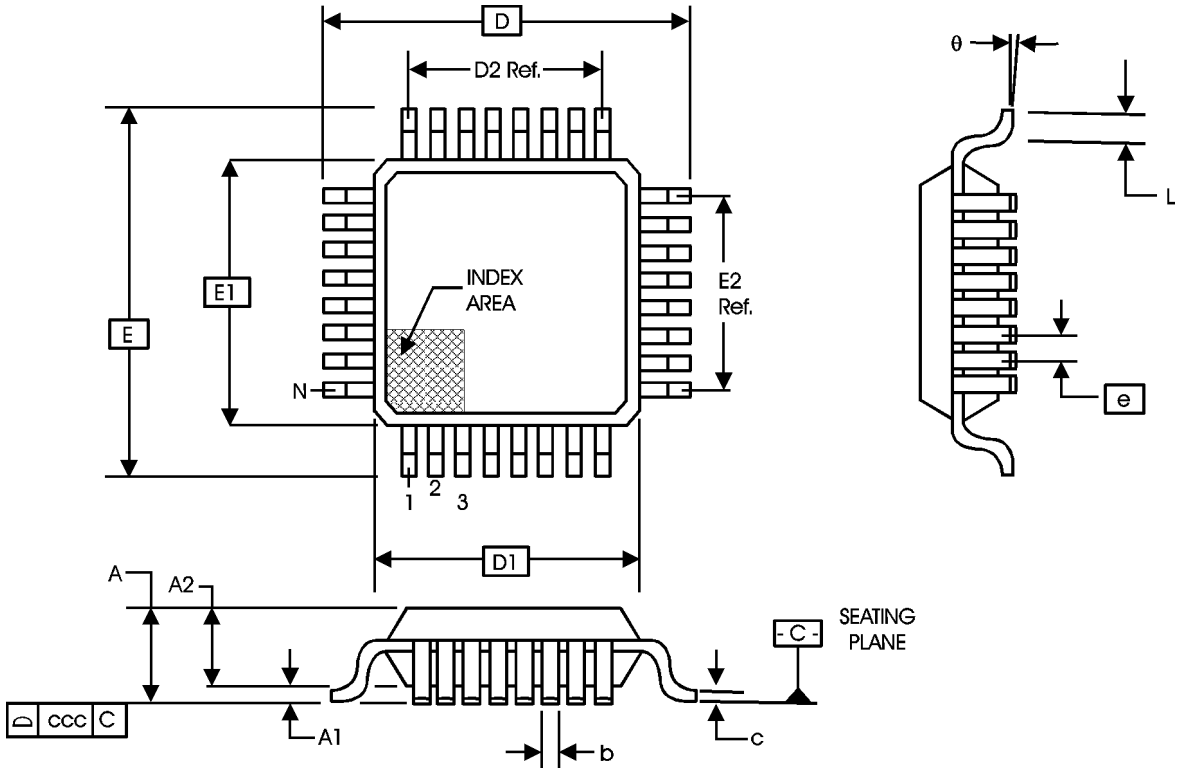

Table 7. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

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TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
83940BY	ICS83940BY	32 Lead LQFP	Tray	0°C to 70°C
83940BYT	ICS83940BY	32 Lead LQFP	1000 Tape & Reel	0°C to 70°C
83940BYLF	ICS83940BYLF	32 Lead "Lead-Free" LQFP	Tray	0°C to 70°C
83940BYLFT	ICS83940BYLF	32 Lead "Lead-Free" LQFP	1000 Tape & Reel	0°C to 70°C

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REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T2	2	CPD Value changed from 10pF to 13pF for 3.47V and added 11pF for 2.625V	4/25/02
A		1 2	In Features section, first bullet changed Output Impedance from 23Ω to 16Ω. T1 Pin Description, changed Q outputs description from 23Ω to 16Ω output impedanace.	5/23/02
A			Updated format.	12/12/02
A	T5A	4 7 8	3V AC Characteristics - corrected Part-to-Part Skew (f<150MHz) unit from ps to ns. Updated Single Ended Signal Driving Differential Input diagram. Added LVPECL Input Interface section.	3/17/04
A	T8	1 11	Features Section - added Lead-Free bullet. Ordering Information Table - added Lead-Free part number.	12/14/04
A	T8	11 13	Updated datasheet's header/footer with IDT from ICS. Removed "ICS" prefix from Part/Order Number column. Added Contact Page.	11/17/10
A		1	Not Recommended For New Designs For new designs use 83940D	5/21/13
B			Product Discontinuation Notice - Last time buy expires January 27, 2015, PDN# CQ-14-02	1/31/14

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