



# 700MHz, Low Jitter, Differential-to-3.3V LVPECL Frequency Synthesizer

ICS8430-111

PRELIMINARY DATA SHEET

## GENERAL DESCRIPTION

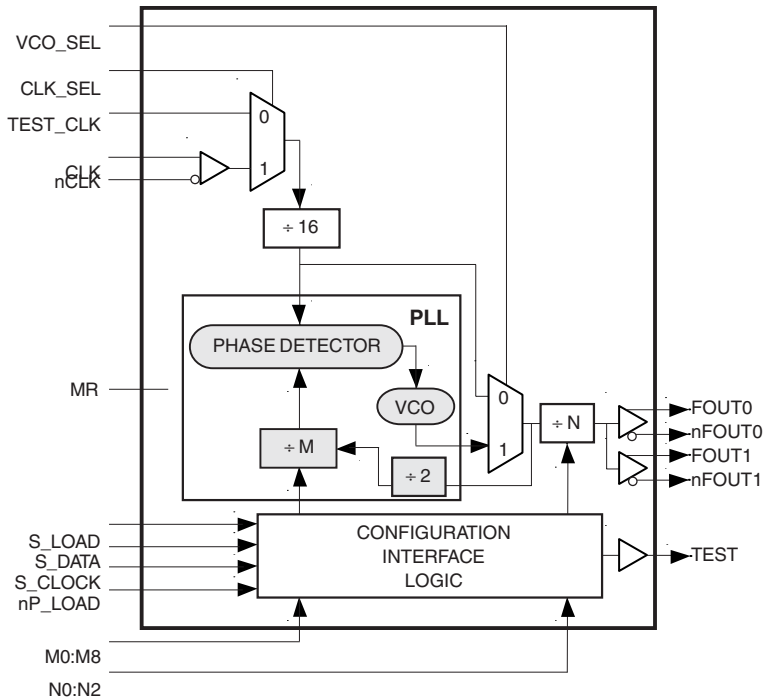


The ICS8430-111 is a general purpose, dual output high frequency synthesizer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The CLK, nCLK pair can accept most standard differential input levels. The single ended TEST\_CLK input accepts LVCMOS or LVTTTL input levels and translates them to 3.3V LVPECL levels. The VCO operates at a frequency range of 200MHz to 700MHz. With the output configured to divide the VCO frequency by 2, output frequency steps as small as 2MHz can be achieved using a 16MHz differential or single ended reference clock. Output frequencies up to 700MHz can be programmed using the serial or parallel interfaces to the configuration logic. The low jitter and frequency range of the ICS8430-111 makes it an ideal clock generator for most clock tree applications.

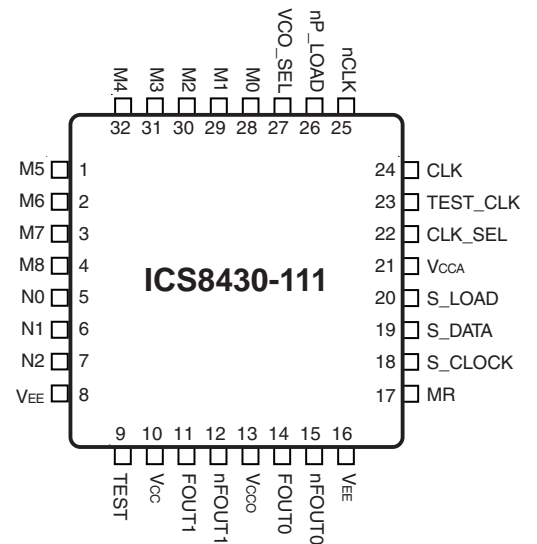
## FEATURES

- Dual differential 3.3V LVPECL output
- Selectable 14MHz to 27MHz differential CLK, nCLK or TEST\_CLK input
- CLK, nCLK accepts any differential input signal: LVPECL, LVHSTL, LVDS, SSTL, HCSL
- TEST\_CLK accepts the following input types: LVCMOS, LVTTTL
- Output frequency range up to 700MHz
- VCO range: 200MHz to 700MHz
- Parallel or serial interface for programming counter and output dividers
- Cycle-to-cycle jitter: 25ps (maximum)
- 3.3V supply voltage
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages
- Industrial temperature information available upon request

## BLOCK DIAGRAM



## PIN ASSIGNMENT



32-Lead LQFP

7mm x 7mm x 1.4mm package body

Y Package

Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

### FUNCTIONAL DESCRIPTION

The ICS8430-111 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A differential clock input is used as the input to the on-chip oscillator. The output of the oscillator is divided by 16 prior to the phase detector. A 16MHz clock input provides a 1MHz reference frequency. The VCO of the PLL operates over a range of 200 to 700MHz. The output of the M divider is also applied to the phase detector.

The phase detector and the M divider force the VCO output frequency to be 2M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to each of the LVPECL output buffers. The divider provides a 50% output duty cycle.

The programmable features of the ICS8430-111 support two input modes to program the M divider and N output divider. The two input operational modes are parallel and serial. *Figure 1* shows the timing diagram for each mode. In parallel mode the nP\_LOAD input is LOW. The data on inputs M0 through M8 and N0 through N1 is passed directly to the M divider and N output divider. On the LOW-to-HIGH transition of the nP\_LOAD input, the data is latched and the M divider remains loaded until the next LOW transition on nP\_LOAD or until a serial event occurs. The TEST output is Mode 000 (shift register out) when operating in the parallel input mode. The relationship between the VCO frequency, the crystal frequency and the M divider is defined as follows:

$$f_{VCO} = \frac{f_{xtal}}{16} \times 2M$$

The M value and the required values of M0 through M8 are shown in Table 3B, Programmable VCO Frequency Function Table. Valid M values for which the PLL will achieve lock are defined as  $125 \leq M \leq 350$ . The frequency out is defined as follows:

$$f_{out} = \frac{f_{VCO}}{N} = \frac{f_{xtal}}{16} \times \frac{2M}{N}$$

Serial operation occurs when nP\_LOAD is HIGH and S\_LOAD is LOW. The shift register is loaded by sampling the S\_DATA bits with the rising edge of S\_CLOCK. The contents of the shift register are loaded into the M divider and N output divider when S\_LOAD transitions from LOW-to-HIGH. The M divide and N output divide values are latched on the HIGH-to-LOW transition of S\_LOAD. If S\_LOAD is held HIGH, data at the S\_DATA input is passed directly to the M divider and N output divider on each rising edge of S\_CLOCK. The serial mode can be used to program the M and N bits and test bits T1 and T0. The internal registers T0 and T1 determine the state of the TEST output as follows:

T1	T0	TEST Output
0	0	LOW
0	1	S_Data, Shift Register Input
1	0	Output of M divider
1	1	CMOS Fout

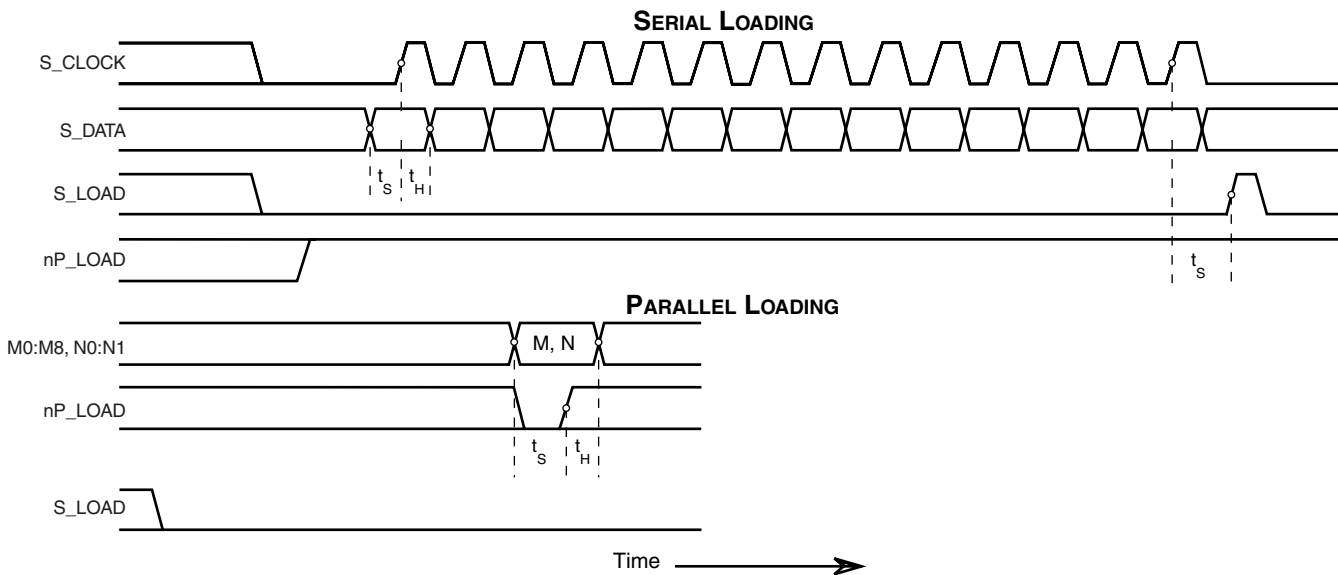


FIGURE 1. PARALLEL & SERIAL LOAD OPERATIONS

\*NOTE: The NULL timing slot must be observed.



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TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2, 3, 28, 29, 30, 31, 32	M5, M6, M7, M0, M1, M2, M3, M4	Input	Pulldown	M divider inputs. Data latched on LOW-to-HIGH transition of nP_LOAD input. LVCMOS/LVTTL interface levels.
4	M8	Input	Pullup	
5, 6	N0, N1	Input	Pulldown	Determines output divider value as defined in Table 3C Function Table. LVCMOS/LVTTL interface levels.
7	N2	Input	Pullup	
8, 16	V <sub>EE</sub>	Power		Negative supply pins.
9	TEST	Output		Test output which is ACTIVE in the serial mode of operation. Output driven LOW in parallel mode. LVCMOS/LVTTL interface levels.
10	V <sub>CC</sub>	Power		Core supply pin.
11, 12	FOUT1, nFOUT1	Output		Differential output for the synthesizer. 3.3V LVPECL interface levels.
13	V <sub>CCO</sub>	Power		Output supply pin.
14, 15	FOUT0, nFOUT0	Output		Differential output for the synthesizer. 3.3V LVPECL interface levels.
17	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs FOUTx to go low and the inverted outputs nFOUTx to go high. When logic LOW, the internal dividers and the outputs are enabled. Assertion of MR does not affect loaded M, N, and T values. LVCMOS / LVTTL interface levels.
18	S_CLOCK	Input	Pulldown	Clocks in serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK. LVCMOS/LVTTL interface levels.
19	S_DATA	Input	Pulldown	Shift register serial input. Data sampled on the rising edge of S_CLOCK. LVCMOS/LVTTL interface levels.
20	S_LOAD	Input	Pulldown	Controls transition of data from shift register into the dividers. LVCMOS/LVTTL interface levels.
21	V <sub>CCA</sub>	Power		Analog supply pin.
22	CLK_SEL	Input	Pullup	Selects between differential clock or test inputs as the PLL reference source. Selects CLK, nCLK inputs when HIGH. Selects TEST_CLK when LOW. LVCMOS/LVTTL interface levels.
23	TEST_CLK	Input	Pulldown	Test clock input. LVCMOS/LVTTL interface levels.
24	CLK	Input	Pulldown	Non-inverting differential clock input.
25	nCLK	Input	Pullup	Inverting differential clock input.
26	nP_LOAD	Input	Pulldown	Parallel load input. Determines when data present at M8:M0 is loaded into the M divider, and when data present at N2:N0 sets the N output divider value. LVCMOS/LVTTL interface levels.
27	VCO_SEL	Input	Pullup	Determines whether synthesizer is in PLL or bypass mode. LVCMOS/LVTTL interface levels.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ



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**TABLE 3A. PARALLEL AND SERIAL MODE FUNCTION TABLE**

Inputs							Conditions
MR	nP_LOAD	M	N	S_LOAD	S_CLOCK	S_DATA	
H	X	X	X	X	X	X	Reset. Forces outputs LOW.
L	L	Data	Data	X	X	X	Data on M and N inputs passed directly to the M divider and N output divider. TEST output forced LOW.
L	↑	Data	Data	L	X	X	Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs.
L	H	X	X	L	↑	Data	Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK.
L	H	X	X	↑	L	Data	Contents of the shift register are passed to the M divider and N output divider.
L	H	X	X	↓	L	Data	M divider and N output divider values are latched.
L	H	X	X	L	X	X	Parallel or serial input do not affect shift registers.
L	H	X	X	H	↑	Data	S_DATA passed directly to M divider as it is clocked.

NOTE: L = LOW  
H = HIGH  
X = Don't care  
↑ = Rising edge transition  
↓ = Falling edge transition

**TABLE 3B. PROGRAMMABLE VCO FREQUENCY FUNCTION TABLE (NOTE 1)**

VCO Frequency (MHz)	M Divide	256	128	64	32	16	8	4	2	1
		M8	M7	M6	M5	M4	M3	M2	M1	M0
200	100	0	0	1	1	0	0	1	0	0
202	101	0	0	1	1	0	0	1	0	1
204	102	0	0	1	1	0	0	1	1	0
206	103	0	0	1	1	0	0	1	1	1
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
696	348	1	0	1	0	1	1	1	0	0
698	349	1	0	1	0	1	1	1	0	1
700	350	1	0	1	0	1	1	1	1	0

NOTE 1: These M divide values and the resulting frequencies correspond to an input frequency of 16MHz.

**TABLE 3C. PROGRAMMABLE OUTPUT DIVIDER FUNCTION TABLE**

Input			N Divider Value	Output Frequency (MHz)	
N2	N1	N0		Minimum	Maximum
0	0	0	2	100	350
0	0	1	4	50	175
0	1	0	8	25	87.5
0	1	1	16	12.5	43.75
1	0	0	1	200	700
1	0	1	2	100	350
1	1	0	4	50	175
1	1	1	8	25	87.5



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### ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{CC}$	4.6V
Inputs, $V_I$	-0.5V to $V_{CC} + 0.5V$
Outputs, $I_O$	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, $\theta_{JA}$	65.7°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Core Supply		3.135	3.3	3.465	V
$V_{CCA}$	Analog Voltage		3.135	3.3	3.465	V
$V_{CCO}$	Output Voltage		3.135	3.3	3.465	V
$I_{EE}$	Power Supply Current			120		mA
$I_{CCA}$	Analog Supply Current			10		mA

**TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage			2		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage			-0.3		0.8	V
$I_{IH}$	Input High Current	M0-M7, N0, N1, MR, S_CLOCK, S_DATA, S_LOAD, TEST_CLK, nP_LOAD	$V_{CC} = V_{IN} = 3.465V$			150	$\mu A$
		M8, N2, CLK_SEL, VCO_SEL	$V_{CC} = V_{IN} = 3.465V$			5	$\mu A$
$I_{IL}$	Input Low Current	M0-M7, N0, N1, MR, S_CLOCK, S_DATA, S_LOAD, TEST_CLK, nP_LOAD	$V_{CC} = 3.465V$ , $V_{IN} = 0V$	-5			$\mu A$
		M8, N2, CLK_SEL, VCO_SEL	$V_{CC} = 3.465V$ , $V_{IN} = 0V$	-150			$\mu A$
$V_{OH}$	Output High Voltage	TEST; NOTE 1		2.6			V
$V_{OL}$	Output Low Voltage	TEST; NOTE 1				0.5	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CCO}/2$ .



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**TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	nCLK	$V_{IN} = V_{CC} = 3.465V$		5	$\mu A$
		CLK	$V_{IN} = V_{CC} = 3.465V$		150	$\mu A$
$I_{IL}$	Input Low Current	nCLK	$V_{IN} = 0V, V_{CC} = 3.465V$	-150		$\mu A$
		CLK	$V_{IN} = 0V, V_{CC} = 3.465V$	-5		$\mu A$
$V_{PP}$	Peak-to-Peak Input Voltage		0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		$V_{EE} + 0.5$		$V_{CC} - 0.85$	V

NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is  $V_{CC} + 0.3V$ .

NOTE 2: Common mode voltage is defined as  $V_{IH}$ .

**TABLE 4D. LVPECL DC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CCO} - 1.4$		$V_{CCO} - 0.9$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CCO} - 2.0$		$V_{CCO} - 1.7$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CCO} - 2V$ . See 3.3V Output Load Test Circuit figure in the Parameter Measurement Information section.

**TABLE 5. INPUT FREQUENCY CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{IN}$	Input Frequency	TEST_CLK; NOTE 1	14		27	MHz
		CLK, nCLK; NOTE 1	14		27	MHz
		S_CLOCK			50	MHz

NOTE1: For the differential input and reference frequency range, the M value must be set for the VCO to operate within the 200MHz to 700MHz range. Using the minimum input frequency of 14MHz, valid values of M are  $115 \leq M \leq 400$ . Using the maximum frequency of 27MHz, valid values of M are  $60 \leq M \leq 208$ .



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**TABLE 6. AC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$F_{MAX}$	Output Frequency				700	MHz
$f_{jit(cc)}$	Cycle-to-Cycle Jitter; NOTE 1	$f_{OUT} > 87.5MHz$			25	ps
		$f_{OUT} < 87.5MHz$			40	ps
$f_{jit(per)}$	Period Jitter, RMS				9.5	ps
$t_{sk(o)}$	Output Skew; NOTE 1, 2				15	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	200		700	ps
$t_S$	Setup Time	M, N to nP_LOAD	5			ns
		S_DATA to S_CLOCK	5			ns
		S_CLOCK to S_LOAD	5			ns
$t_H$	Hold Time	M, N to nP_LOAD	5			ns
		S_DATA to S_CLOCK	5			ns
		S_CLOCK to S_LOAD	5			ns
odc	Output Duty Cycle	$N \neq 1$	48		52	%
		$N = 1$	45		55	%
$t_{LOCK}$	PLL Lock Time				1	ms

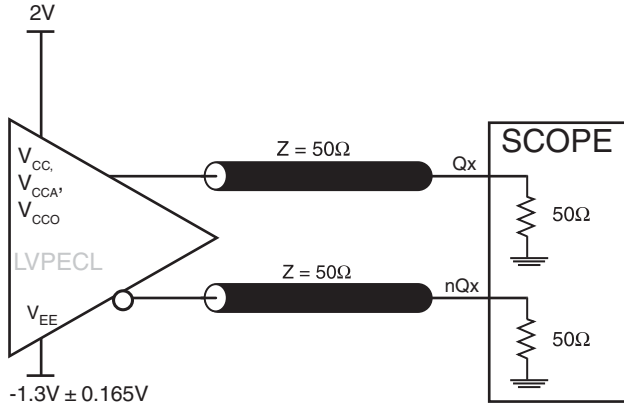
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: See Parameter Measurement Information section.

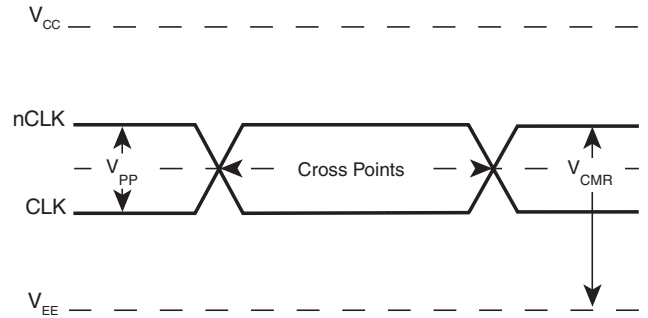
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

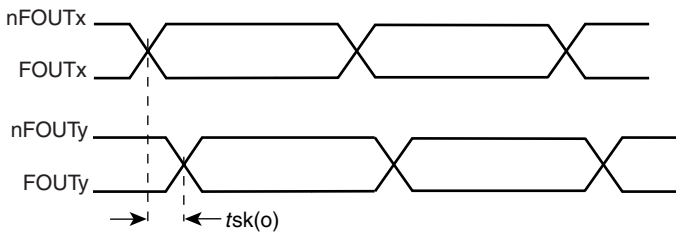
### PARAMETER MEASUREMENT INFORMATION



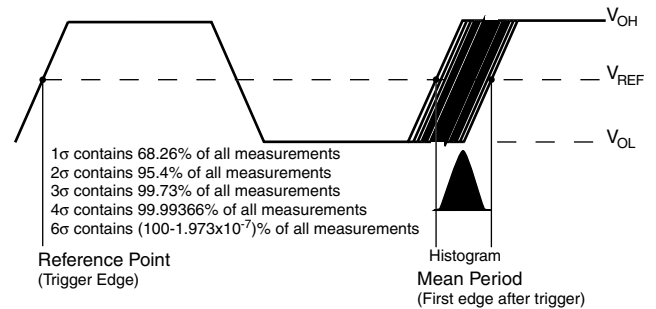
**3.3V OUTPUT LOAD AC TEST CIRCUIT**



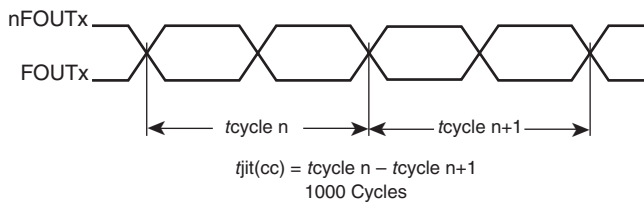
**DIFFERENTIAL INPUT LEVEL**



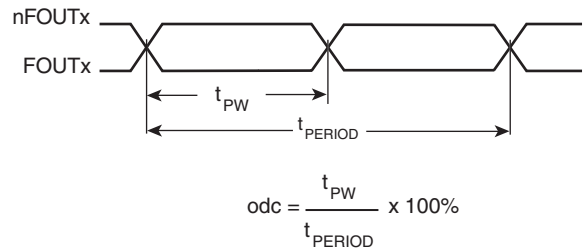
**OUTPUT SKEW**



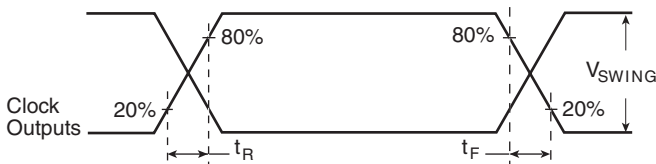
**PERIOD JITTER**



**CYCLE-TO-CYCLE JITTER**



**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**



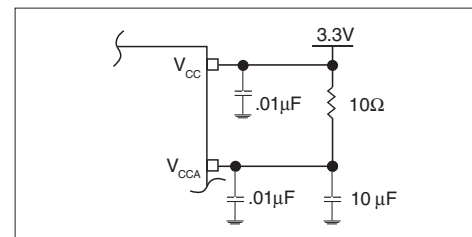
**OUTPUT RISE/FALL TIME**



### APPLICATION INFORMATION

#### POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8430-111 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{CC}$ ,  $V_{CCA}$ , and  $V_{CCO}$  should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 2* illustrates how a 10Ω resistor along with a 10μF and a .01μF bypass capacitor should be connected to each  $V_{CCA}$  pin. The 10Ω resistor can also be replaced by a ferrite bead.



**FIGURE 2. POWER SUPPLY FILTERING**

#### RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

##### INPUTS:

###### TEST\_CLK INPUT:

For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the TEST\_CLK to ground.

###### CLK/nCLK INPUT:

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

###### LVC MOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

##### OUTPUTS:

###### LVPECL OUTPUT

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 3 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{CC}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio

of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{CC} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .

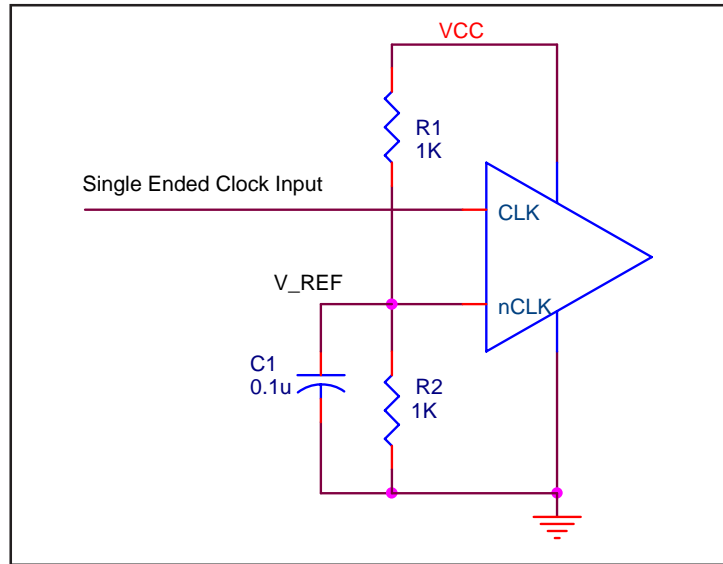
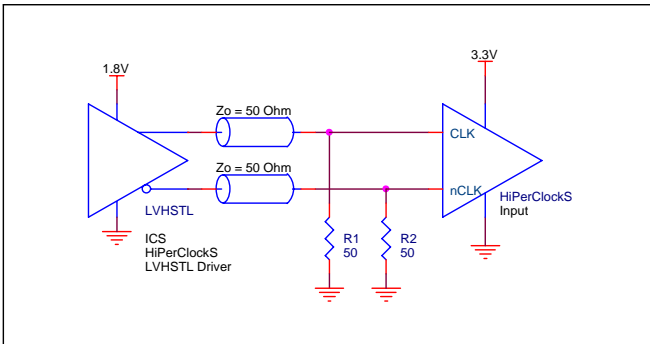


FIGURE 3. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

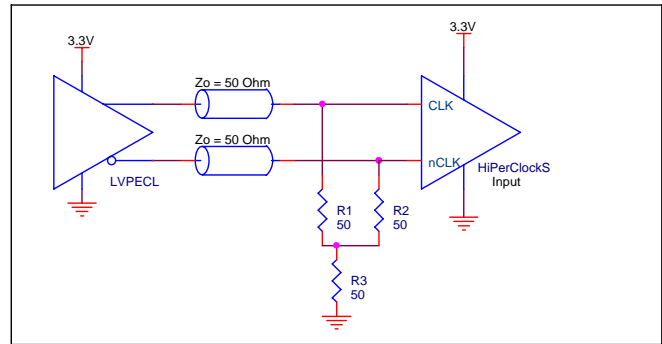
#### DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSSL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 4A to 4E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are

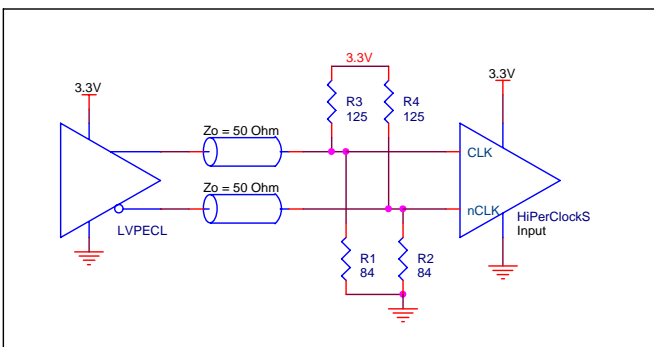
examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 4A*, the input termination applies for IDT HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



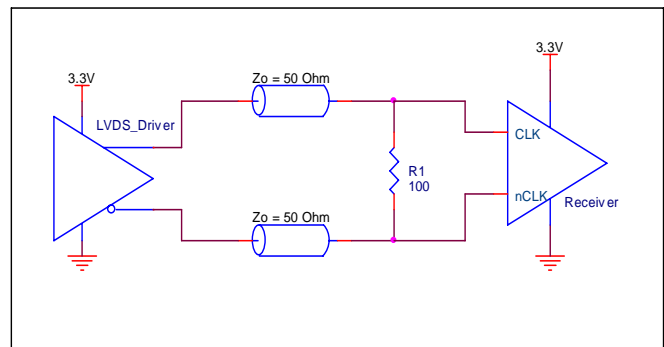
**FIGURE 4A. HiPerClockS CLK/nCLK INPUT DRIVEN BY IDT HiPerClockS LVHSTL DRIVER**



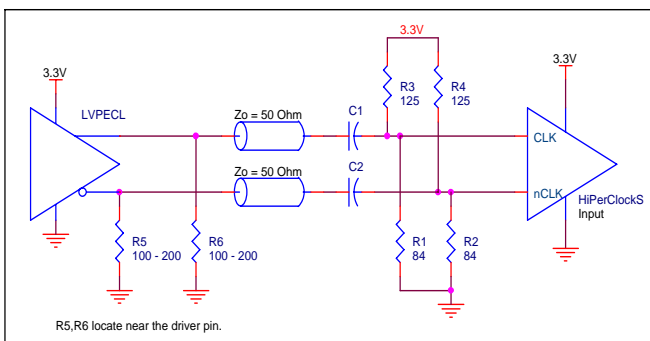
**FIGURE 4B. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 4C. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 4D. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER**



**FIGURE 4E. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE**

### TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to

drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

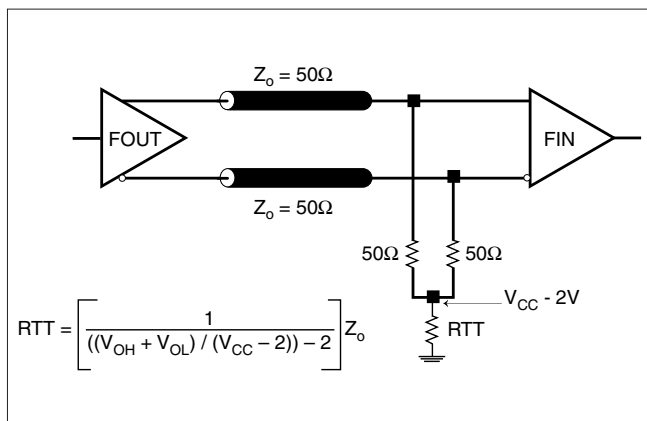


FIGURE 5A. LVPECL OUTPUT TERMINATION

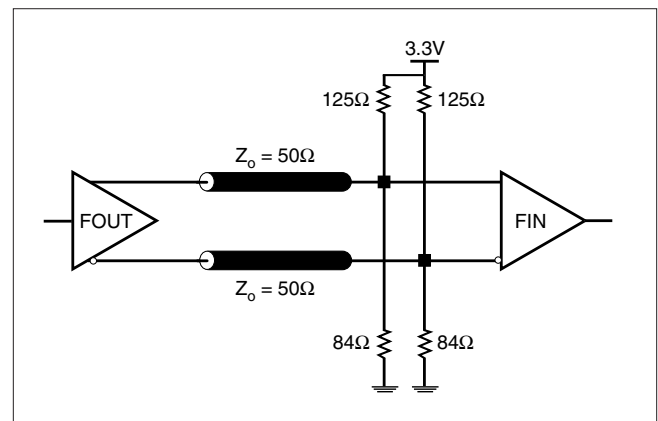


FIGURE 5B. LVPECL OUTPUT TERMINATION

### POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8430-111. Equations and example calculations are also provided.

#### 1. Power Dissipation.

The total power dissipation for the ICS8430-111 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC,MAX} * I_{EE,MAX} = 3.465V * 120mA = 415.8mW$
- Power (outputs)<sub>MAX</sub> = **30mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $2 * 30mW = 60mW$

**Total Power**<sub>MAX</sub> (3.465V, with all outputs switching) =  $415.8mW + 60mW = 475.8mW$

#### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd_{total} + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd_{total}$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 65.7°C/W per Table 7 below.

Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$70°C + 0.476W * 65.7°C/W = 101.3°C$ . This is well below the limit of 125°C.

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

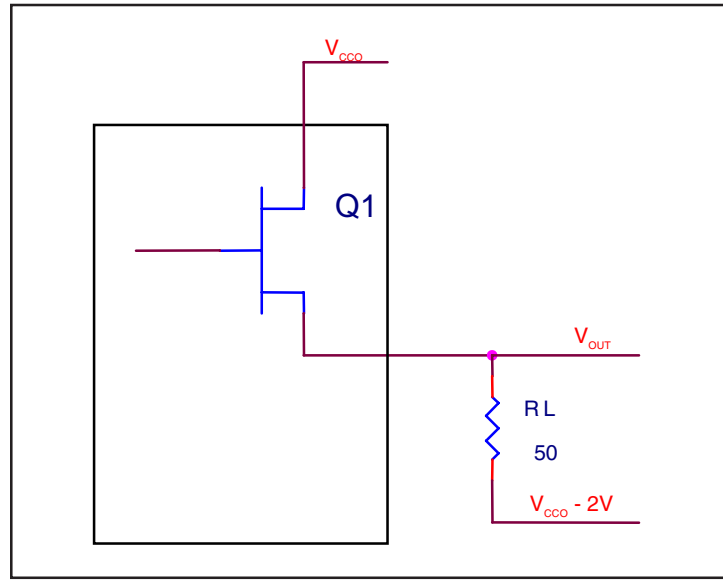
**TABLE 7. THERMAL RESISTANCE  $\theta_{JA}$  FOR 32-PIN LQFP, FORCED CONVECTION**

$\theta_{JA}$ by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	65.7°C/W	55.9°C/W	52.4°C/W

### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6*.



**FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CCO} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CCO\_MAX} - 0.9V$

$$(V_{CCO\_MAX} - V_{OH\_MAX}) = 0.9V$$

- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CCO\_MAX} - 1.7V$

$$(V_{CCO\_MAX} - V_{OL\_MAX}) = 1.7V$$

Pd\_H is power dissipation when the output drives high.

Pd\_L is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

Total Power Dissipation per output pair = Pd\_H + Pd\_L = 30mW



**RELIABILITY INFORMATION**

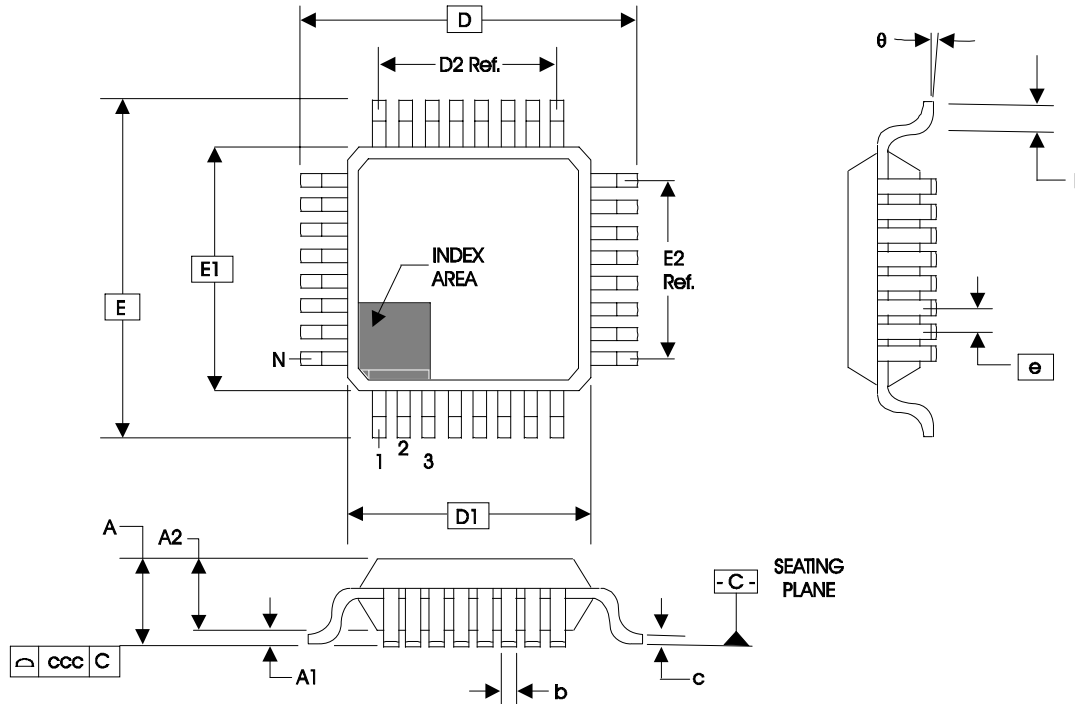
**TABLE 8.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 32 LEAD LQFP**

	$\theta_{JA}$ by Velocity (Meters per Second)		
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	65.7°C/W	55.9°C/W	52.4°C/W

**TRANSISTOR COUNT**

The transistor count for ICS8430-111 is: 3960

### PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD LQFP



**TABLE 9. PACKAGE DIMENSIONS**

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N	32		
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09		0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60	
e		0.80 BASIC	
L	0.45	0.60	0.75
q	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026





# 700MHz, Low Jitter, Differential-to-3.3V LVPECL Frequency Synthesizer

ICS8430-111

PRELIMINARY DATA SHEET

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8430DY-111	ICS8430DY-111	32 Lead LQFP	tray	0°C to 70°C
8430DY-111T	ICS8430DY-111	32 Lead LQFP	1000 tape & reel	0°C to 70°C
8430DY-111LF	ICS8430D111L	32 Lead "Lead-Free" LQFP	tray	0°C to 70°C
8430DY-111LFT	ICS8430D111L	32 Lead "Lead-Free" LQFP	1000 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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