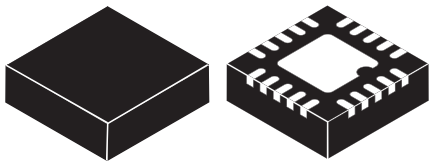
PM6613N

2 to 4-cell Li-Ion, Li-FePO$_4$ battery charger with SMBus interface, N-channel RBFET and BATFET MOSFET selectors

Datasheet - production data



VFQFPN 3x3 20L

Features

- Synchronous buck converter with N-channel high-side, low-side power MOSFET integrated drivers
- 350 kHz or 700 kHz switching frequency, selectable with SMBus
- AC adapter input voltage range 9 V - 24 V
- 5 V bias input voltage supply
- Battery charge voltage range 2.5 V -18 V
- ±1.53% charge voltage accuracy
- 0.1% cell charge voltage resolution
- ±3% charge current accuracy
- ±3% input current accuracy
- Overvoltage, overcurrent protections
- Battery, inductor, power MOSFET short-circuit protection
- Internal loop compensation network
- Integrated soft-start
- Selector
  - N-channel ACFET/RBFET MOSFET driver
  - N-channel BATFET MOSFET driver
- System
  - 1 mA quiescent supply current
  - 17 µA - 35 µA sleep mode current (BATFET charge pump off - on)
  - Thermal shutdown list

Applications

- Mobile PC:
  - UMPC/MID and tablets
  - Netbook and notebook computers

Description

The PM6613N is a high efficiency battery charger with SMBus communication interface. It includes a synchronous switching DC-DC converter with N-channel high-side and low-side power MOSFET drivers. The possibility to set the switching frequency with SMBus by choosing one of the two preset values of 350 kHz or 700 kHz assures the best trade-off between power conversion efficiency and PCB cost and size.

Integrated loop compensation network and soft-start allow the reduction of the number of external components.

The PM6613N integrates 2 charge pumps to drive N-channel ACFET/RBFET and BATFET MOSFETs.

The SMBus communication interface is used to set the battery charge current and voltage.

The PM6613N charges 2 to 4 series Li-Ion or LiFePO$_4$ cells, for mobile PC applications. It is available in a compact VFQFPN 3x3 mm package.

Table 1. Device summary

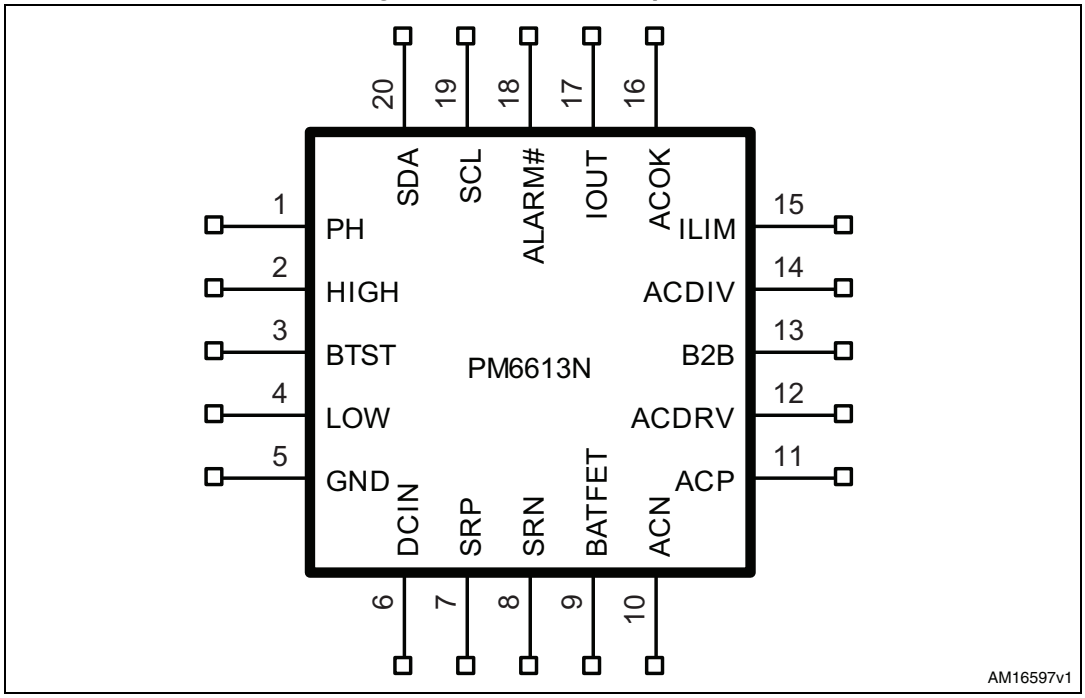
Order code	Package	Packing
PM6613NTR	VFQFPN 3x3 20L	Tape and reel

Contents

List of tables

1 Device pinout

Figure 1. The PM6613N pinout



2 Pin description

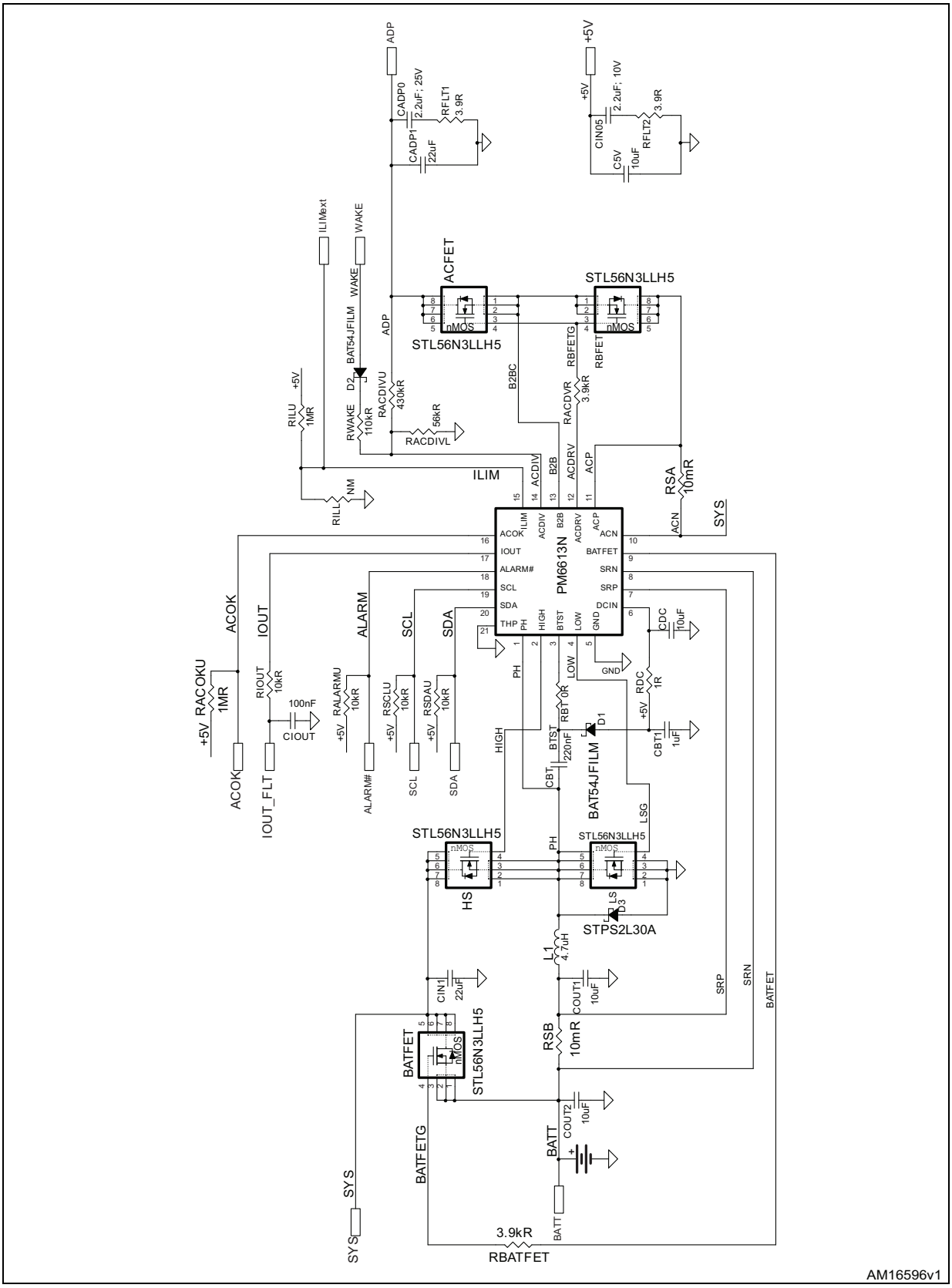
Table 2. Pin description

Pin	Name	Description
1	PH	High-side power nMOS driver source. Connection to the high-side nMOS source pin and low-side nMOS drain pin.
2	HIGH	High-side power nMOS driver output. Connection to the high-side nMOS gate pin. In critical application conditions, a series resistor can be used to increase the nMOS turn-on/off time and to limit the phase ringing, R = 4.7 Ω.
3	BTST	High-side power nMOS driver power supply. Connection to 5 V power supply voltage through a Schottky diode, and to the phase net through a filtering capacitor.
4	LOW	Low-side power nMOS driver output. Connection to the low-side nMOS gate pin. In critical application conditions, a series resistor can be used to increase the nMOS turn-on/off time and to limit the phase ringing, R = 4.7Ω.
5	GND	Device analog and power ground reference.
6	DCIN	5 V input power supply. It is used to bias the internal logic and to supply the internal power drivers. An RC filter is used to limit inrush current and voltage spikes, typical value R=1 Ω, C=10 µF.
7	SRP	Battery charge current sense resistor positive pin.
8	SRN	Battery charge current sense resistor negative pin.
9	BATFET	nMOS driver output. Connection to the BATFET nMOS gate pin, through a series resistor used to limit the inrush current.
10	ACN	Input current sense resistor negative input. System power connection.
11	ACP	Input current sense resistor positive input. RBFET nNMOS drain pin connection.
12	ACDRV	nMOS driver output. Connection to the ACFET and RBFET nMOS gate pin, through a series resistor used to limit the inrush current.
13	B2B	Output driven by AC adapter back-to-back MOS switches. Connection to the ACFET and RBFET nMOS source pins.
14	ACDIV	Adapter detection pin. Adapter resistor divider connection.
15	ILIM	Battery charge current limit setting pin.
16	ACOK	AC adapter detection status pin. Open-drain pin. It pulls high, when a valid adapter voltage is detected: 2 V < ACDIV < 2.625 V. It pulls low when ACDIV > 2.625 V or ACDIV < 2 V.
17	IOUT	Adapter/battery charge current output pin, selectable using SMBus command. I_{OUT} voltage is 20 times the differential voltage across sense resistor.
18	ALARM#	Open-drain output pin. Low when a fault condition is detected, to trigger the system microcontroller interrupt.

Table 2. Pin description (continued)

Pin	Name	Description
19	SCL	SMBus clock pin. Connection to the SMBus clock line. Open-drain pin, a pull-up resistor R = 10 kΩ is used.
20	SDA	SMBus data pin. Connection to the SMBus data line. Open-drain pin, a pull-up resistor R = 10 kΩ is used.

Figure 2. Typical application circuit



3 Electrical characteristics

3.1 Absolute maximum ratings

Stresses beyond those listed in "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 3. Voltage characteristics

PINs	Values	Unit
BATFET, ACDRV, BTST, HIGH to GND	-0.3 to 36	V
SRP, SRN, B2B, ACP, ACN to GND	-0.3 to 30	
LOW, DCIN, ACDIV, ILIM to GND	-0.3 to 6	
PH to GND	-2 to 30	
BTST to PH	-0.3 to 6	
ACOK, IOUT, ALARM#, SCL, SDA to GND	-0.3 to 6	
SRP to SRN, ACP to ACN	-0.5 to 0.5	
ACDRV to B2B	-0.3 to 7	
BATFET to SRN	-0.3 to 7	

Table 4. Thermal characteristics

Symbol	Parameters	Values	Unit
$R_{th(JA)}$	Thermal resistance junction-to-ambient	45	°C/W
T_J	Junction operating temperature range	-40 to 125	°C
T_A	Ambient operating temperature range	-40 to 85	
T_{stg}	Storage temperature range	-50 to 150	

Table 5. Electrical characteristics

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Unit
Supply current						
I_{SLP}	Total current (DCIN, SRN, SRP, ACP, ACN, PH) consumption in sleep mode	ACDIV < $ACDIV_{SLP}$ BATFET on		40	60	uA
		ACDIV < $ACDIV_{SLP}$ BATFET off		18	35	
I_{OP}	Total quiescent supply current	Charge disabled		1.25	2.1	mA
Supply voltage						
$DCIN_{UVLO}$	DCIN UVLO rising threshold		3.8	4	4.2	V
	DCIN UVLO falling threshold		3.65	3.85	4.05	
ACOK comparator						
$ACDIV_{TH}$	ACDIV rising voltage threshold to assert ACOK		1.87	2	2.13	V
$ACDIV_{HYS}$	ACDIV voltage threshold hysteresis		5	20	35	mV
$ACDIV_{SLP}$	ACDIV voltage threshold to enable internal bias		0.55	0.65	0.75	V
$ACDIV_{OV}$	ACDIV rising threshold voltage to determine an OV condition that let ACOK go low		2.55	2.625	2.70	V
$ACDIV_{OV\_H}$	ACDIV overvoltage hysteresis		35	65	95	mV
t_{R_ACOK}	Rising edge deglitch time	AD bit cleared	230	250	270	ms
Switching frequency						
f_{SW}	Buck converter switching frequency	BSE bit cleared	600	700	800	kHz
		BSE bit set	300	350	400	
Charging voltage						
V_{BATT_ERR}	Charge voltage accuracy		-1.53		1.53	%
Charging current						
I_{CHG_ERR}	Charge current accuracy V_{SRN} = 12 V	I_{CHG} = 0.128 A R_{SENSE} = 10 mΩ	-50		50	%
		I_{CHG} = 8.192 A R_{SENSE} = 10 mΩ	-3		+3	
Adapter current sense amplifier						
I_{ADP_G}	Current sense amplifier gain		18	20	22	
$I_{ADP\_G\_ERR}$	Current sense amplifier gain error		-10		10	%

Table 5. Electrical characteristics (continued)

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Unit
I_{ADP_SRC}	I_{ACP} + I_{ACN} source current	V_{SENSE} = = ACP- ACN = 0	5	25	45	mA
Battery current sense amplifier						
I_{BATT_G}	Current sense amplifier gain		18	20	22	
$I_{BATT\_G\_ERR}$	Current sense amplifier gain error		-10		+10	%
I_{BATT_SRC}	I_{SRP} + I_{SRN} source current	V_{SENSE} = = SRP- SRN = 0	5	25	50	mA
Light load comparator						
I_{LL}	Light load average current falling threshold for asynchronous working mode. Low-side MOSFET turned on only when $I_{CHG} > I_{LL}$	AM[1:0]=0x0	0.25	0.45	0.65	A
		AM[1:0]=0x1	0.70	0.90	1.10	
		AM[1:0]=0x2	1.10	1.30	1.50	
		AM[1:0]=0x3	1.50	1.70	1.90	
I_{LL_hys}	I_{LL} hysteresis		255	280	305	mA
B2B						
I_{B2B}	B2B pull-down current	ACOK = '0' DCIN = 5 V	1.9	2.3	2.7	mA
V_{B2B_LOW}	B2B rising threshold to enable charge		4.4	5	5.6	V
$V_{B2B\_LOW\_H}$	V_{B2B_LOW} hysteresis		300	450	600	mV
I_{LIM} comparator						
V_{ILIM_FALL}	I_{LIM} falling threshold for disabling charge		55	75	95	mV
V_{ILIM_RISE}	I_{LIM} rising threshold for enabling charge		75	95	115	
Battery fault comparators						
V_{BATT_LOW}	Battery voltage rising threshold for enabling charge		2.45	2.55	2.65	V
$V_{BATT\_LOW\_HIST}$	V_{BATT_LOW} comparator hysteresis		85	100	115	mV
V_{BATT_OV}	Battery overvoltage rising threshold as difference between SRN voltage and CHRG_VOLT register value	Li- Ion	120	170	220	mV/cell
		$LiFePO_4$	100	140	170	

Table 5. Electrical characteristics (continued)

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Unit
$V_{BATT\_OV\_H}$	V_{BATT_OV} overvoltage hysteresis	Li- Ion	75	90	105	mV/cell
		$LiFePO_4$	55	75	85	
$V_{BATT\_OV\_PD}$	Pull down current on SRN pin during overvoltage condition		3.5	5	6.5	mA
I_{BATT_OC}	Battery overcurrent threshold as difference with CHRG_AMP register value		1.7	2	2.3	A
$I_{BATT\_OC\_H}$	BATTERY overcurrent hysteresis		300	400	510	mA
Adapter fault comparators						
I_{ADP_OC}	Adapter input overcurrent threshold as difference with INPUT_AMP register value		1.7	2	2.3	A
$I_{ADP\_OC\_H}$	I_{ADP_OC} overcurrent hysteresis		250	400	550	mA
BATFET driver						
V_{BATFET_DRV}	BATFET gate driving voltage respect to SRN pin	BATFET-SRN	5.3	6	6.6	V
I_{BATFET_SHORT}	BATFET driver max. current	BATFET shorted to SRN	35	60	80	mA
ACDRV driver						
V_{ACDRV_DRV}	RBFET gate driving voltage respect to B2B pin	ACDRV-B2B	5.3	6	6.6	V
I_{ACDRV_SHORT}	BATFET driver max. current	BATFET shorted to SRN	35	55	75	mA

3.2 Operating characteristics

Table 6. Typical operating characteristics

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Unit
Charging voltage						
V_{CELL_RES}	Cell voltage resolution			4		mV/cell
Charging current						
I_{CHG_RES}	Charge current control resolution	R_{SENSE} = 10 mΩ		64		mA
A2B adapter to battery comparator						
t_{R_A2B}	Rising edge deglitch time			3		ms
Adapter current sense amplifier						
I_{ADP_VOS}	Current sense amplifier offset	Referred to input		1		mV
Battery current sense amplifier						
I_{BATT_VOS}	Current sense amplifier offset	Referred to input		1		mV
HS short detection(1)						
V_{HS_SHORT}	Phase to GND threshold for high-side short detection when low-side is on			200		mV
t_{HS_SHORT}	Mask time on HS_SHORT from low-side turn-on time			300		ns
BATFET driver						
R_{BATFET_DRV}	BATFET driver output impedance	I_{BATFET} < 20 µA		42		kΩ
R_{BATFET_OFF}	Charge pump off resistance			5		kΩ
ACDRV driver						
R_{ACDRV_DRV}	RBFET driver output impedance	I_{ACDRV} < 20 µA		42		kΩ
R_{ACDRV_OFF}	Charge pump off resistance			5		kΩ
HS driver(1)						
HS_{RON}	High-side driver turn-on resistance	V_{BTST} -V_{PH} = 5 V		3.6		Ω
HS_{ROFF}	High-side driver turn-off resistance			0.7		
LS driver(1)						
LS_{RON}	Low-side driver turn-on resistance			3.2		Ω
LS_{ROFF}	Low-side driver turn-off resistance			0.8		

1. Guaranteed by design

3.3 Recommended operating conditions

(DCIN = 5 V, T_j = 25 °C unless otherwise specified)

Table 7. Recommended operating conditions

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Unit
Supply voltage						
$DCIN_{OP}$	DCIN input voltage operating range		4.5		5.5	V
V_{ADP}	Adapter maximum voltage				24	V
Charging voltage						
V_{CELL}	Cell charge voltage	Li-Ion	4		4.508	V/cell
		LiFePO4	3.4		3.908	
V_{BATT}	Charge voltage range		6.8		18.032	V
Charging current						
I_{CHG}	Buck converter regulated charge current range	R_{SENSE} = 10 mΩ	0.128		16.320	A
A2B adapter to battery comparator						
$A2B_{TH}$	A2B rising threshold		0.35	0.45	0.55	V
I_{A2B}	A2B sink current from B2B pin		12	14	16	µA
Adapter current sense amplifier						
I_{ADP_CM}	IADP input common mode minimum voltage		2.5			V
Battery current sense amplifier						
I_{BATT_CM}	IBATT input common mode minimum voltage		2.5			V
Thermal protection						
T_{SHUT}	Temperature rising threshold for disabling charge			160		°C
T_{SHUT_H}	Thermal shutdown temperature hysteresis			10		°C

Table 8. SMBus communication timing values

Symbol	Parameters	Min.	Max.	Unit
f_{SMB}	SMBus operating frequency	10	100	kHz
$t_{(BUF)}$	Bus free time between stop and start condition	4.7		µs
$t_{h(STA)}$	Hold time after (repeated) start condition. After this period, the first clock is generated	4		
$t_{SU(STA)}$	Repeated start condition setup time	4.7		
$t_{SU(STOP)}$	Stop condition setup time	4		
$t_{H(DAT)}$	Data hold time	300		ns
$t_{SU(DAT)}$	Data setup time	250		
$t_{TIMEOUT}$	Detect clock high timeout		50	µs
$t_{w(L)}$	Clock low period	4.7		µs
$t_{w(H)}$	Clock high period	4	50	
t_r	Clock/data fall time		300	ns
t_f	Clock/data rise time		1000	
t_{POR}	Time in which a device must be operational after power-on reset		500	ms

Table 9. Low power SMBus DC specifications

Symbol	Parameters	Min.	Max.	Unit
V_{IL}	Data, clock input low voltage		0.8	V
V_{IH}	Data, clock input high voltage	2.1	VDD	
V_{OL}	Data, clock output low voltage		0.4	
I_{LEAK}	Input leakage		±5	µA
I_{PULLUP}	Current through pull-up resistor or current source	100	350	
VDD	Nominal SMBus voltage	2.7	5.5	V

4 Operating description

4.1 SMBus communication interface

The PM6613N communicates to the system MCU by the SMBus interface. The PM6613N is compliant with the system management Bus specification v2.0 (please refer to the official website www.smbus.org).

The PM6613N uses a simplified command subset, with SMBus read-word and write-word protocols to communicate to the system MCU.The PM6613N works in slave mode only; according to the SMBus specifications, the slave address is set by using 7 bits, the value is 0b0010010 (0x12).

The SMBus interface input pins SDA (data) and SCL (clock) have Schmitt-trigger inputs. Selecting pull-up resistors by 10 k for both of them to achieve rise times according to the SMBus specifications.

A watchdog timer adjust function is provided within register 0x12. The charge is suspended if IC does not receive write charge voltage or write charge current command within the watchdog time period and watchdog timer is enabled. The charge is resumed after receiving write charge voltage or write charge current command when watchdog timer expires and charge suspends.

Figure 3. SMBus communication timing waveforms

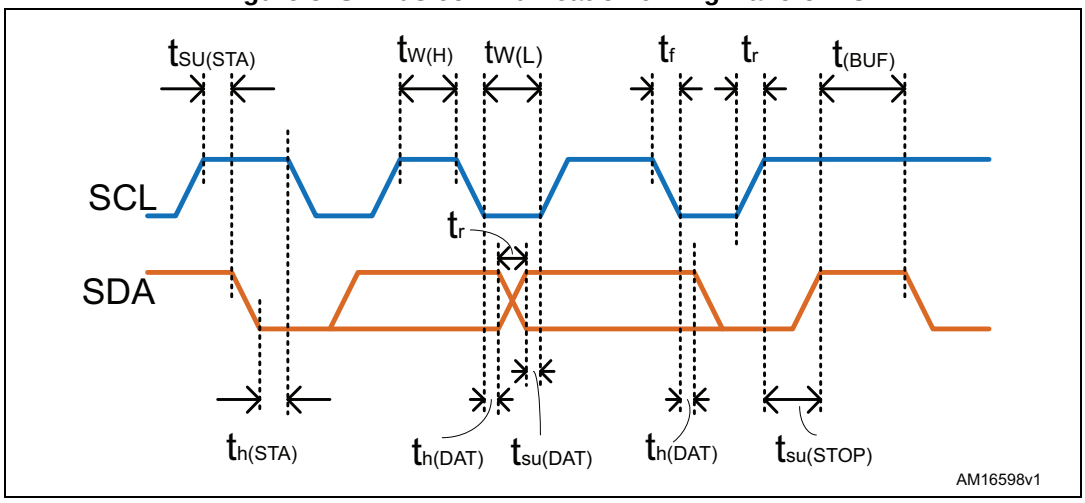
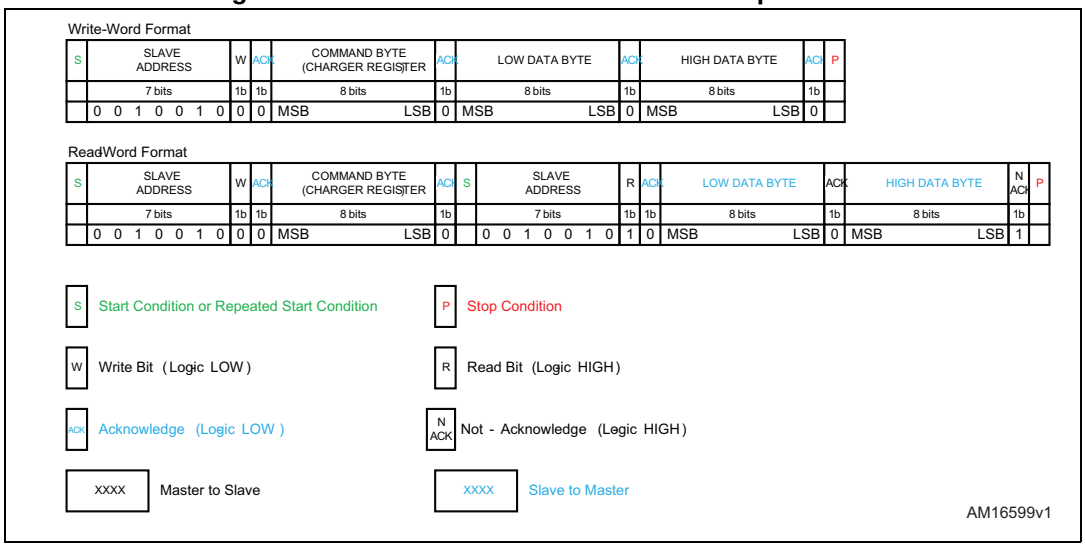


Figure 4. SMBus write-word and read-word protocols



The PM6613N supports 7 SMBus commands as listed in *Table 10*.

Table 10. SMBus command summary

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x12	CHRG_OPT	AD	WD[1:0]		BSE	PF	EFA	EE	AM[1:0]		IS	SOVR	BED	ARED	CF	R	CI
	Reset value	0	1	1	1	0	0	0	1	0	0	0	0	0	0		1
0x13	STATUS	Reserved					TS	HBRO	RBSS	AOC	IOC	BOV	BOC	LB	AOV	AUV	HS
	Reset value						0	0	0	0	0	0	0	0	0	0	0
0x14	CHRG_AMP	Res		AMP[13:6]								Reserved					
	Reset value			0	0	0	0	0	0	0	0						
0x15	CHRG_VOLT	R	VOLT[14:1]														R
	Reset value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x3F	INPUT_AMP	Res		AMP[13:7]							Reserved						
	Reset value			1	0	0	0	0	0	0							
0xFE	MAN_ID	Manufacturer ID															
	Reset value	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	
0xFF	DEV_ID	Device ID															
	Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

4.2 ACFET/RBFET and BATFET system power selectors

The PM6613N integrates 2 charge pumps to drive nMOS selectors for ACFET/RBFET and BATFET. At reset condition, the PM6613N internal circuitry controls the RBFET turn-on, to avoid inrush current flowing from ADP (adapter) to SYS (system). The BATFET selector connects (disconnects) the battery from the system. At reset condition, the BATFET selector is controlled by the internal circuitry. During a charging process, if the adapter is disconnected, the PM6613N stops any charge operation and remains in sleep mode: if the BSE is set, the PM6613N connects the battery to the system. If the SOVR bit is set, the internal circuitry can be disabled: the nMOS selectors can be manually controlled changing the ARED and BED bits respectively.

4.3 Adapter detection

The ACOK pin is an open-drain output signal to inform the system MCU that a valid ADAPTER voltage has been detected by the ACDIV pin (ACDIV > 2 V). At reset condition, for safety reason, a delay is applied to the internal circuitry, in order to avoid false adapter insertions. An adapter insertion is detected when the voltage across ACDIV pin is higher than 2.0 V. A voltage divider assures that when the adapter is inserted a voltage between 2.0 V and 2.65 V is applied to ACDIV pin. The internal circuitry checks for 250 ms that this voltage is stable, and in this case enables the ACFET/RBFET selectors and the ACOK pin. The delay can be removed clearing the AD bit on the CHRG_OPT register.

4.4 Internal charge pumps

Some charge pumps allow the PM6613N to supply the internal drivers necessary to drive the ACFET/RBFET selectors, the BATFET selector and the high-side MOSFET. The ACFET/RBFET selectors are switched off/on by the ACDRV pin. An internal charge pump is used to lift the ACDRV voltage using the voltage coming from the B2B pin.The high-side MOSFET is controlled by the HIGH pin. A charge pump receives the base voltage from the PH pin, allowing the HIGH pin to be toggled. The BATFET selector is driven by the BATFET pin whose voltage is bootstrapped using the BTST pin.

4.5 Switching frequency selection and EMI adjustments

The PM6613N buck converter switching frequency can be chosen, by setting bit 9 and bit 10 of the CHRG_OPT register. The choice depends on the compromise among efficiency, inductance, output capacitor, and the PCB area. An additional offset can be applied to the nominal frequency to avoid EMI issues, setting the bit EE of the CHRG_OPT register. The offset can be set to ±15% changing the bit EFA of the CHRG_OPT register.

4.6 Charge settings

The PM6613N uses 3 SMBus registers and the ILIM pin to control the charging process. The CHRG_VOLT register sets the voltage limit, ranging from a minimum value of 6800 mV to a maximum value of 18032 mV, with 2 mV step resolution. Not all the values are allowed within the above range (see *Table 11* and *Table 12*). Any attempt to write a non valid value causes the internal circuitry to clear the register and stop any charging process. The CHRG_AMP register sets the current limit drained to the battery. The allowable value ranges from a minimum of 128 mA to a maximum of 16320 mA. Setting a value outside this range causes the PM6613N to clear the register and terminate any charging process. The charging current is sensed measuring the differential voltage between SRP and SRN pins where a small resistor value is connected to. A suggested value is 10 mΩ, and not more than 20 mΩ. Greater values increase the sensitivity of the current sensing and the regulation accuracy, but cause a higher power loss and could lead to an overcurrent protection latching.

The charge current limit can be set forcing a voltage through the ILIM pin too. The PM6613N automatically sets the maximum charge current by choosing the minimum value between the I_{LIM} voltage value and the CHRG_AMP register. The relationship between the I_{LIM} voltage and the input current limit is reported below:

Equation 1

$$V_{ILIM} = R_{SB} \cdot I_{CHG} \cdot 10 + 0.03125$$

whereas R_{SB} is the sensing resistor connected between the SRP and SRN pins and I_{CHG} is the charge current limit.

The charge is disabled when the I_{LIM} voltage decreases below 70 mV and re-enabled when increases over 90 mV. The I_{LIM} control can be disabled by pulling it to 5 V.

Table 11. Valid battery charge voltage ranges for Li-Ion battery cells

Cells	CHRG_VOLT		Charge voltage [mV]	
	Min.	Max.	Min.	Max.
2	0x1F40	0x2338	8000	9016
3	0x2EE0	0x34D4	12000	13524
4	0x3E80	0x4670	16000	18032

Table 12. Valid battery charge voltage ranges for $LiFePO_4$ battery cells

Cells	CHRG_VOLT		Charge voltage [mV]	
	Min.	Max.	Min.	Max.
2	0x1A90	0x1E88	6800	7816
3	0x27D8	0x2DCC	10200	11724
4	0x3520	0x3D10	13600	15632

4.7 Adapter constant power function

The adapter constant power function manages the amount of input current flowing to the system and to the battery during a charging process. If the input current exceeds the chosen input current limit, the PM6613N keeps the input current at the limit decreasing the charging current. In this manner the system load has the priority. As the system load current increases, the charging current linearly decreases down to 0 A. The input current is sensed measuring the differential voltage between ACP and ACN pins where a small resistor is connected. A suggested value is 10 mΩ, and eventually not more than 20 mΩ. Greater values increase the sensitivity and a finer current limit management, but cause a higher power loss and could lead to an overcurrent protection due to a higher voltage ripple. The INPUT_AMP register sets the input current limit through SMBus. Valid ranges are between 128 mA and 16256 mA. Any attempt to write a value outside this range causes the register to be cleared and any charging process to be stopped.

4.8 Input current limit protection

An input current limit protection is integrated into the PM6613N. When the input current, sensed by ACP and ACN pins, reaches 2 A more than the value stored on INPUT_AMP, the internal circuit stops any charging process and sets the AOC bit of the STATUS register. When the fault condition is not more present for 2.5 ms, the charging process is recovered by a soft-start.

4.9 Thermal shutdown

A thermal protection feature is integrated in the PM6613N. If the junction temperature (T_J) exceeds 165 °C, the internal circuitry stops any charging process and the bit TS of STATUS register is set. When T_J falls below 145 °C, the charger exits from the fault condition and after 2.5 ms the charging process resumes by a soft-start.

4.10 Battery protection

Several protection features disable the charging process if the battery condition falls in one of the following conditions:

- battery undervoltage
- battery overvoltage
- battery overcurrent

A voltage fault is detected sensing the battery voltage on SRN pin. A battery undervoltage condition occurs when the SRN voltage is below 2.5 V: the LB bit of the STATUS register is set. A battery overvoltage occurs when SRN voltage exceeds the charging voltage according to the *Table 13*:

Table 13. Battery overvoltage detection ranges

Battery type	Overvoltage threshold
Li-Ion	CHRG_VOLT[mV]+170 mV* cells
Li-$FePO_4$	CHRG_VOLT[mV]+144 mV* cells

Battery current is sensed by the current flowing through a small resistor connected between SRP and SRN pins. An overcurrent condition occurs when the battery average current exceeds the value set in the CHRG_AMP register by 2 A: the BOC bit of the STATUS register is set.

4.11 Adapter insertion

When the ACDIV pin has a voltage under the $ACDIV_{SLP}$ (see *Table 14*), the PM6613N is in sleep mode. If BSE of CHRG_OPT register is set, the BATFET selector is kept closed, allowing the battery to supply the system. When the adapter is inserted, the ACDIV pin voltage rises, and when it reaches a 0.65 V threshold, the PM6613N goes out of the sleep mode. When the ACDIV pin reaches 2 V threshold, an internal comparator monitors this condition for a programmable deglitch time, set to 250 ms at power-on reset. If the condition is stable after this time, the ACOK pin goes high. This time can be reduced setting the AD bit

of CHRG_OPT register. When ACOK is high, the ACFET selector has to be switched on, in order to supply the B2B pin. This pin is used to provide the offset for the charge pump that supplies the ACFET/RBFET selectors. Once B2B reaches the 2.5 V threshold, the BATFET selector is switched off and the battery is disconnected from the system: in this case the current flows to the system through the body diode of the selector. When the B2B pin crosses the battery voltage (sensed by SRN pin) by 255 mV, the RBFET is switched ON. From now on the system is supplied by the adapter. The described sequence is summarized in the below table:

Table 14. Adapter insertion sequence

Condition	Action
Adapter insertion	ACDIV voltage rises
ACDIV > 0.65 V	PM6613N goes out of sleep mode B2B pin forces a low voltage
ACDIV > 2 V	ACOK pin goes high after 250 ms B2B pin stops forcing voltage
ACFET is turned on	B2B voltage rises
B2B > 2.5 V	BATFET is off
B2B > SRN+225 mV	ACFET/RBFET is on

4.12 Adapter removal

When the adapter is unplugged, a disconnection sequence occurs, bringing the charger into a sleep mode. When the ACDIV pin goes below 1.95 V, the ACOK pin goes immediately low: there's no deglitch time in this case. Any charging process is interrupted and the B2B pin is internally discharged. The B2B pin is used to sense the system voltage through the ACFET/RBFET selectors. When the B2B pin goes below the value of the battery plus 225 mV, the ACFET/RBFET selectors are opened if SOVR bit of CHRG_OPT is set, and the BATFET selector is closed if the BSE bit of CHRG_OPT is set, allowing the battery to supply the system. As the system voltage is much closer to the battery voltage, any inrush current caused by system capacitors is avoided. When the ACDIV voltage goes below 0.6 V the PM6613N is in sleep mode. The sequence is summarized in *Table 15*

Table 15. Adapter removal sequence

Condition	Action
Adapter unplugged	ACDIV voltage decreases
ACDIV < 1.95 V	ACOK goes low B2B pin forces a low voltage Internal circuitry disables any charging process
B2B < SRN+ 225 mV	ACFET/RBFET selectors opened BATFET selector closed
ACDIV < 0.6 V	The PM6613N is in sleep mode

5 The PM6613N registers

5.1 Charge option register (CHRG_OPT)

Address: 0x12

Reset value: 0x7101

Table 16. CHRG_OPT 0x12

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AD	WD[1:0]		BSE	PF	EFA	EE	AM[1:0]		IS	SOVR	BED	ARED	CF	Res	CI
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw		rw

- Bit 15 AD: ACOK deglitch
  - set by software to enable a delay for the adapter insertion
  - 0: the PM6613N waits for 250 ms for adapter voltage detection
  - 1: the PM6613N waits for a time < 50 µs for adapter voltage detection
- Bit [14:13] WD: watchdog
  - set by software to enable and select the timeout of the PM6613N watchdog
  - 00: watchdog disabled
  - 01: enabled, timeout at 44 sec.
  - 10: enabled, timeout at 88 sec.
  - 11: enabled, timeout at 175 sec.
- Bit 12 BSE: BATFET sleep enabled
  - set by software to control the BATFET selector behavior, when the PM6613N is in sleep mode
  - 0: BATFET disabled during sleep mode
  - 1: BATFET enabled during sleep mode
- Bit 11 PF: PWM frequency
  - set by software to select the working PWM frequency of the buck converter
  - 0: PWM frequency set to 700 kHz
  - 1: PWM frequency set to 350 kHz
- Bit 10 EFA: EMI frequency adjustments
  - set by software in order to increase or decrease by 15% the PWM frequency of the buck converter when EE bit is enabled
  - 0: PWM frequency decreased by 15%
  - 1: PWM frequency increased by 15%

- Bit 9 EE: EMI enabled
  - set by software to enable the EMI reduction function
  - 0: EMI disabled
  - 1: EMI enabled
- Bit 8:7 AM: asynchronous mode
  - set by software to choose the average charging current limit for passive recirculation condition
  - 00: 375 mA
  - 01: 750 mA
  - 10: 1125 mA
  - 11: 1500 mA
- Bit 6 IS: IOUT selection
  - set by software to choose which current has to be monitored through the IOUT pin
  - 0: adapter current
  - 1: battery current
- Bit 5 SOVR: selector override
  - set by software to enable the external control of the RBFET/BATFET selectors. Once set, RBFET/BATFET can be controlled by bits 3 and 4
  - 0: override enabled
  - 1: override disabled
- Bit 4 BED: BATFET external driver
  - set by software to control the external selector BATFET. OVR bit has to be set, in order to control BATFET
  - 0: open BATFET
  - 1: close BATFET
- Bit 3 ARED: ACFET/RBFET external driver
  - set by software to control the external selectors ACFET/RBFET. OVR bit has to be set, in order to control ACFET/RBFET
  - 0: open ACFET/RBFET selectors
  - 1: close ACFET/RBFET selectors
- Bit 2 CF: clear fault
  - set by software to clear the STATUS register. The bit is cleared once the process has been executed
  - 0: STATUS register unchanged
  - 1: clear STATUS register
- Bit 1 reserved, read as 0
- Bit 0 CI: charge inhibited
  - set by software to inhibit the charging process
  - 0: charge enabled
  - 1: charge inhibited

5.2 STATUS register

Address: 0x13

Reset value: 0x0000

Table 17. Status 0x13

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					TS	HBRO	RBSS	AOC	IOC	BOV	BOC	LB	AOV	AUV	HS
					r	r	r	r	r	r	r	r	r	r	r

- Bit 15:11 reserved, read as 0
- Bit 10 TS: thermal shutdown
  - set by hardware to indicate that thermal shutdown condition occurred on the PM6613N. Thermal shutdown occurs when the junction temperature (T_j) is higher than 165 °C. It's cleared by hardware when T_j drops below 145 °C.
- Bit 9 HBRO: HS BTST RBFET open
- Bit 8 RBSS: RBFET selector short
  - set by hardware to indicate a short on RBFET between drain and source
  - 0: no short detected
  - 1: short detected
- Bit 7 AOC: adapter overcurrent
  - set by hardware to indicate that the adapter current is 2 A higher than the value
- Bit 6 OC: I_{LIM} overcurrent
  - set by hardware when input current crosses the input limit set by INPUT_AMP register and ILIM pin
  - 0: no input overcurrent detected
  - 1: input overcurrent detected
- Bit 5 BOV: battery overvoltage
  - set by hardware when the PM6613N detects a battery voltage (SRN pin) higher than the value reported on *Table 13*
  - 0: no battery overvoltage detected
  - 1: battery overvoltage detected
- Bit 4 BOC: battery overcurrent
  - set by hardware when the PM6613N detects a current flowing through the battery, 2 A higher than the value set on CHRG_AMP register
  - 0: no battery overcurrent detected
  - 1: battery overcurrent detected
- Bit 3 LB: low battery
  - set by hardware when the PM6613N detects a battery voltage (SRN pin) lower than 2.5 V
  - 0: no low battery condition detected
  - 1: low battery condition detected

- Bit 2 AOV: ACDIV overvoltage
  - set by hardware when the PM6613N detects an ACDIV pin voltage higher than 2.625 V
  - 0: no ACDIV overvoltage detected
  - 1: ACDIV overvoltage detected
- Bit 1 AUV: ACDIV undervoltage
  - set by hardware when the PM6613N detects an ACDIV pin voltage lower than 2 V
  - 0: no ACDIV undervoltage detected
  - 1: ACDIV undervoltage detected
- Bit 0 HS: high-side short
  - set by hardware when a short condition is detected between drain and source of the high-side MOS
  - 0: no short detected on high-side MOS
  - 1: short detected on high-side MOS

5.3 Charge current register (CHRG_AMP)

Address: 0x14

Reset value: 0x0000

Table 18. CHRG_AMP 0x14

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		AMP[13:6]								Reserved					
		rw	rw	rw	rw	rw	rw	rw	rw						

- Bits 13:6 AMP[13:6]: charge current configuration bits
  - these bits are written by software and fix the amount of current to be delivered when battery is charging. Values are in mA. The range goes from 64 mA when AMP[13:6] = 0x0040 to 16320 mA when AMP[13:6] = 0x3FC0. Minimum step is 64 mA.

5.4 Charge voltage register (CHRG_VOLT)

Address: 0x15

Reset value: 0x0000

Table 19. CHRG_VOLT 0x15

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	VOLT[14:1]														Res
	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	

- Bits 14:1 VOLT[14:1]: charge voltage configuration bits
  - these bits are written by software and fix the voltage to apply to the battery when it is charging. Values are in mV and set according to the following formula:

Equation 2

$$V_{BAT} = (2 \cdot 2^{VOLT[14 \div 1]})mV$$

Not all the values are allowed. See *Table 11* and *Table 12* for allowable ranges.

5.5 Input current register (INPUT_AMP)

Address: 0x3F

Reset value: 0x2000

Table 20. INPUT_AMP 0x3F

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		AMP[13:7]							Reserved						
		rw	rw	rw	rw	rw	rw	rw							

- Bits 13:7 AMP[13:7]: charge current configuration bits
  - these bits are written by software and fix the current limit delivered by the adapter. The range goes from 128 mA when AMP[13:6] = 0x0080 to 16256 mA when AMP[13:6] = 0x3F80. Minimum step is 128 mA.

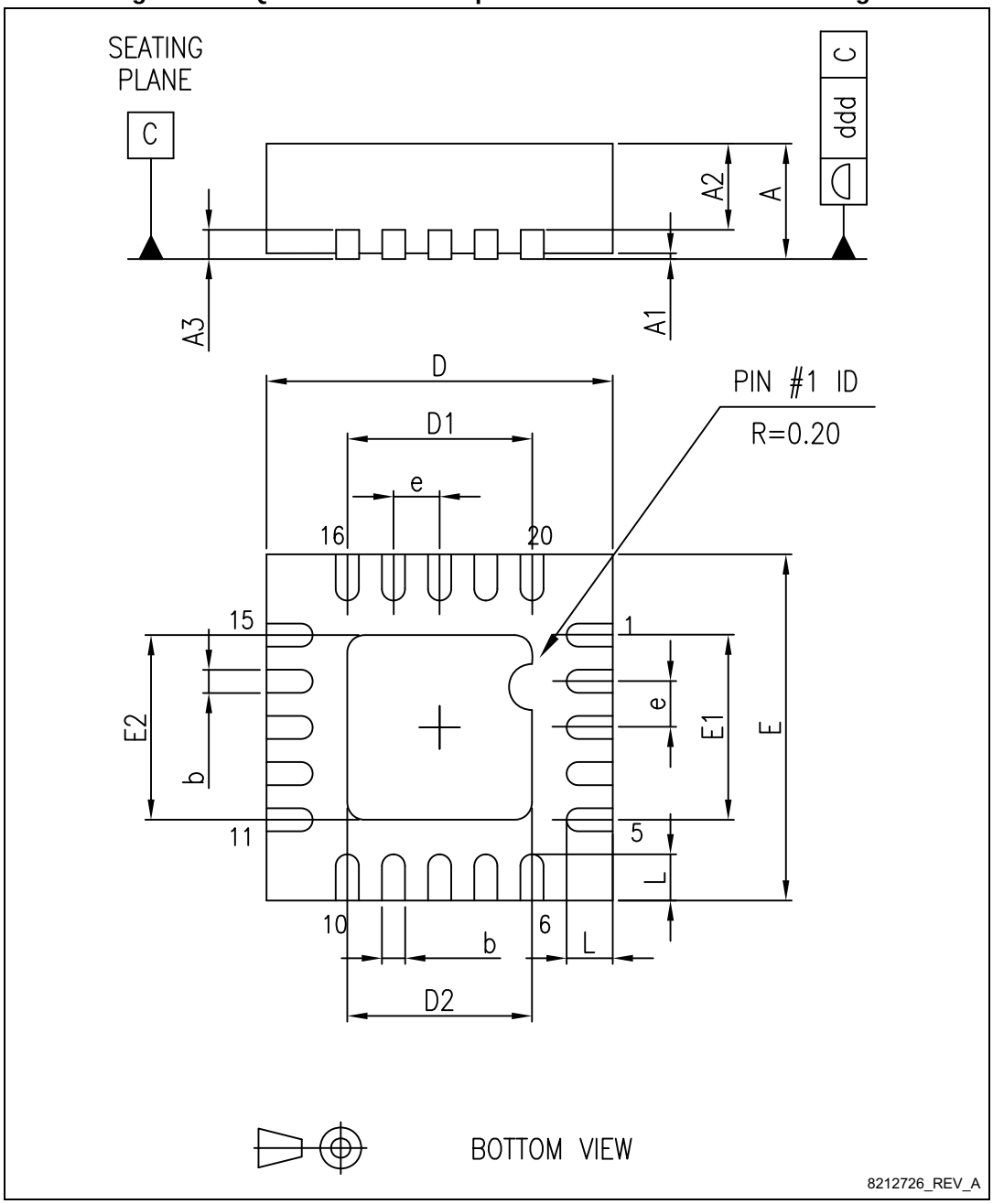
6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 21. VFQFPN 3x3x1.0 20 L pitch 0.4 package dimensions

Ref.	Min.	Typ.	Max.
A	0.8	0.90	1.00
A1		0.02	0.05
A2		0.65	1.00
A3		0.20	
b	0.15	0.20	0.25
D	2.85	3.00	3.15
D1		1.60	
D2	1.50	1.60	1.70
E	2.85	3.00	3.15
E1		1.60	
E2	1.50	1.60	1.70
e	0.35	0.40	0.45
L	0.30	0.40	0.50
ddd			0.07

Figure 5. VFQFPN 3x3x1.0 20 L pitch 0.4 mechanical data drawings



7 Revision history

Table 22. Document revision history

Date	Revision	Changes
23-Jul-2013	1	Initial release.
25-Sep-2013	2	Updated, in *Table 5: Electrical characteristics*, the following parameters: I_{OP}, $ACDIV_{TH}$, V_{BATT_ERR}, I_{CHG_ERR}, $I_{ADP\_G\_ERR}$, $I_{BATT\_G\_ERR}$ and I_{BATT_SRC}. Datasheet status promoted from preliminary to production data.
27-Nov-2013	3	Changed the value of charge voltage accuracy from 0.5% to 1.53% in the features. Updated light load comparator, battery fault comparators, t_{R_ACOK} and f_{SW} test conditions in *Table 5: Electrical characteristics*. Updated I_{BATT_OC} and I_{ADP_OC} parameters in *Table 5: Electrical characteristics*. Updated *Table 7: Recommended operating conditions*. Changed the title of *Table 16*, *Table 17*, *Table 18*, *Table 19* and *Table 20*.

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