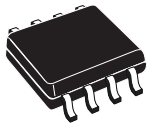
STS5DNF20V

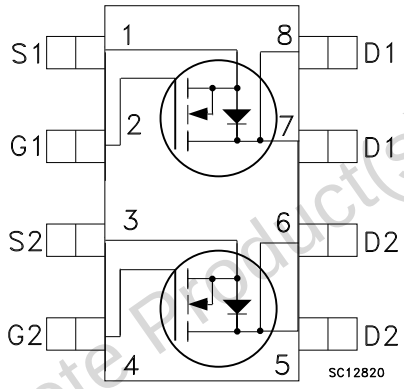
N-channel 20 V, 0.030 Ω typ, 5 A STripFET™ II Power MOSFET in a SO-8 package

Datasheet - production data



SO-8

Figure 1. Internal schematic diagram



Features

Order code	V_{DSS}	$R_{DS(on)}$ max.	I_D
STS5DNF20V	20 V	0.040 Ω @ 4.5 V	5 A
		0.045 Ω @ 2.7 V	

- Ultra low threshold gate drive (2.7 V)
- Standard outline for easy automated surface mount assembly

Applications

- Switching application

Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

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Table 1. Device summary

Order code	Marking	Package	Packaging
STS5DNF20V	5DF20V	SO-8	Tape and reel

This is information on a product in full production. www.st.com

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	20	V
V_{GS}	Gate-source voltage	±12	V
I_D	Drain current (continuous) at T_C = 25 °C	5	A
I_D	Drain current (continuous) at T_C = 100 °C	3	A
I_{DM} (1)	Drain current (pulsed)	20	A
P_{TOT}	Total dissipation at T_C = 25 °C (dual operation)	1.6	W
P_{TOT}	Total dissipation at T_C = 25 °C (single operation)	2	W
T_J	Max. operating junction temperature	-55 to 150	°C
T_{stg}	Storage temperature		

1. Pulse width limited by safe operating area.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}a}$	Thermal resistance junction-ambient single operation	62.5	°C/W
	Thermal resistance junction-ambient dual operation	78	°C/W

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2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	I_D = 250 µA, V_{GS} = 0	20			V
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0)	V_{DS} = 20			1	µA
		V_{DS} = 20 V, T_C=125 °C			10	µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 12 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.6			Ω
$R_{DS(on)}$	Static drain-source on- resistance	V_{GS} = 4.5 V, I_D = 2.5 A		0.030	0.040	Ω
		V_{GS} = 2.7 V, I_D = 2.5 A		0.037	0.045	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	460		pF
C_{oss}	Output capacitance		-	200		pF
C_{rss}	Reverse transfer capacitance		-	50		pF
Q_g	Total gate charge	V_{DD} = 16 V, I_D = 5 A, V_{GS} = 4.5 V (see *Figure 13*)	-	8.5	11.5	nC
Q_{gs}	Gate-source charge		-	1.8		nC
Q_{gd}	Gate-drain charge		-	2.4		nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}=10 V, I_D=2.5A, R_G=4.7Ω, V_{GS}= 4.5V (see *Figure 12*)	-	7	-	ns
t_r	Rise time		-	33	-	ns
$t_{d(off)}$	Turn-off delay time		-	27	-	ns
t_f	Fall Time		-	10	-	ns

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Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		5	A
I_{SDM} (1)	Source-drain current (pulsed)		-		20	A
V_{SD} (2)	Forward on voltage	I_{SD} = 5 A, V_{GS} = 0	-		1.2	V
t_{rr}	Reverse recovery time	I_{SD} = 5 A, V_{DD} = 10 V, di/dt = 100 A/µs, T_j = 150 °C (see *Figure 14*)	-	26		ns
Q_{rr}	Reverse recovery charge		-	13		nC
I_{RRM}	Reverse recovery current		-	1		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

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2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

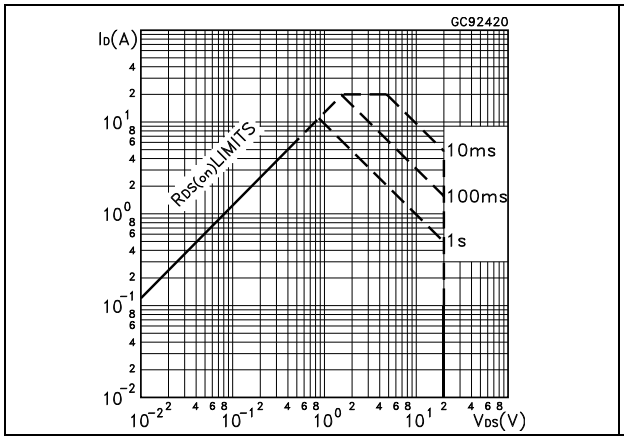

Figure 3. Thermal impedance

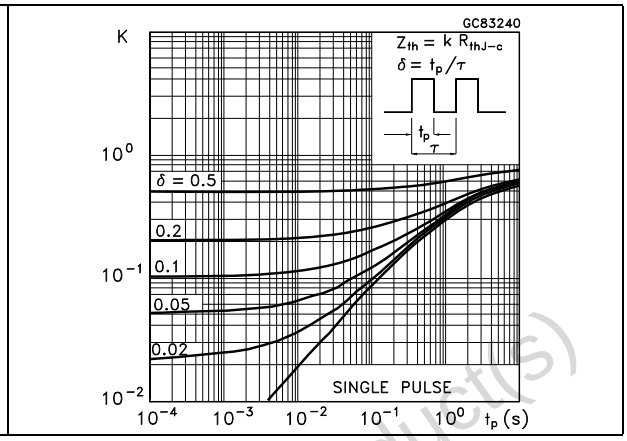

Figure 4. Output characteristics

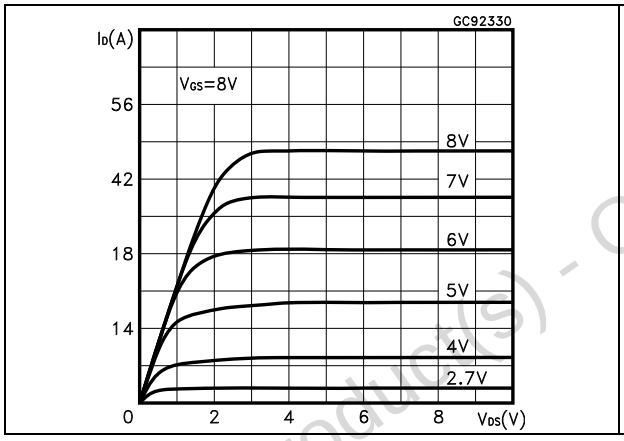

Figure 5. Transfer characteristics

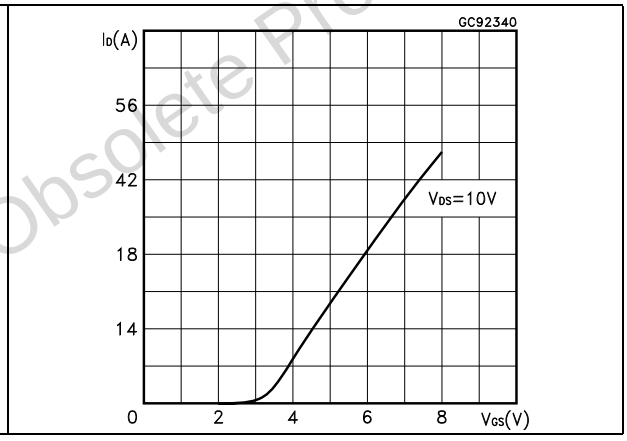

Figure 6. Source-drain diode forward characteristics

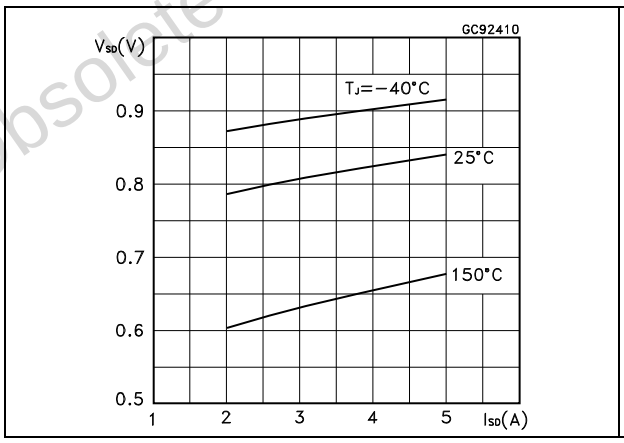

Figure 7. Static drain-source on resistance

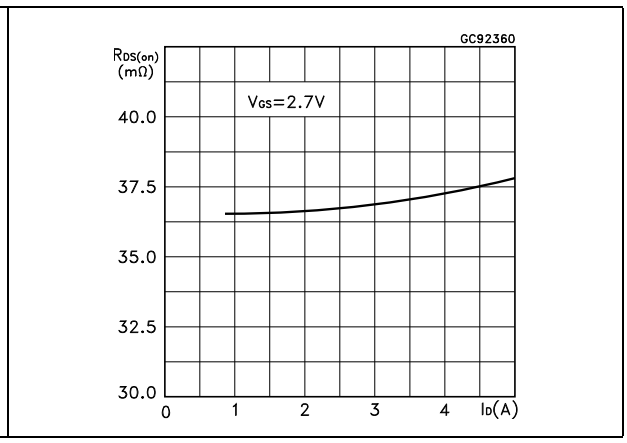

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Figure 8. Gate charge vs gate-source voltage

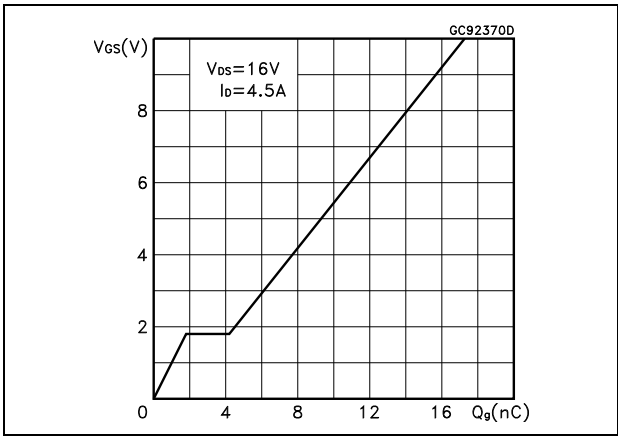


Figure 9. Capacitance variations

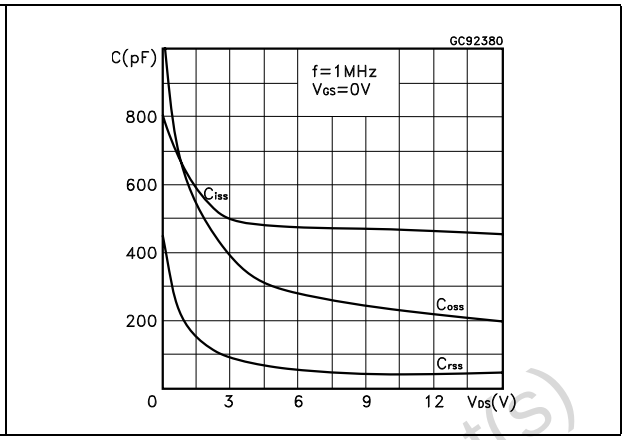


Figure 10. Normalized gate threshold voltage vs temperature

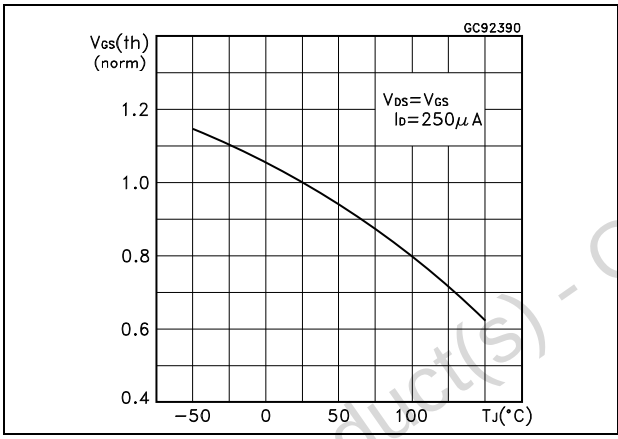
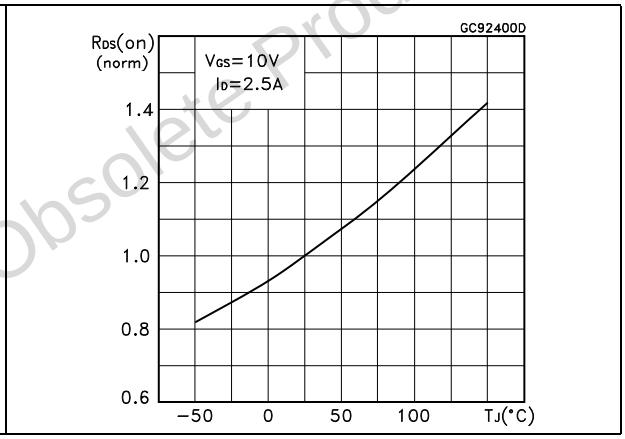


Figure 11. Normalized on-resistance vs temperature



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3 Test circuit

Figure 12. Switching times test circuit for resistive load

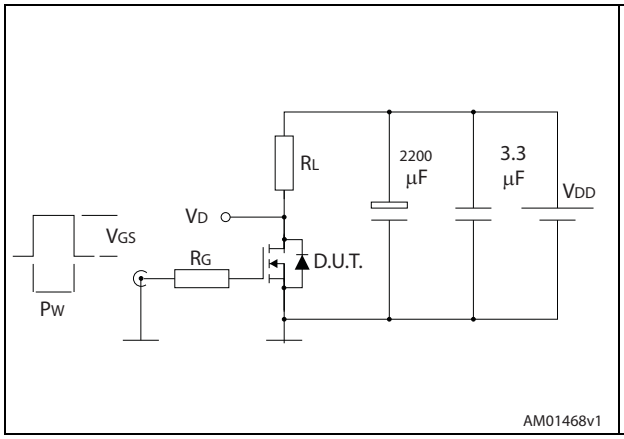


Figure 13. Gate charge test circuit

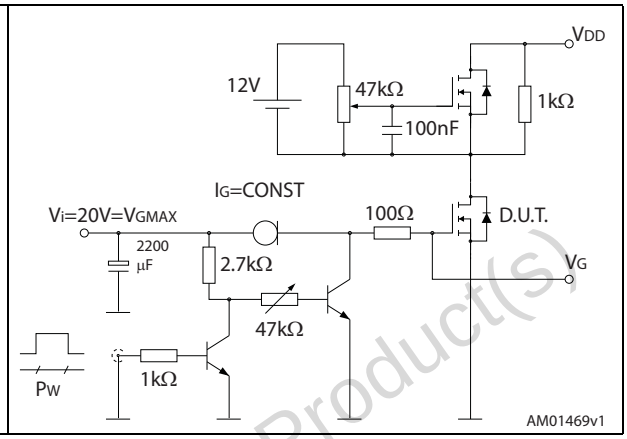


Figure 14. Test circuit for inductive load switching and diode recovery times

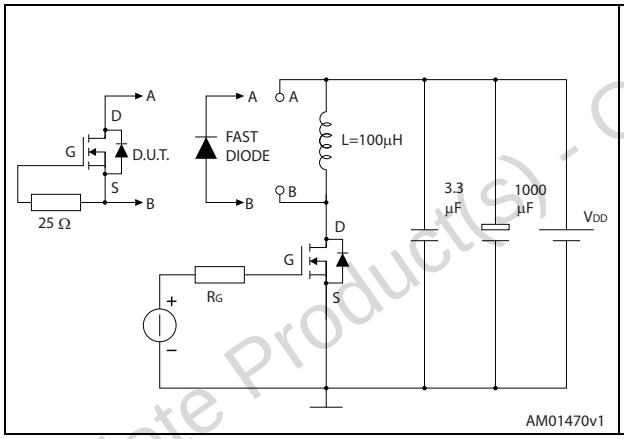


Figure 15. Unclamped Inductive load test circuit

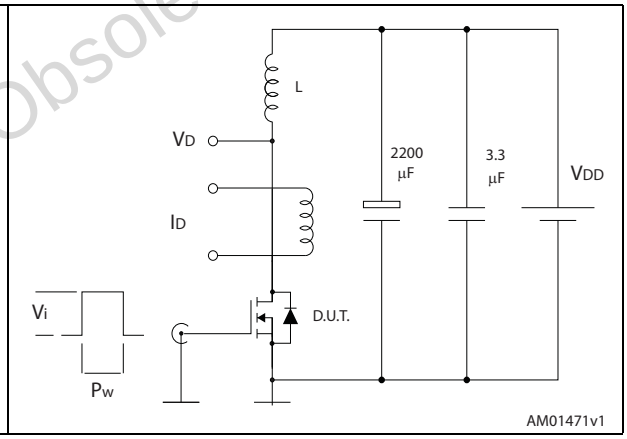


Figure 16. Unclamped inductive waveform

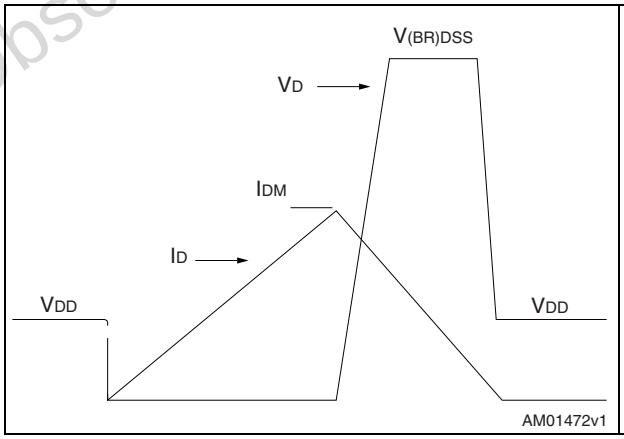
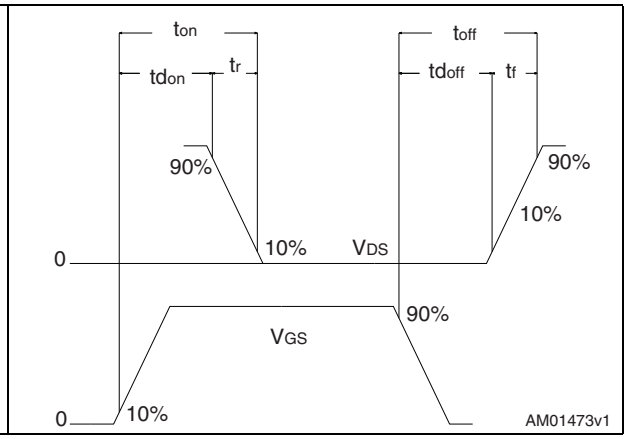


Figure 17. Switching time waveform



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4 Package mechanical data

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Figure 18. SO-8 drawing

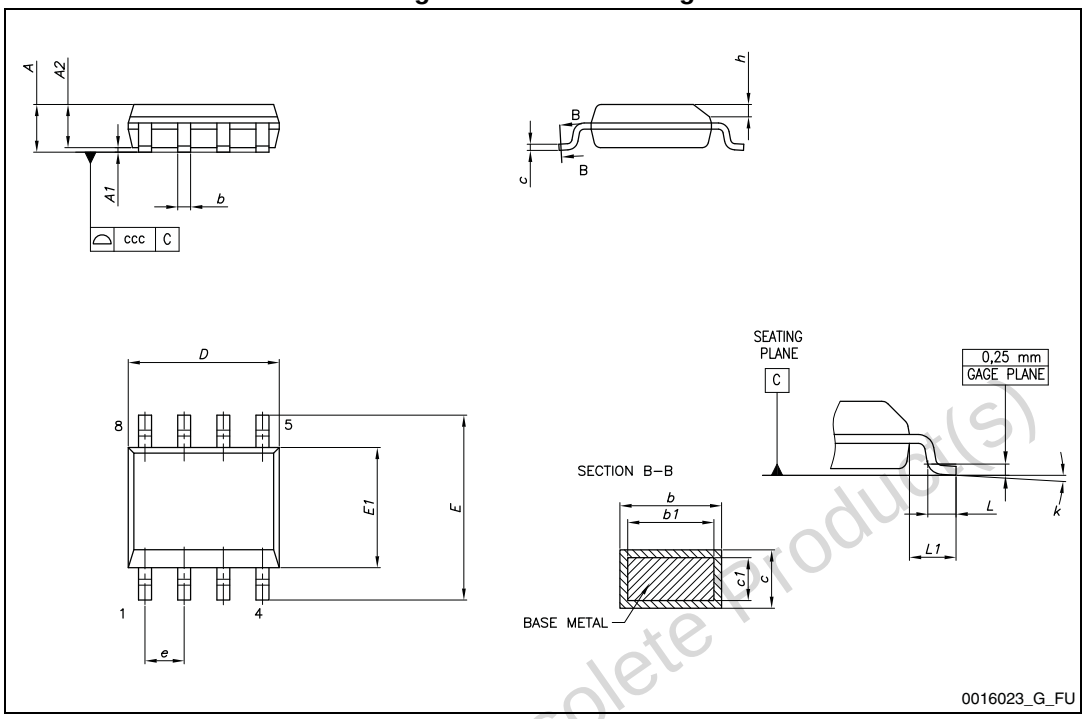

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Table 8. SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

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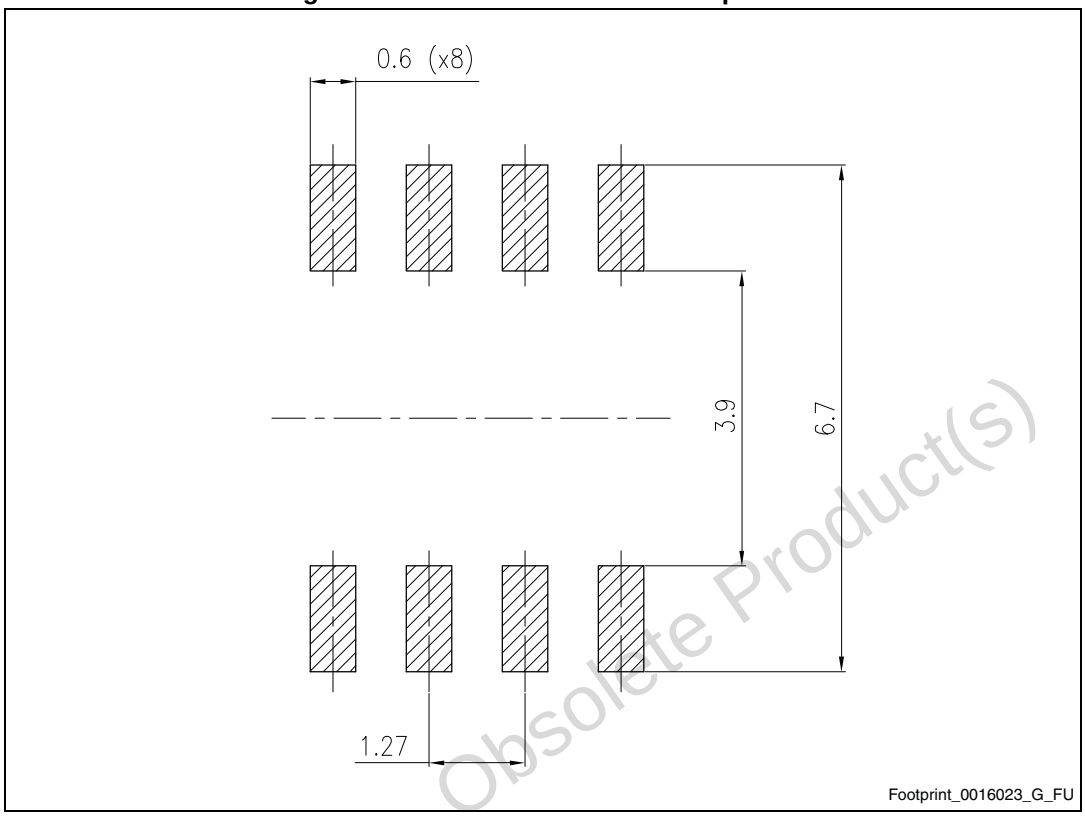
Figure 19. SO-8 recommended footprint[(a)]



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a. All dimensions are in millimeters.

5 Revision history

Table 9. Revision history

Date	Revision	Changes
21-Jun-2004	4	Complete document
13-Nov-2006	5	The document has been reformatted
02-May-2011	6	*Table 1: Device summary* has been corrected
06-Mar-2014	7	Modified: Marking in *Table 1* Updated: *Section 4: Package mechanical data*, *Figure 12: Switching times test circuit for resistive load*, *Figure 13: Gate charge test circuit*,*Figure 14: Test circuit for inductive load switching and diode recovery times* and *Figure 15: Unclamped Inductive load test circuit*. Minor text changes.

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