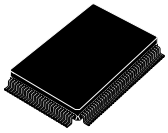
STE10/100A

PCI 10/100 Ethernet controller with integrated PHY (3.3V)

Features

- IEEE802.3u 100BASE-TX and IEEE802.3 10BASE-T compliant
- Support for IEEE802.3x flow control
- IEEE802.3u auto-negotiation support for 10BASE-T and 100BASE-TX
- PCI bus interface rev. 2.2 compliant
- ACPI and PCI power management standard compliant
- Support for PC99 wake on LAN
- Provides 32-bit PCI bus master data transfer at PCI clocks of 20-33 MHz
- Provides writable EEPROM/Boot rom interface
- Provides independent transmission and receiving FIFOs, each 2k bytes long
- Supports big endian or little endian byte ordering
- ACPI and PCI compliant power management functions offer significant power-savings performance
- Provides general purpose timers
- 128-pin QFP package



PQFP128 (14mm x 20mm x 2.7mm)

Description

The STE10/100A is a high performing PCI fast ethernet controller with integrated physical layer interface for 10BASE-T and 100BASE-TX applications.

It was designed with advanced CMOS technology to provide glueless 32-bit bus master interface for PCI bus, boot ROM interface, CSMA/CD protocol for fast ethernet, as well as the physical media interface for 100BASE-TX of IEEE802.3u and 10BASE-T of IEEE802.3. The auto-negotiation function is also supported for speed and duplex detection.

The STE10/100A provides both half-duplex and full-duplex operation, as well as support for full-duplex flow control. It provides long FIFO buffers for transmission and receiving, and early interrupt mechanism to enhance performance. The STE10/100A also supports ACPI and PCI compliant power management function

Contents

1 Overview

1.1 Block diagrams

Figure 1. STE10/100A block diagram

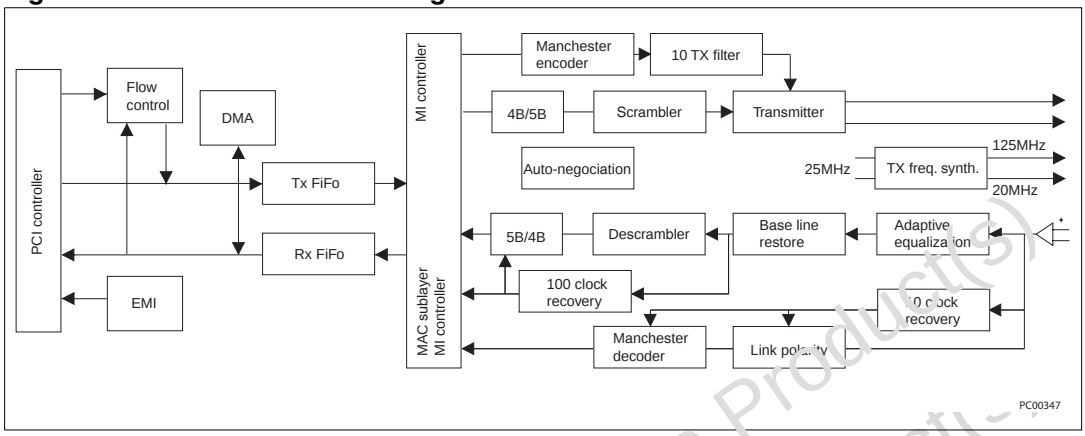
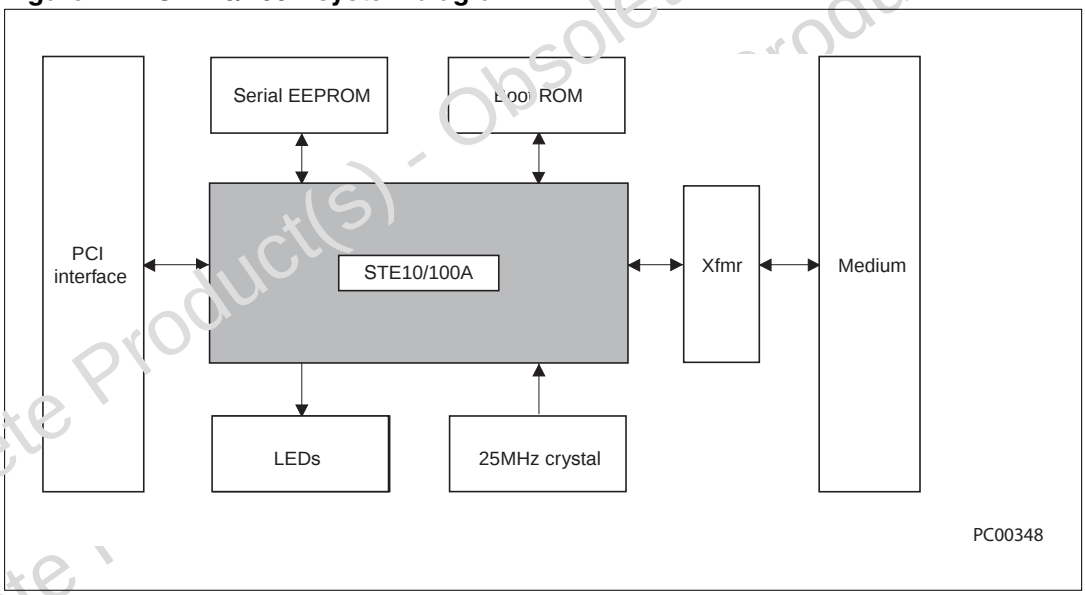


Figure 2. STE10/100A system diagram



1.2 Detailed features

FIFO

- Provides independent transmission and receiving FIFOs, each 2k bytes long
- Pre-fetches up to two transmit packets to minimize inter frame gap (IFG) to 0.96us
- Retransmits collided packet without reload from host memory within 64 bytes.
- Automatically retransmits FIFO under-run packet with maximum drain threshold until 3rd time retry failure threshold of next packet.

PCI interface

- Provides 32-bit PCI bus master data transfer
- Supports PCI clock with frequency from 0Hz to 33MHz
- Supports network operation with PCI system clock from 20MHz to 33MHz
- Provides performance meter and PCI bus master latency timer for tuning the threshold to enhance the performance
- Provides burst transmit packet interrupt and transmit/receive early interrupt to reduce host CPU utilization
- As bus master, supports memory-read, memory-read-line, memory-read-multiple, memory-write, memory-write-and-invalidate command
- Supports big or little endian byte ordering

EEPROM/Boot ROM interface

- Provides writable flash ROM and EPROM as boot ROM, up to 128Kbit
- Provides PCI to access boot ROM by byte, word, or double word
- Re-writes flash boot ROM through I/O port by programming register
- Provides serial interface for read/write 93C46 EEPROM
- Automatically loads device ID, vendor ID, subsystem ID, subsystem vendor ID, maximum-latency, and minimum-grand from the 64 byte contents of 93C46 after PCI reset de-asserted

MAC/physical

- Integrates the complete set of physical layer 100BASE-TX and 10BASE-T functions
- Provides full-duplex operation in both 100Mbps and 10Mbps modes
- Provides auto-negotiation (NWAY) function of full/half duplex operation for both 10 and 100 Mbps
- Provides MLT-3 transceiver with DC restoration for base-line wander compensation
- Provides transmit wave-shaper, receive filters, and adaptive equalizer
- Provides MAC and transceiver (TXCVR) loop-back modes for diagnostic
- Built-in stream cipher scrambler/ de-scrambler and 4B/5B encoder/decoder
- Supports external transmit and receive transformer with 1:1 turn ratio

LED display

- Provides 2 LED display modes:
  - 3 LED displays for

    100Mbps (on) or 10Mbps (off) link (remains on when link ok) or activity (Blinks at 10Hz when receiving or transmitting collision-free) FD (Remains on when in full duplex mode) or when collision detected (Blinks at 20Hz)
  - 4 LED displays for:

    100 link (On when 100M link ok)
    10 link (On when 10M link ok)
    Activity (Blinks at 10Hz when receiving or transmitting)
    FD (Remains on when in full duplex mode) or when collision detected (Blinks at 20Hz)
- If no LED is used, then: Pull the pins 90, 91, 92 of U4 to high with 4.7K resistor (see STE10/100A evaluation board schematics for details)

2 Pin description

Figure 3. Pin connection

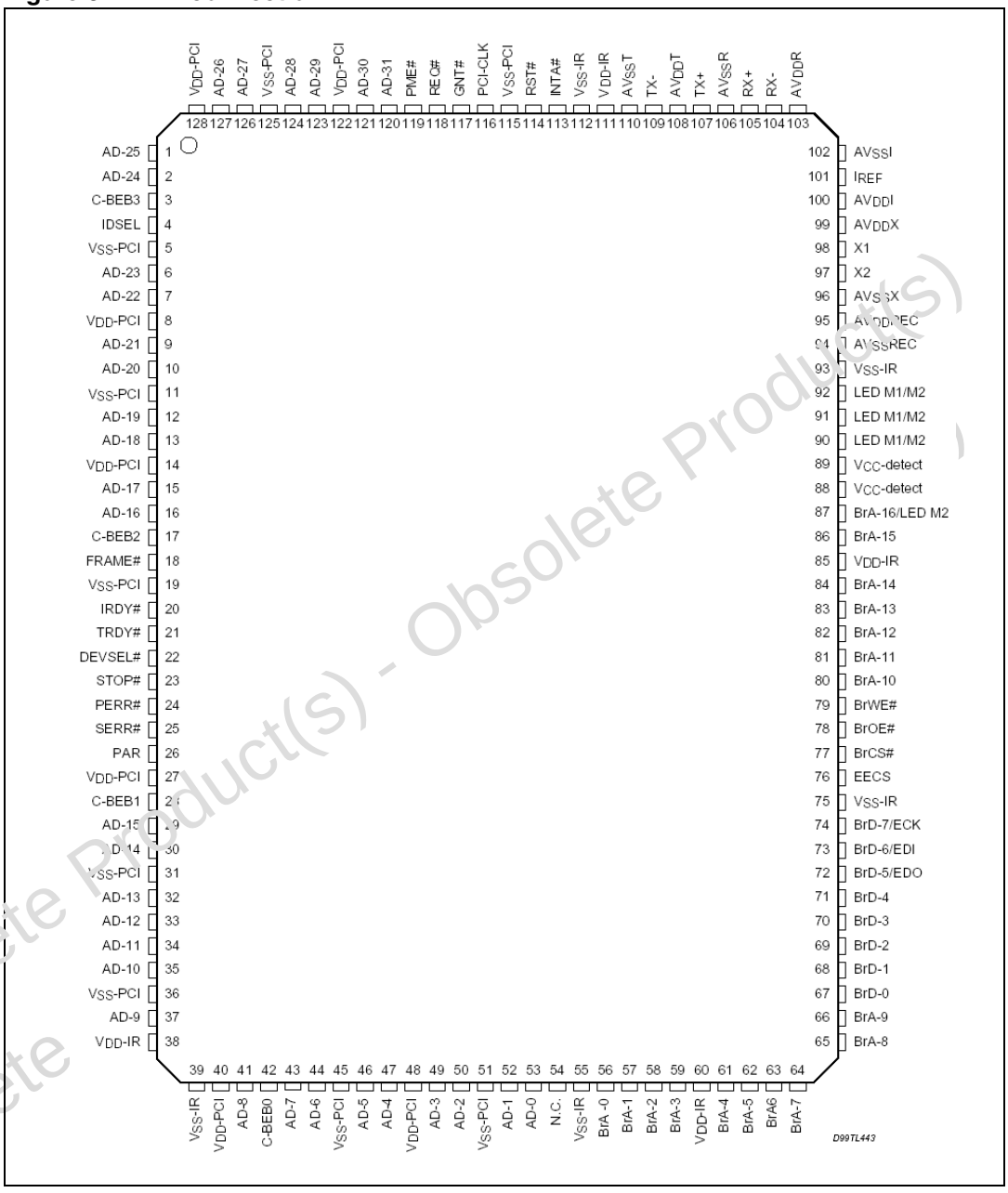


Table 1. Pin description

Pin no.	Name	Type	Description
PCI bus interface			
113	INTA#	O/D	PCI interrupt request. STE10/100A asserts this signal when one of the interrupt event is set.
114	RST#	I	PCI reset signal to initialize the STE10/100A. The RST signal should be asserted for at least 100µs to ensure that the STE10/100A completes initialization. During the reset period, all the output pins of STE10/100A will be placed in a high-impedance state and all the O/D pins are floated.
116	PCI-CLK	I	PCI clock input to STE10/100A for PCI bus functions. The Bus signals are synchronized relative to the rising edge of PCI-CLK PCI-CLK must operate at a frequency in the range between 20MHz and 33MHz to ensure proper network operation.
117	GNT#	I	PCI bus granted. This signal indicates that the STE10/100A has been granted ownership of the PCI bus as a result of a bus request.
118	REQ#	O	PCI bus request. STE10/100A asserts this line when it needs access to the PCI Bus.
119	PME#	O O/D	The power management event signal is an open drain, active low signal. The STE10/100A will assert PME# to indicate that a power management event has occurred. When WOL (bit 18 of CSR18) is set, the STE10/100A is placed in wake on LAN mode. While in this mode, the STE10/100A will activate the PME# signal upon receipt of a magic packet frame from the network. In the wake on LAN mode, when LWS (bit 17 of CSR18) is set, the LAN-wake signal follows HP's protocol; otherwise, it is IBM protocol.
120,121 123,124 126,127 1,2 6,7 9,10 12,13 15,16 29,30 32~35 37 41 43,44 46,47 49,50 52,53	AD-31,30 AD-29,28 AD-27,26 AD-25,24 AD-23,22 AD-21,20 AD-19,18 AD-17,16 AD-15,14 AD-13~10 AD-9 AD-8 AD-7, 6 AD-5,4 AD-3,2 AD-1,0	I/O	Multiplexed PCI bus address/data pins

Table 1. Pin description (continued)

Pin no.	Name	Type	Description
3 17 28 42	C-BEB3 C-BEB2 C-BEB1 C-BEB0	I/O	Bus command and byte enable
4	IDSEL	I	Initialization device select. This signal is asserted when the host issues configuration cycles to the STE10/100A.
18	FRAME#	I/O	Asserted by PCI bus master during bus tenure
20	IRDY#	I/O	Master device is ready to begin data transaction
21	TRDY#	I/O	Target device is ready to begin data transaction
22	DEVSEL#	I/O	Device select. Indicates that a PCI target device address has been decoded
23	STOP#	I/O	PCI target device request to the PCI master to stop the current transaction
24	PERR#	I/O	Data parity error detected, driven by the device receiving data
25	SERR#	O/D	Address parity error
26	PAR	I/O	Parity. Even parity computed for AD[31:0] and C/BE[3:0]; master drives PAR for address and write data phase, target drives PAR for read data phase.
Boot ROM/EEPROM interface			
56~59 61~66 80~86 87	BrA0~3 BrA4~9 BrA10~15 BrA16/ LED M2 - Fd/Col	I/O	ROM data bus Provides up to 128Kbit EPROM or flash-ROM application space. This pin can be programmed as mode 2 LED display for full duplex or collision status. It will be driven (LED on) continually when a full duplex configuration is detected, or it will be driven at a 20 Hz blinking frequency when a collision status is detected in the half duplex configuration.
67~71 72 73 74	BrD0~4 BrD5/EDO BrD6/EDI BrD7/ECK	O O/I O/O O/O	BootROM data bus (0~7) EDO: Data output of serial EEPROM, data input to STE10/100A EDI: Data input to serial EEPROM, data output from STE10/100A ECK: Clock input to serial EEPROM, sourced by STE10/100A
76	EECS	O	Chip select of serial EEPROM
77	BrCS#	O	BootROM chip select
78	BrOE#	O	BootROM read output enable for flash ROM application
79	BrWE#	O	BootROM write enable for flash ROM application.

Table 1. Pin description (continued)

Pin no.	Name	Type	Description
Physical interface			
98	X1	I	25MHz reference clock input for physical portion. When an external 25MHz crystal is used, this pin will be connected to one of its terminals, and X2 will be connected to the other terminal. If an external 25 MHz oscillator is used, then this pin will be connected to the oscillator's output pin.
97	X2	O	25MHz reference clock output for physical portion. When an external 25MHz crystal is used, this pin will be connected to one of the crystal terminals (see X1, above). If an external clock source is used, then this pin should be left open.
107,109	TX+, TX-	O	The differential transmit outputs of 100BASE-TX or 10BASE-T, these pins connect directly to magnetic.
105,104	RX+, RX-	I	The differential receive inputs of 100BASE-TX or 10BASE-T, these pins connect directly from magnetic.
101	Iref	O	Reference resistor connecting pin for reference current, directly connects a 5KOhm ±1% resistor to Vss.
LED display & miscellaneous			
90	LED M1- LK/Act or LED M2- Act	O	This pin can be programmed as mode 1 or mode 2: For mode 1: LED display for link and activity status. This pin will be driven on continually when a good Link test is detected. This pin will be driven at a 10Hz blinking frequency when either effective receiving or transmitting is detected. For mode 2: LED display for activity status. This pin will be driven at a 10Hz blinking frequency when either effective receiving or transmitting is detected.
92	LED M1- Speed or LED M2- 100 link	O	This pin can be programmed as mode 1 or mode 2: For mode 1: LED display for 100M b/s or 10M b/s speed. This pin will be driven on continually when the 100M b/s network operating speed is detected. For mode 2: LED display for 100Ms/s link status. This pin will be driven on continually when 100Mb/s network operating speed is detected.

Table 1. Pin description (continued)

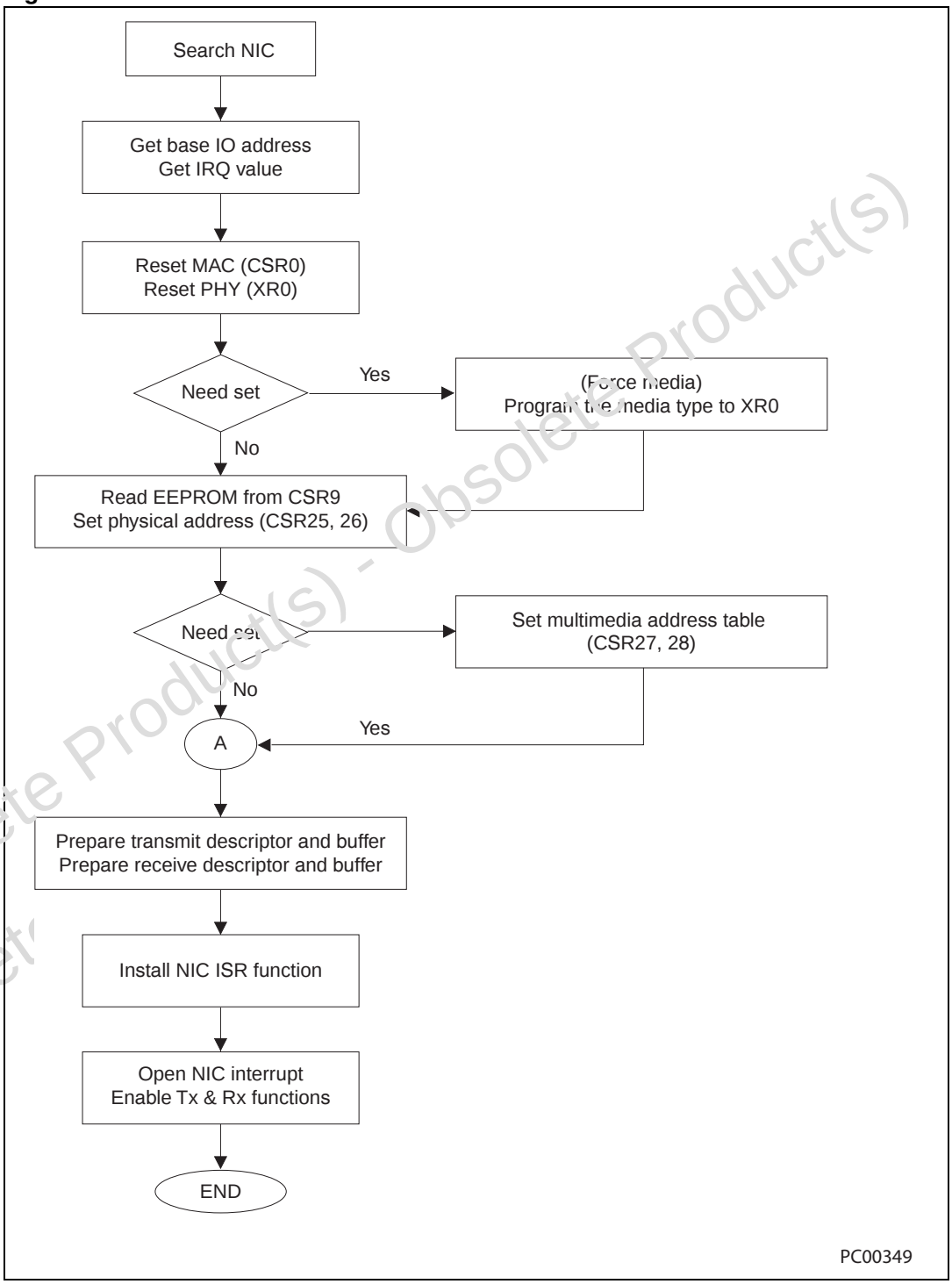
Pin no.	Name	Type	Description
91	LED M1-Fd/Col or LED M2-10 link	O	This pin can be programmed as mode 1 or mode 2: For mode 1: LED display for full duplex or collision status. This pin will be driven on continually when a full duplex configuration is detected. This pin will be driven at a 20 Hz blinking frequency when a collision status is detected in the half duplex configuration. For mode 2: LED display for 10Ms/s link status. This pin will be driven on continually when 10Mb/s network operating speed is detected.
89	Vaux-detect	I	When this pin is asserted, it indicates an auxiliary power source is supported from the system.
88	Vcc-detect	I	When this pin is asserted, it indicates a PCI power source is supported.

Pin no.	Name
Digital power pins	
5,11,19,31,36,39,45,51,55,75,93,112,115,125	Vss
8,14,27,38,40,48,60,85,111,122,128	Vdd
Analog power pins	
94,96,102,106,110	AVss
95,99,100,103,108	AVdd

3 Functional description

3.1 Initialization flow

Figure 4. STE10/100A initialization flow



3.2 Network packet buffer management

3.2.1 Descriptor structure types

During normal network transmit operations, the STE10/100A transfers the data packets from transmit buffers in the host's memory to the STE10/100A's transmit FIFO. For receive operations, the STE10/100A transfers the data packet from its receive FIFO to receive buffers in the host's memory. The STE10/100A makes use of descriptors, data structures which are built in host memory and contain pointers to the transmit and receive buffers and maintain packet and frame parameters, status, and other information vital to controlling network operation.

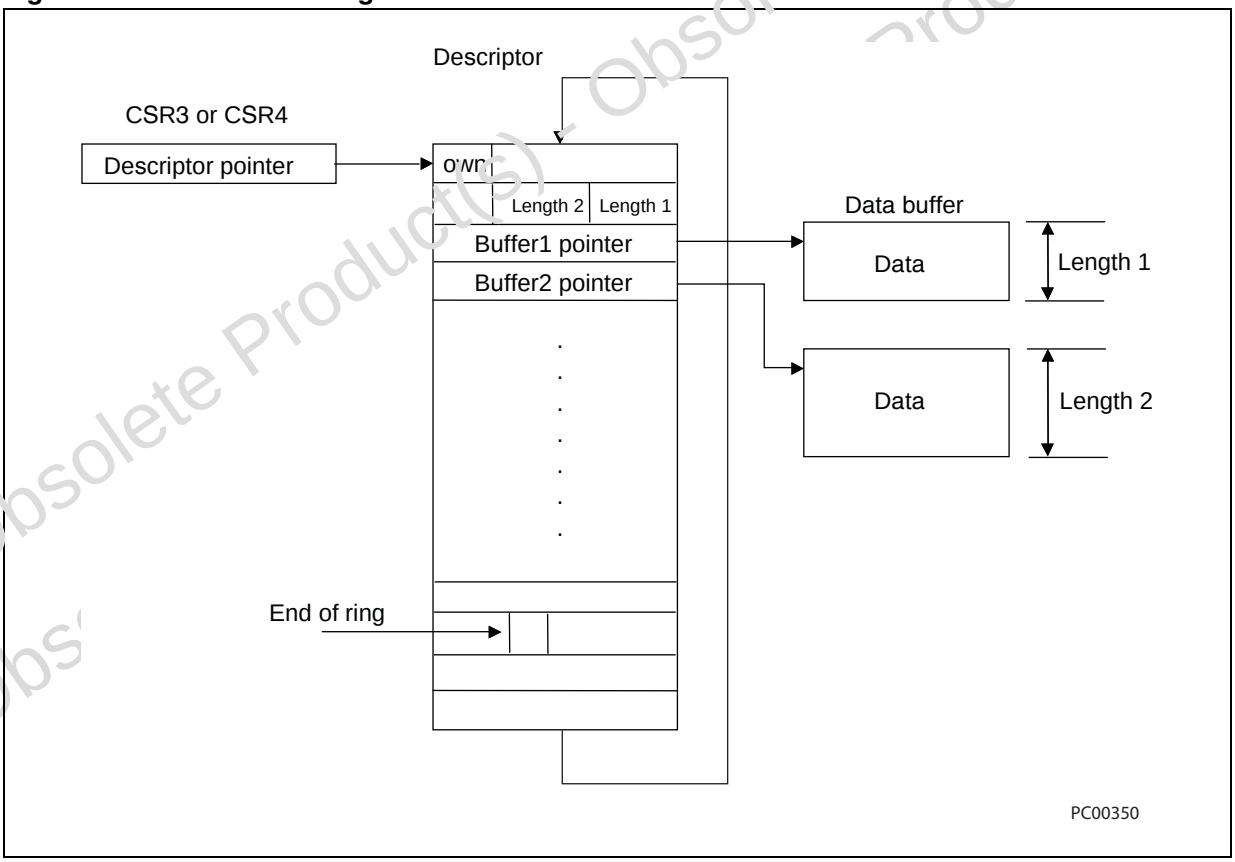
There are two types of structures employed to group descriptors, the **Ring** and the **Chain**, both supported by the STE10/100A and shown below. The selection of structure type is controlled by RCH (RDES1 bit 24) and TCH (TDES1 bit 24).

The transmit and receive buffers reside in the host's memory. Any buffer can contain either a complete or partial packet. A buffer may not contain more than one packet.

Ring structure

There are two buffers per descriptor in the ring structure. Support receive early interrupt.

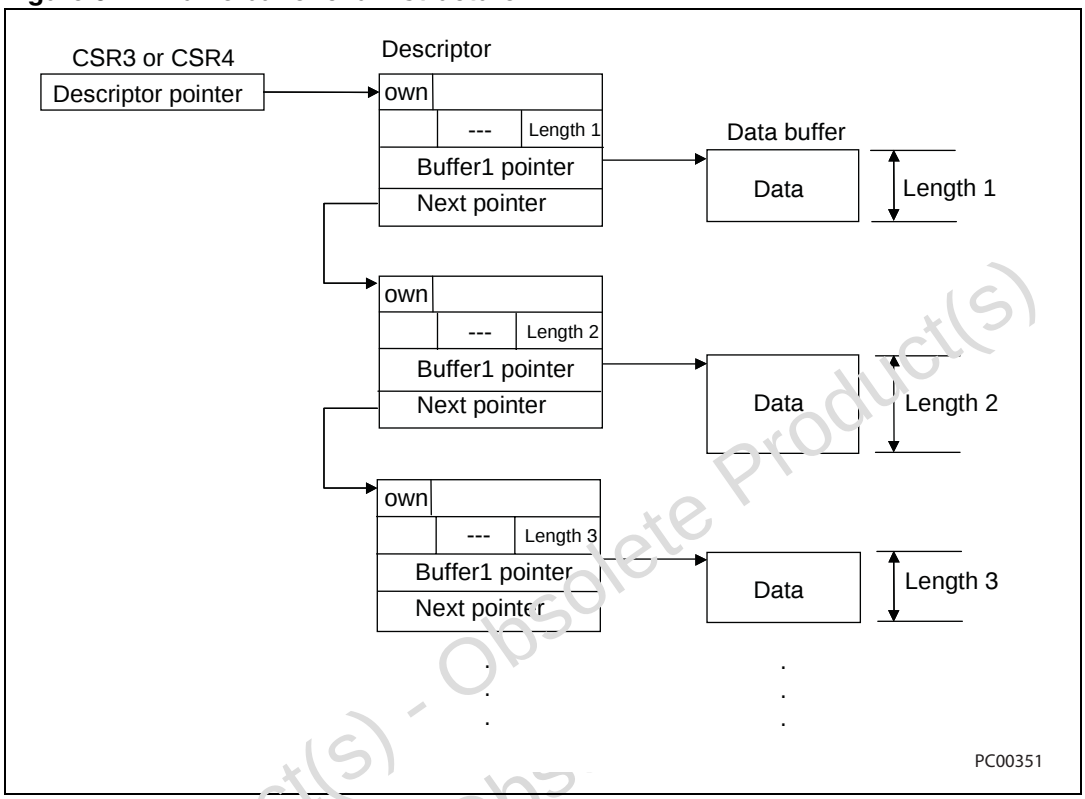
Figure 5. Frame buffer ring structure



Chain structure

There is only one buffer per descriptor in chain structure.

Figure 6. Frame buffer chain structure



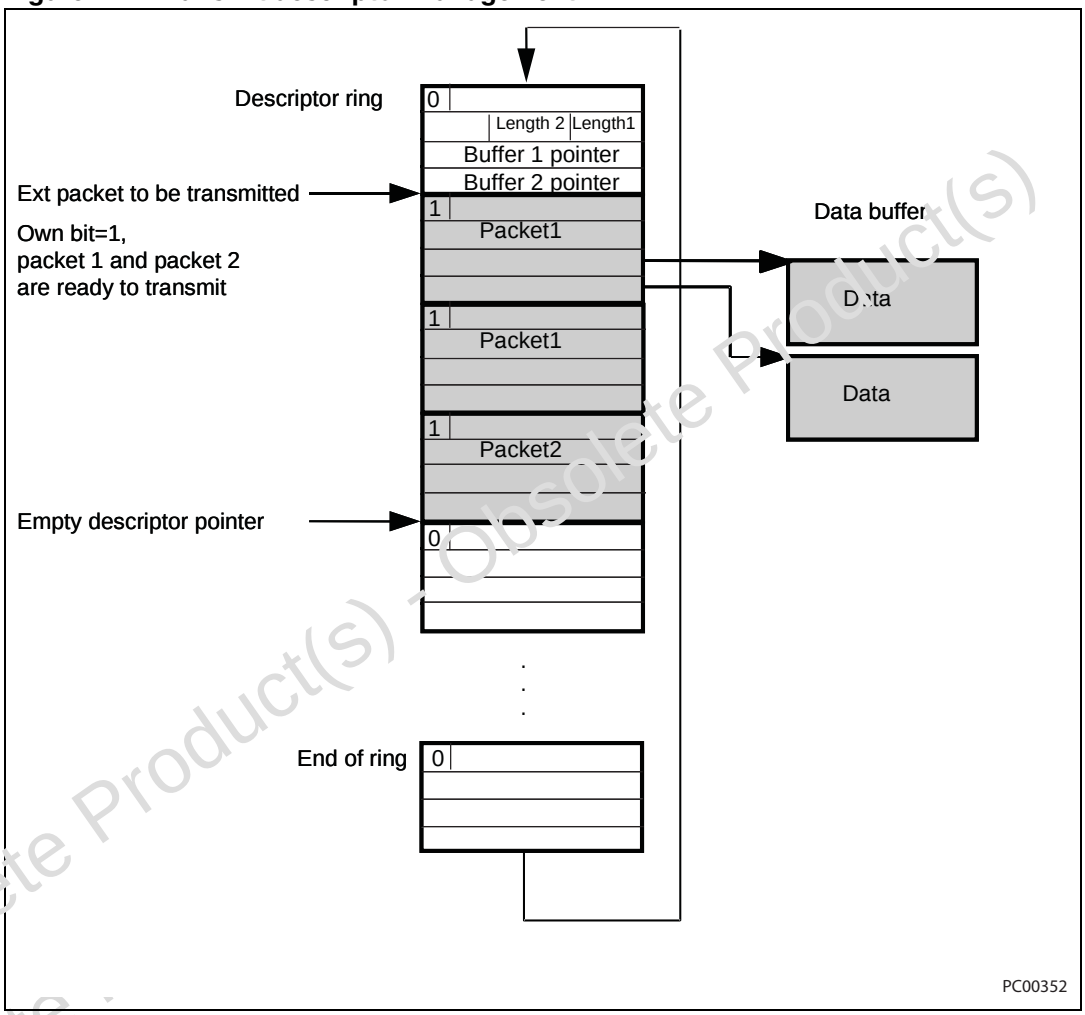
3.2.2 Descriptor management

OWN bit = 1, ready for network side access

OWN bit = 0, ready for host side access

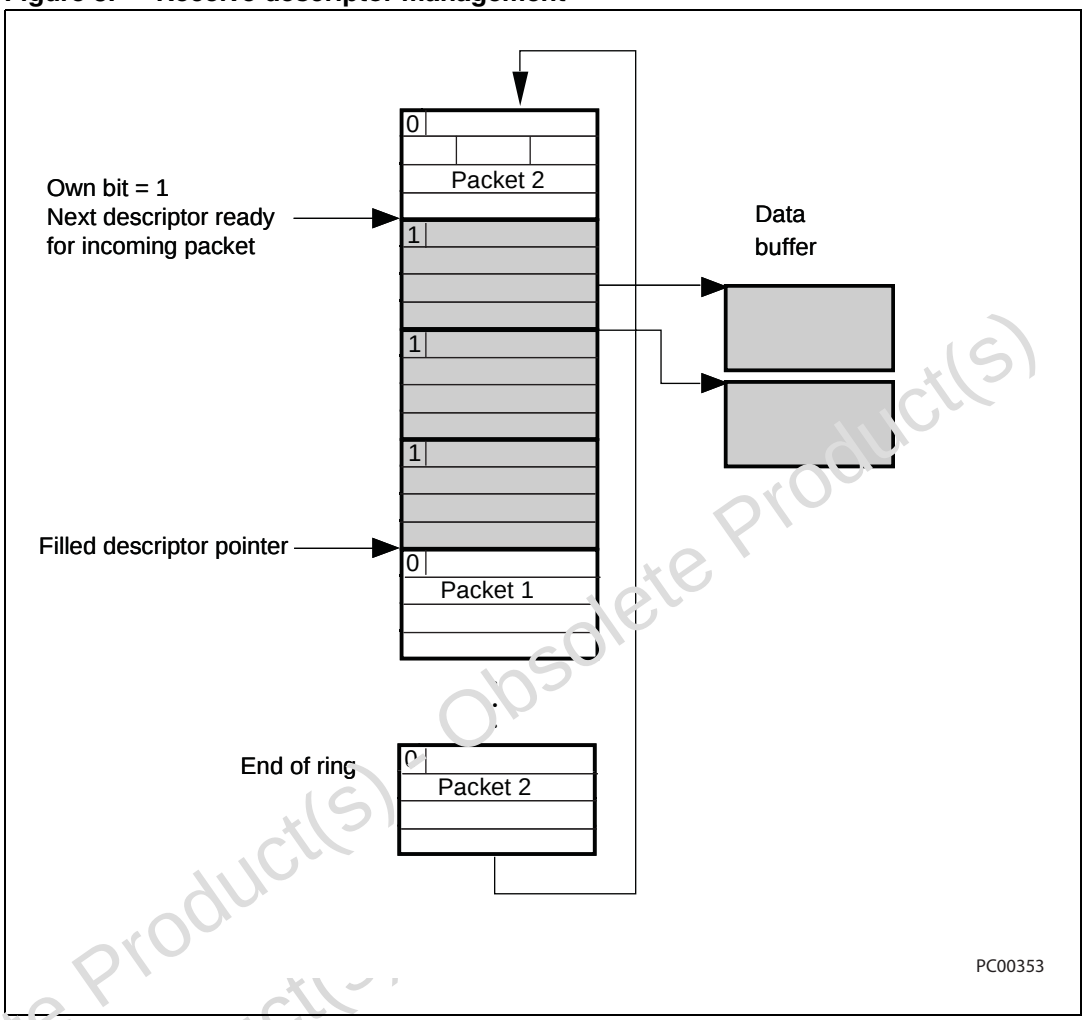
Transmit descriptors

Figure 7. Transmit descriptor management



Receive descriptors

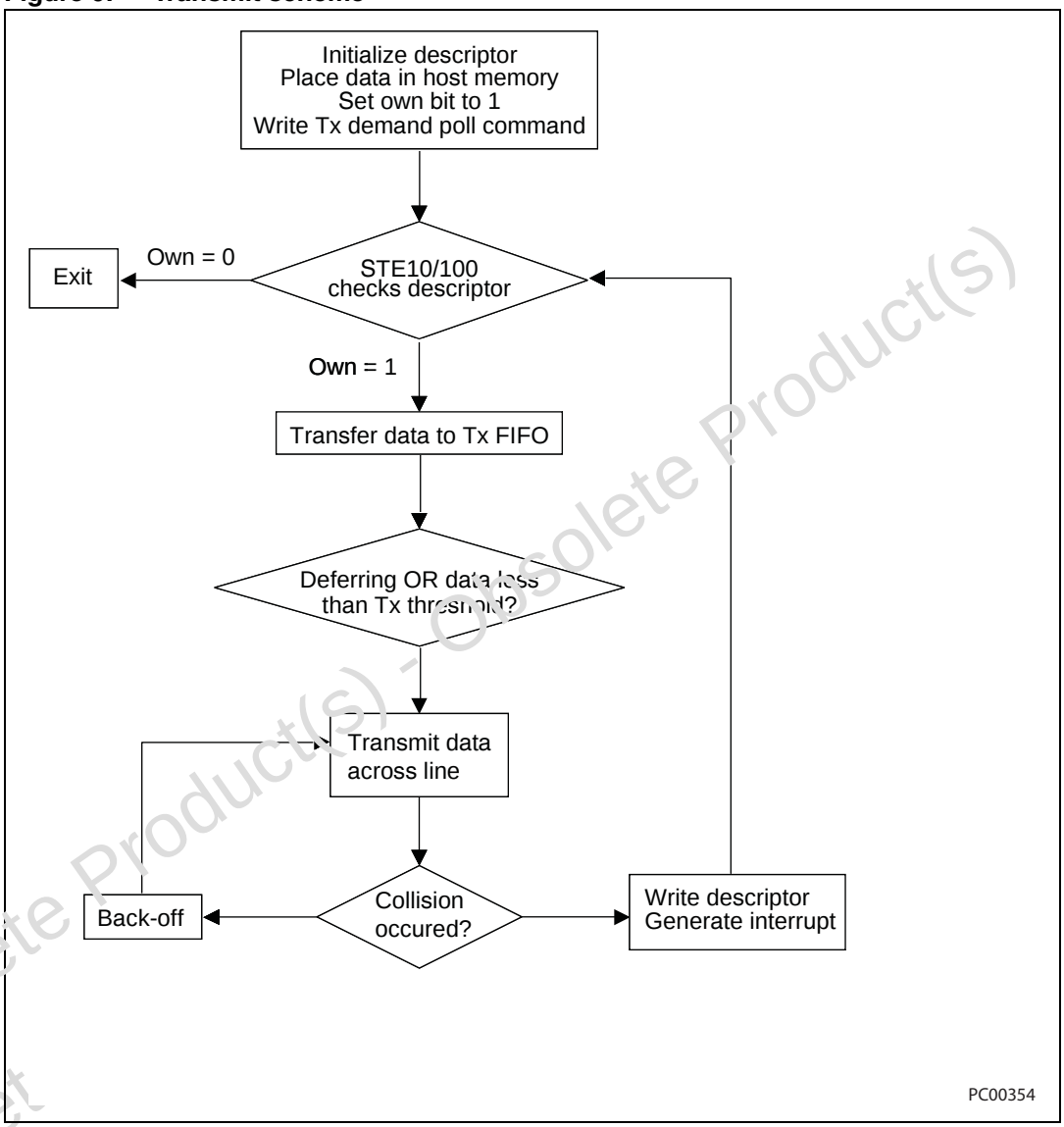
Figure 8. Receive descriptor management



3.3 Transmit scheme and transmit early interrupt

3.3.1 Transmit scheme

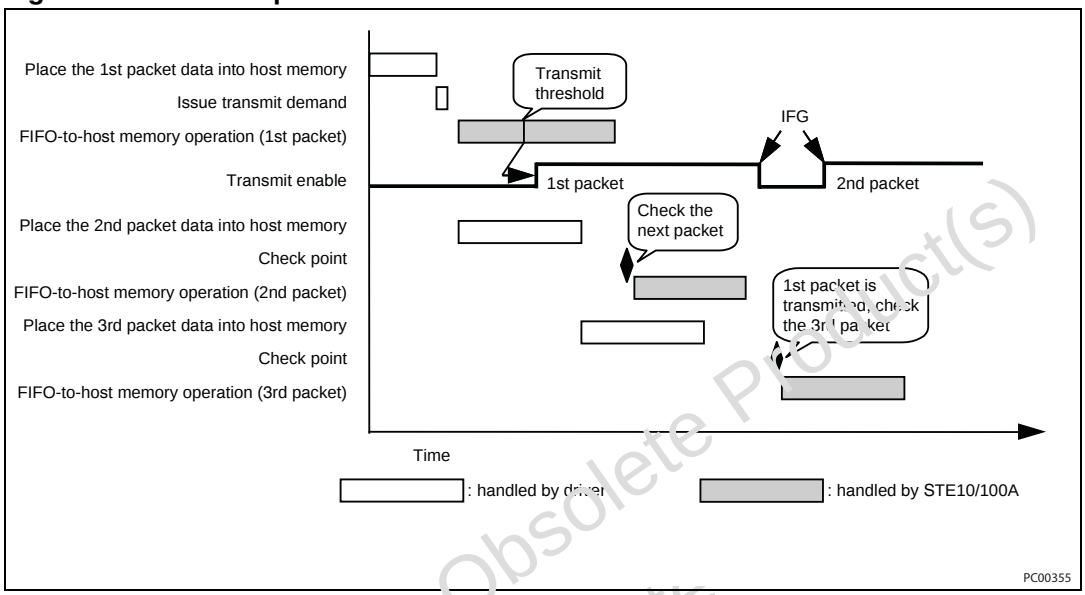
Figure 9. Transmit scheme



3.3.2 Transmit pre-fetch data flow

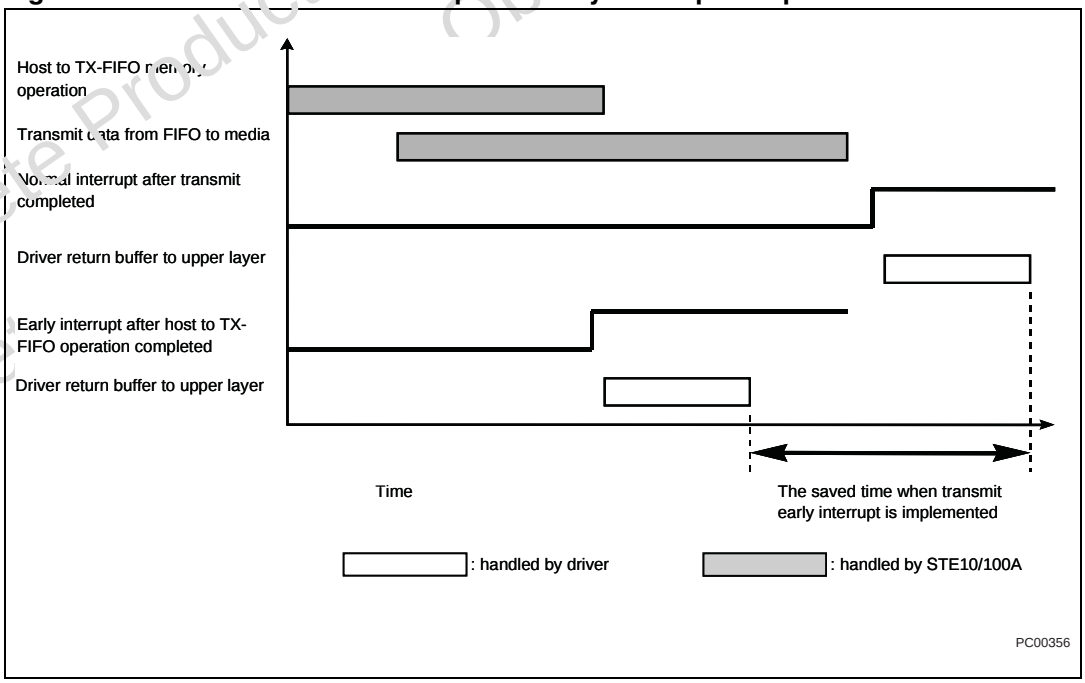
- Transmit FIFO size=2K-byte
- Two packets in the FIFO at the same time
- Meet the transmit min. back-to-back

Figure 10. Transmit pre-fetch data flow



3.3.3 Transmit early interrupt scheme

Figure 11. Transmit normal interrupt and early interrupt comparison



3.4 Receive scheme and receive early interrupt scheme

The following figure shows the difference of timing without early interrupt and with early interrupt.

Figure 12. Receive data flow (without early interrupt and with early interrupt)

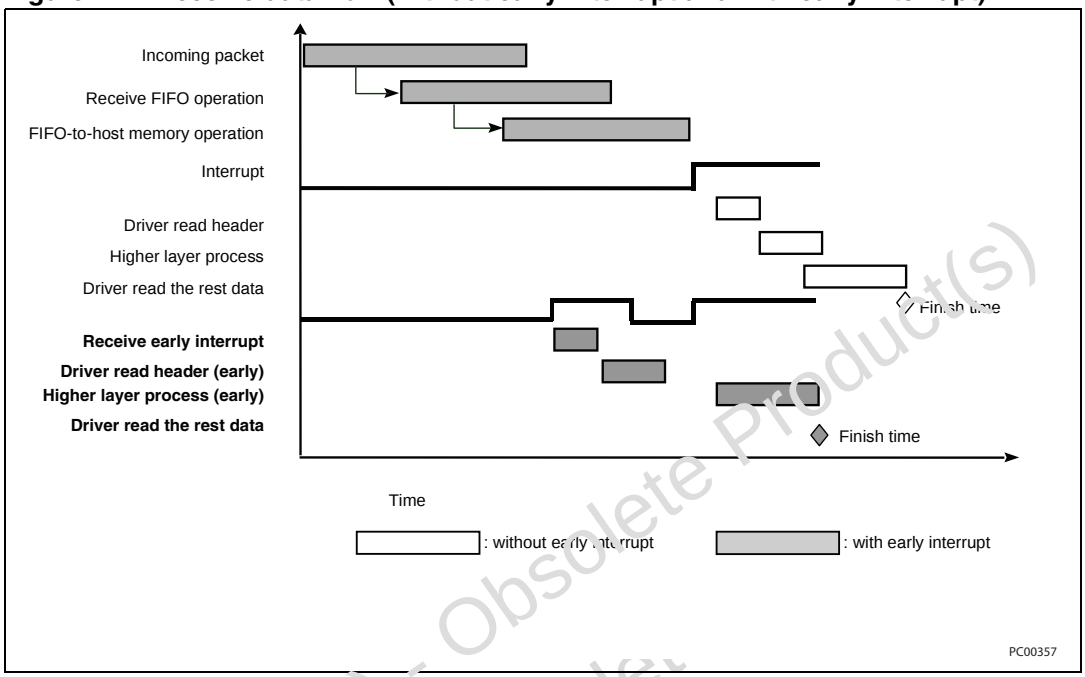
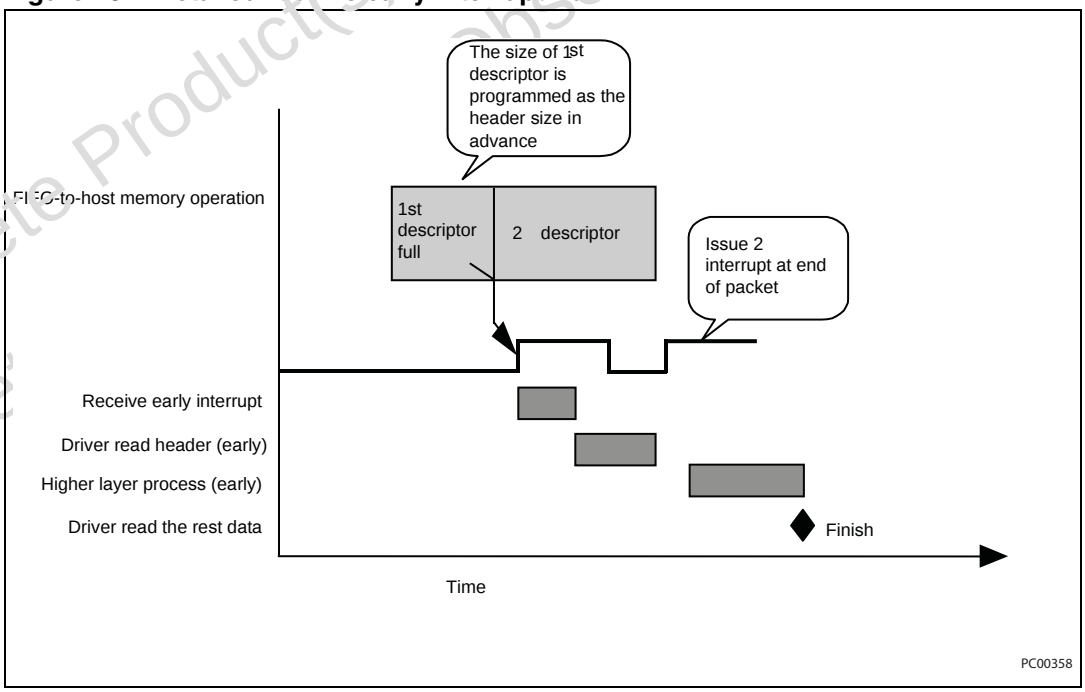


Figure 13. Detailed receive early interrupt flow



3.5 Network operation

3.5.1 MAC operation

The MAC (Media access control) portion of STE10/100A incorporates the essential protocol requirements for operating as an IEEE802.3 and ethernet compliant node.

Format

Table 2. Format

Field	Description
Preamble	A 7-byte field of (10101010b)
Start frame diameter	A 1-byte field of (10101011b)
Destination address	A 6-byte field
Source address	A 6-byte field
Length/type	A 2-byte field indicated the frame is in IEEE802.3 format or ethernet format. IEEE802.3 format: 0000H ~ 05DCH for length field Ethernet format: 05DD ~ FFFFH for type field
Data	46(1) ~ 1500 bytes of data information
CRC	A 32-bit cyclic redundancy code for error detection

1. If padding is disabled (TDES1 bit 23), the data field may be shorter than 46 bytes

Transmit data encapsulation

The differences between transmit data encapsulation and a MAC frame while operating in 100BASE-TX mode are listed as follows:

– The first byte of the preamble is replaced by the JK code according to IEE802.3u, clause 24.
– After the CRC field of the MAC frame, the STE10/100A will insert the TR code according to IEE802.3u, clause 24.

Receive data decapsulation

When operating in 100BASE-TX mode the STE10/100A detects a JK code in a preamble as well as a TR code at the packet end. If a JK code is not detected, the STE10/100A will abort the reception of the frame and wait for a new JK code detection. If a TR code is not detected, the STE10/100A will report a CRC error.

Deferring

The inter-frame gap (IFG) time is divided into two parts:

– FG1 time (64-bit time): If a carrier is detected on the medium during this time, the STE10/100A will reset the IFG1 time counter and restart to monitor the channel for an idle again.
– IFG2 time (32-bit time): After counting the IFG2 time the STE10/100A will access the channel even though a carrier has been sensed on the network.

Collision handling

The scheduling of re-transmissions are determined by a controlled randomization process called “truncated binary exponential back-off”. At the end of enforcing a collision (jamming), the STE10/100A delays before attempting to re-transmit the packet. The delay is an integer multiple of slot time. The number of slot times to delay before the nth re-transmission attempt is chosen as a uniformly distributed integer **r** in the range:

$0 \cdot r < 2^k$ where k = min(n, 10)

3.5.2 Transceiver operation

The transceiver portion of the ste10/100a integrates the ieee802.3u compliant functions of PCS (physical coding sub-layer), PMA (physical medium attachment) sub-layer, and PMD (physical medium dependent) sub-layer for 100base-tx, and the ieee802.3 compliant functions of manchester encoding/decoding and transceiver for 10base-t. All the functions and operating schemes are described in the following sections.

100BASE-TX transmit operation

For 100BASE-TX transmissions, the STE10/100A transceiver provides the transmission functions of PCS, PMA, and PMD for encoding of MII data nibbles into five-bit code-groups (4B/5B), scrambling, serialization of scrambled code-groups, converting the serial NRZ code into NRZI code, converting the NRZI code into MLT3 code, and then driving the MLT3 code into the category 5 unshielded twisted pair cable through an isolation transformer with the turns ratio of 1: 1.

Recommended transformers

HB626-1 from transpower technologies, 9410 prototype drive, suite #1, Reno, NV 89511. Tel: (775) 852-0140 and H1102 from pulse engineering Inc., 12220 World Trade Drive, San Diego, CA92128. Tel: (619) 674-8100.

Data code-groups encoder

In normal MII mode applications, the transceiver receives nibble type 4B data via the TxD0~3 inputs of the MII. These inputs are sampled by the transceiver on the rising edge of Tx_clk and passed to the 4B/5B encoder to generate the 5B code-group used by 100BASE-TX.

Idle code-groups

In order to establish and maintain the clock synchronization, the transceiver must keep transmitting signals to medium. The transceiver will generate Idle code-groups for transmission when there is no actual data to be sent by MAC.

Start-of-stream delimiter-SSD (/J/K/)

In a transmission stream, the first 16 nibbles comprise the MAC preamble. In order to let a network partner delineate the boundary of a data transmission sequence and to authenticate carrier events, the transceiver will replace the first 2 nibbles of the MAC preamble with /J/K/ code-groups.

End-of-stream delimiter-ESD (/T/R/)

In order to indicate the termination of normal data transmissions, the transceiver will insert 2 nibbles of /T/R/ code-group after the last nibble of the FCS.

Scrambling

All the encoded data (including the idle, SSD, and ESD code-groups) is passed to the data scrambler to reduce EMI by spreading the power spectrum using a 10-bit scrambler seed loaded at the beginning.

Data conversion of parallel to serial, NRZ to NRZI, NRZI to MLT3

After being scrambled, the 5B type transmission data at 25MHz will be converted to a 125HMz serial bit stream by the parallel-to-serial function. The bit stream will be further converted from NRZ to NRZI format, unless the conversion function is bypassed by clearing ENRZI (bit 7 of XR10) to 0. After NRZI conversion, the NRZI bit stream is passed through MLT3 encoder to generate the TP-PMD specified MLT3 code. By using MLT3 code, the frequency and energy content of the transmission signal is reduced in the UTP, making the system more easily compliant to FCC EMI specifications.

Wave-shaper and media signal driver

In order to reduce the energy of the harmonic frequency of transmission signals, the transceiver provides a wave-shaper prior the line driver to smooth the rising/falling edge of transmission signals while maintaining the waveforms' symmetry. The 100BASE-TX and 10BASE-T wave-shaped signals are both passed to the same media signal driver. This can simplify system design by employing a single external magnetic connection.

100BASE-TX receiving operation

For 100BASE-TX receiving operation, the transceiver provides the receiving functions of PMD, PMA, and PCS for incoming data signals through category 5 UTP cable and an isolation transformer with a 1:1 turns ratio. The receive transceiver portion includes the adaptive equalizer and baseline wander, MLT3 to NRZI data conversion, NRZI to NRZ conversion, serial to parallel conversion, a PLL for clock and data recovery, de-scrambler, and the 5B/4B decoder.

Adaptive equalizer and baseline wander

High speed signals over unshielded (or shielded) twisted pair cable will experience attenuation and phase shift. These effects depend on the signal frequency, cable type, cable length and the cable connectors. Robust circuits in the transceiver provide reliable adaptive equalizer and baseline wander compensation for amplitude attenuation and phase shift due to transmission line parasites.

MLT3 to NRZI decoder and PLL for data recovery

Following adaptive equalizer, baseline wander, the transceiver converts the resulting MLT3 to NRZI code, which is passed to the Phase Lock Loop circuits in order to extract the synchronous clock and the original data.

Data conversions of NRZI to NRZ and serial to parallel

After the data is recovered, it will be passed to the NRZI-to-NRZ converter to produce a 125MHz serial bit stream. This serial bit stream will be packed to parallel 5B type for further processing. The NRZI to NRZ conversion may be bypassed by clearing ENRZI (bit 7 of XR10) to 0.

De-scrambling and decoding of 5B/4B

The parallel 5B type data is passed to the de-scrambler and 5B/4B decoder to restore it to its original MII nibble representation.

Carrier sensing

The carrier sense (CRS) signal is asserted when the transceiver detects any 2 non-contiguous zeros within any 10-bit boundary of the receiving bit stream. CRS is de-asserted when ESD code-group or Idle code-group is detected. In half duplex mode, CRS is asserted during packet transmission or receive; in full duplex mode, CRS is asserted only during packet reception.

10BASE-T transmission operation

The parallel-to-serial converter, Manchester Encoder, Link test, Jabber and the transmit wave-shaper and line driver functions described in the section of “Wave-Shaper and Media Signal Driver” of “100BASE-T Transmission Operation” are also provided for 10BASE-T transmission. Additionally, Collision detection and SQE test for half duplex application are provided.

10BASE-T receive operation

Carrier sense function, receiving filter, PLL for clock and data recovery, Manchester decoder, and serial to parallel converter functions are provided to support 10BASE-T reception.

Loop-back operation of transceiver

- The transceiver provides internal loop-back (also called transceiver loop-back) operation for both 100BASE-TX and 10BASE-T operation. The loop-back function can be enabled by setting XLBEN (bit 14 of XR0) to 1. In loop-back mode, the TX± and RX± lines are isolated from the media. The transceiver also provides remote loop-back operation for 100BASE-TX operation. The remote loop-back operation can be enabled by setting ENRLB (bit 9 of XR10) to 1.
- In 100BASE-TX internal loop-back operation, the data is routed from the transmit output of NRZ-to-NRZI converter and looped back to the receive input of NRZI-to-NRZ converter.
  In 100BASE-TX remote loop-back operation, data is received from RX± pins and passed through the receive path to the output of the data and clock recovery section, and then looped back to the input of the NRZI-to-MLT3 converter and out to the medium via the transmit line drivers.
  In 10BASE-T loop-back operation, the data is passed through the transmit path to the output of the Manchester encoder and then looped back into the input of the phase lock loop circuit in the receive path.

Full duplex and half duplex operation of transceiver

The transceiver can operate in either full duplex or half duplex network applications. In full duplex, both transmission and reception can take place simultaneously. In full duplex mode, collision (COL) signal is ignored and carrier sense (CRS) signal is asserted only when the transceiver is receiving.
In half duplex mode, transmission and reception can not take place simultaneously. In half duplex mode, the collision signal is asserted when transmitted and received signals collide, and carrier sense is asserted during both transmission and reception.

Auto-negotiation operation

The auto-negotiation function provides the means to exchange information between the transceiver and the network partner to automatically configure both to take maximum advantage of their abilities. The auto-negotiation function is controlled by ANEN (bit 12 of XR0).

During auto-negotiation information is exchanged with the network partner using fast link pulses (FLPs) - a burst of link pulses. There are 16 bits of signaling information contained in the link pulses which advertise to the remote partner the capabilities which are represented by the contents of ANA (register XR4). According to this information the partners find out their highest common capabilities by following the priority sequence listed below:

- 100BASE-TX full duplex
- 100BASE-TX half duplex
- 10BASE-T full duplex
- 10BASE-T half duplex

During power-up or reset, if auto-negotiation is enabled, the FLPs will be transmitted and the auto-negotiation function will proceed. Otherwise, auto-negotiation will not occur until ANEN (bit 12 of XR0) is set to 1. When the auto-negotiation is disabled, then network speed and duplex mode are selected by programming the XR0 register.

Power down operation

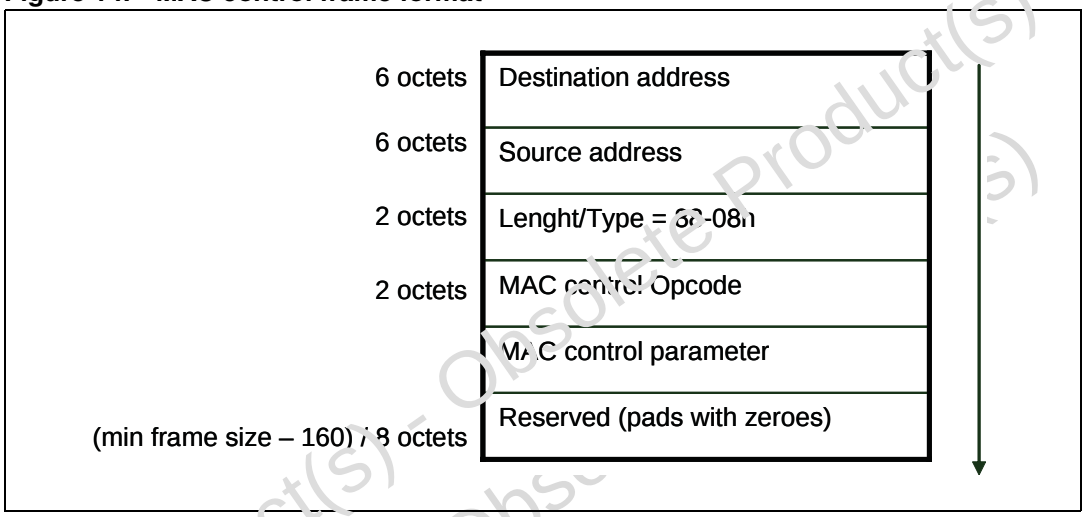
The transceiver is designed with a power-down feature which can reduce power consumption significantly. Since the power supply of the 100BASE-TX and 10BASE-T circuits are separate, the transceiver can turn off the circuit of either the 100BASE-TX or 10BASE-T when the other is active.

3.5.3 Flow control in full duplex application

The PAUSE function is used to inhibit transmission of data frames for a specified period of time. The STE10/100A supports the full duplex protocol of IEEE802.3x. To support the PAUSE function, the STE10/100A implements the MAC Control Sub-layer functions to decode the MAC Control frames received from MAC control clients and to execute the relative requests accordingly. When full duplex mode and the PAUSE function are selected after Auto-Negotiation completes (refer to the configuration of XR8), the STE10/100A will enable the PAUSE function for flow control in a full duplex application. In this section we will describe how the STE10/100A implements the PAUSE function.

MAC control frame and PAUSE frame

Figure 14. MAC control frame format



The MAC control frame is distinguished from other MAC frames only by its length/type field identifier. The MAC control opcode defined in MAC control frame format for the PAUSE function is 0001h, and the PAUSE time is specified in the MAC control parameters field with 2 octets, representing an unsigned integer, in units of slot-times. The range of possible PAUSE times is 0 to 65535 slot-times.

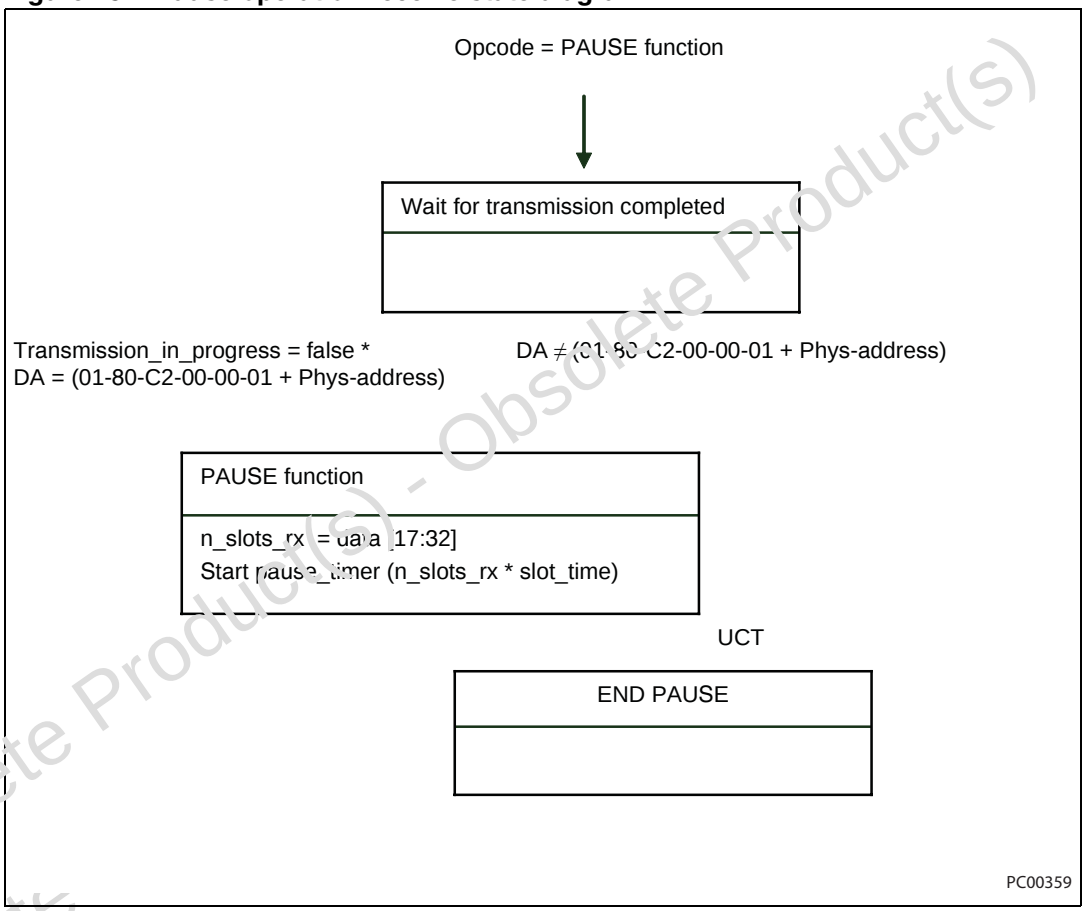
A valid PAUSE frame issued by a MAC control client (for example, a switch or a bridge) would contain:

- The destination address, set to the globally assigned 48 bit mulitcast address 01-80-C2-00-00-01, or to the unicast address to which the MAC control client requests to inhibit its transmission of data frames.
- The MAC control opcode field set to 0001h.
- 2 octets of PAUSE time specified in the MAC control parameter field to indicate the length of time for which the destination is requested to inhibit data frame transmission.

Receive operation for PAUSE function

Upon reception of a valid MAC Control frame, the STE10/100A will start a timer for the length of time specified by the MAC control parameters field. When the timer value reaches zero, the STE10/100A exits the PAUSE state. However, a PAUSE frame will not affect the transmission of a frame that has been submitted to the MAC (i.e., once a transmit out of the MAC is begun, it can't be interrupted). Conversely, the STE10/100A will not begin to transmit a frame more than one slot-time after valid PAUSE frame is received a with a non-zero PAUSE time. If the STE10/100A receives a PAUSE frame with a zero PAUSE time value, the STE10/100A exits the PAUSE state immediately.

Figure 15. Pause operation receive state diagram



3.6 LED display operation

The STE10/100A provides 2 LED display modes; the detailed descriptions of their operation are described in the pin description section.

First mode – 3 LED displays

- 100Mbps (on) or 10Mbps (off)
- Link (Remains on when link ok) or activity (Blinks at 10Hz when receiving or transmitting collision-free)
- FD (Remains on when in full duplex mode) or collision (Blinks at 20Hz when collisions detected)

Second mode – 4 LED displays

- 100 Link (On when 100M link ok)
- 10 Link (On when 10M link ok)
- Activity (Blinks at 10Hz when receiving or transmitting)
- FD (Remains on when in full duplex mode) or collision (Blinks at 20Hz when collisions detected)

3.7 Reset operation

3.7.1 Reset whole chip

There are two ways to reset the STE10/100A:

- Hardware reset
  Via RST# pin (to ensure proper reset operation, the RST# signal should be asserted at least 100ms)
- Software reset
  Via SWR (bit 0 of CSR0) being set to 1 (the STE10/100A will reset all circuits except the transceivers and configuration registers, set registers to their default values, and will clear SWR) and set XRST(XR0, bit 15) to reset the transceivers.

3.7.2 Reset transceiver only

When XRST (bit 15 of XR0) is set to 1, the transceiver will reset its circuits, will initialize its registers to their default values, and clear XRST.

3.8 Wake on LAN function

The STE10/100A can assert a signal to wake up the system when it has received a Magic Packet from the network. The wake on LAN operation is described as follow.

The Magic Packet format

- Valid destination address that can pass the address filter of the STE10/100A
- Payload of the frame including at least 6 contiguous 'FF' followed immediately by 16 repetitions of IEEE address
- The frame can contain multiple 'six FF + sixteen IEEE address' pattern
- Valid CRC

The wake on LAN operation

The wake on LAN enable function is controlled by WOL (bit 18 of CSR18), which is loaded from EEPROM after reset or programmed by driver software. If WOL is set and the STE10/100A receives a Magic Packet, it will assert the PME# signal (active low) to indicate reception of a wake up frame and will set the PME status bit (bit 15 of CSR20).

3.9 ACPI power management function

The STE10/100A has a built-in capability for power management (PM) which is controlled by the host system.

The STE10/100A will provide:

- Compatibility with device class power management reference specification
- Network device class, draft proposal v0.9, october 1996
- Compatibility with ACPI, Rev 1.0, december 22, 1996
- Compatibility with PCI bus power management interface specification, Rev 1.0, january 6, 1997
- Compatibility with AMD Magic Packet™ Technology.

3.9.1 Power states

DO (Fully on)

In this state the STE10/100A operates with full functionality and consumes normal power. While in the D0 state, if the PCI clock is lower than 16MHz, the STE10/100A may not receive or transmit frames properly.

D1, D2, and $D3_{hot}$

In these states, the STE10/100A doesn't respond to any accesses except configuration space and full function context in place. The only network operation the STE10/100A can initiate is a wake-up event.

$D3_{cold}$ (Power removed)

In this state all function context is lost. When power is restored, a PCI reset must be asserted and the function will return to D0.

$D3_{hot}$ (Software visible D3)

When the STE10/100A is brought back to D0 from D3hot the software must perform a full initialization.
The STE10/100A in the D3hot state responds to configuration cycles as long as power and clock are supplied. This requires the device to perform an internal reset and return to a power-up reset condition without the RST# pin asserted.

Table 3. Power stage

Device state	PCI bus state	Function context	Clock	Power	Supported actions to function	Supported actions from function
D0	B0	Full function context in place	Full speed	Full power	Any PCI transaction	Any PCI transaction or interrupt
D1	B0, B1	Configuration maintained. No Tx and Rx except wake-up events	Stopped to full speed		PCI configuration access	Only wake-up events
D2	B0, B1, B2	Configuration maintained. No Tx and Rx	Stopped to full speed		PCI configuration access(B0, B1)	
D3hot	B0, B1, B2	Configuration lost, full initialization required upon return to D0	Stopped to full speed		PCI configuration access(B0, B1)	
D3cold	B3	All configuration lost. Power-on defaults in place on return to D0	No clock	No power	Power-on reset	

4 Registers and descriptors description

Note: There are three kinds of registers within the STE10/100A: STE10/100A configuration registers, PCI control/status registers, and transceiver control/status registers.

The STE10/100A configuration registers are used to initialize and configure the STE10/100A and for identifying and querying the STE10/100A.

The PCI control/status registers are used to communicate between the host and STE10/100A. The host can initialize, control, and read the status of the STE10/100A through mapped I/O or memory address space.

The STE10/100A contains 11 16-bit registers to supported transceiver control and status. They include 7 basic registers which are defined according to clause 22 “Reconciliation Sub-layer and Media Independent Interface” and clause 28 “Physical Layer link signaling for 10 Mb/s and 100 Mb/s auto-negotiation on twisted pair” of the IEEE802.3u standard. In addition, 4 special registers are provided for advanced chip control and status.

The STE10/100A also provides receive and transmit descriptors for packet buffering and management.

4.1 STE10/100A configuration registers

An STE10/100A software driver can initialize and configure the chip by writing its configuration registers. The contents of configuration registers are set to their default values upon power-up or whenever a hardware reset occurs, but their settings remain unchanged whenever a software reset occurs. The configuration registers are byte, word, and double word accessible.

Table 4. STE10/100A configuration registers list

Offset	Index	Name	Description
00h	CR0	LID	Loaded device ID and vendor ID
04h	CR1	CSC	Configuration status and command
08h	CR2	CC	Class code and revision number
0ch	CR3	LT	Latency timer
10h	CR4	IOBA	IO base address
14h	CR5	MBA	Memory base address
2ch	CR11	SID	Subsystem ID and vendor ID
30h	CR12	BRBA	Boot ROM base address (ROM size = 128Kbit)
34h	CR13	CP	Capability pointer
3ch	CR15	CINT	Configuration interrupt
40h	CR16	DS	Driver space for special purpose
80h	CR32	SIG	Signature of STE10/100A
c0h	CR48	PMR0	Power management register 0
c4h	CR49	PMR1	Power management register 1

Table 5. STE10/100A configuration registers table

offset	b31 ---------- b16		b15 ---------- b0		
00h	Device ID*		Vendor ID(1)		
04h	Status		Command		
08h	Base class code	Subclass	------	Revision #	Step #
0ch	------	------	Latency timer	Cache line size	
10h	Base I/O address				
14h	Base memory address				
18h~28h	Reserved				
2ch	Subsystem ID(1)		Subsystem vendor ID(1)		
30h	Boot ROM base address				
34h	Reserved			Cap_Ptr	
38h	Reserved				
3ch	Max_Lat(1)	Min-Gnt(1)	Interrupt pin	Interrupt line	
40h	Reserved		Driver space	Reserved	
80h	Signature of STE10/100A				
c0h	PMC		Next_Item_Ptr		Cap_ID
c4h	Reserved			PMCSR	

1. Automatically recalled from EEPROM when PCI reset is deserted
DS(40h), bit15-8, is read/write able register
SIG(80h) is hard wired register, read only

4.1.1 STE10/100A configuration registers description

Table 6. Configuration registers description

Bit #	Name	Description	Default	RW type
CR0 (offset = 00h), LID - Loaded identification number of device and vendor				
31~16	LDID	Loaded device ID, the device ID number loaded from serial EEPROM	From EEPROM	R/O
15~0	LVID	Loaded vendor ID, the vendor ID number loaded from serial EEPROM	From EEPROM	R/O
From EEPROM: Loaded from EEPROM				
CR1 (offset = 04h), CSC - Configuration command and status				
31	SPE	Status parity error. 1: means that STE10/100A detected a parity error. This bit will be set even if the parity error response (bit 6 of CR1) is disabled.	0	R/W
30	SES	Status system error. 1: means that STE10/100A asserted the system error pin.	0	R/W
29	SMA	Status master abort. 1: means that STE10/100A received a master abort and has terminated a master transaction.	0	R/W
28	STA	Status target abort. 1: means that STE10/100A received a target abort and has terminated a master transaction.	0	R/W
27	---	Reserved		
26, 25	SDST	Status device select timing. Indicates the timing of the chip's assertion of device select. 01: indicates a medium assertion of DEVSEL#.	01	R/O
24	SDPR	Status data parity report. 1: when three conditions are met: a. STE10/100A asserted parity error (PERR#) or it detected parity error asserted by another device. b. STE10/100A is operating as a bus master. c. STE10/100A's parity error response bit (bit 6 of CR1) is enabled.	0	R/W
23	SFBB	Status fast back-to-back. Always 1, since STE10/100A has the ability to accept fast back to back transactions.	1	R/O
22~21	---	Reserved		

Table 6. Configuration registers description (continued)

Bit #	Name	Description	Default	RW type
20	NC	New capabilities. Indicates whether the STE10/100A provides a list of extended capabilities, such as PCI power management. 1: the STE10/100A provides the PCI management function. 0: the STE10/100A doesn't provide new capabilities.	Same as bit 19 of CSR18	RO
19~ 9	---	Reserved		
8	CSE	Command system error response. 1: enable system error response. The STE10/100A will assert SERR# when it finds a parity error during the address phase.	1	R/W
7	---	Reserved		
6	CPE	Command parity error response. 0: disable parity error response. STE10/100A will ignore any detected parity error and keep on operating. Default value is 0. 1: enable parity error response. STE10/100A will assert system error (bit 13 of CSR5) when a parity error is detected.	0	R/W
5~ 3	---	Reserved		
2	CMO	Command master operation ability. 0: disable the STE10/100A bus master ability. 1: enable the PCI bus master ability. Default value is 1 for normal operation.	1	R/W
1	CMSA	Command memory space access. 0: disable the memory space access ability. 1: enable the memory space access ability.	1	R/W
0	CIOSA	Command I/O space access. 0: enable the I/O space access ability. 1: disable the I/O space access ability.	1	R/W
R/W: Read and write able. RO: Read able only.				
CR2 (offset = 08h), CC - Class code and revision number				
31~24	BCC	Base class code. It means STE10/100A is a network controller.	02h	RO
23~16	SC	Subclass code. It means STE10/100A is a fast ethernet controller.	00h	RO
15~ 8	---	Reserved		
7 ~ 4	RN	Revision number, identifies the revision number of STE10/100A	Ah	RO
3 ~ 0	SN	Step number, identifies the STE10/100A steps within the current revision	1h	RO
RO: Read only				

Table 6. Configuration registers description (continued)

Bit #	Name	Description	Default	RW type
CR3 (offset = 0ch), LT - Latency timer				
31~16	---	Reserved		
15~ 8	LT	Latency timer. This value specifies the latency timer of the STE10/100A in units of PCI bus clock cycles. Once the STE10/100A asserts FRAME#, the latency timer starts to count. If the latency timer expires and the STE10/100A is still asserting FRAME#, the STE10/100A will terminate the data transaction as soon as its GNT# is removed.	40h	R/W
7 ~ 0	CLS	Cache line size. This value specifies the system cache line size in units of 32-bit double words (DW). The STE10/100A supports cache line sizes of 8, 16, or 32 DW. CLS is used by the STE10/100A driver to program the cache alignment bits (bit 14 and 15 of CSR0) which are used for cache oriented PCI commands, for example, memory-read-line, memory-read-multiple, and memory-write-and-invalidate.	08h	R/W
CR4 (offset = 10h), IOBA - I/O base address				
31~ 7	IOBA	I/O base address. This value indicate the base address of PCI control and status register (CSR0~28), and transceiver registers (XR0~10).	0	R/W
6 ~ 1	---	Reserved		
0	IOSI	I/O space indicator. 1: means that the configuration registers map into I/O space.	1	RO
CR5 (offset = 14h), MBA - Memory base address				
31~ 7	MBA	Memory base address. This value indicate the base address of PCI control and status register(CSR0~28), and transceiver registers(XR0~10).	0	R/W
6 ~ 1	---	Reserved		
0	IOSI	Memory space indicator. 1: means that the configuration registers map into I/O space.	0	RO
CR11 (offset = 2ch), SID - Subsystem ID				
31~16	SID	Subsystem ID. This value is loaded from EEPROM as a result of power-on or hardware reset.	From EEPROM	RO
15~ 0	SVID	Subsystem vendor ID. This value is loaded from EEPROM as a result power-on or hardware reset.	From EEPROM	RO
CR12 (offset = 30h), BRBA - Boot ROM base address. This register should be initialized before accessing the boot ROM space.				

Table 6. Configuration registers description (continued)

Bit #	Name	Description	Default	RW type
31~10	BRBA	Boot ROM base address. This value indicates the address mapping of the boot ROM field as well as defining the boot ROM size. The values of bit 16~10 are set to 0 indicating that the STE10/100A supports up to 128Kbit of boot ROM.	X: b31~17 0: b16~10	R/W RO
9 ~ 1	---	Reserved		RO R/W R/W
0	BRE	Boot ROM enable. The STE10/100A will only enable its boot ROM access if both the memory space access bit (bit 1 of CR1) and this bit are set to 1. 1: enable boot ROM. (If bit 1 of CR1 is also set).	0	R/W
CR13 (offset = 34h), CP - Capabilities pointer				
31~8	---	Reserved		
7~0	CP	Capabilities pointer	C0h	RO
CR15 (offset = 3ch), CI - Configuration interrupt				
31~24	ML	Max_Lat register. This value indicates how often the STE10/100A needs to access to the PCI bus in units of 250ns. This value is loaded from serial EEPROM as a result of power on or hardware reset.	From EEPROM	RO
23~16	MG	Min_Gnt register. This value indicates how long the STE10/100A needs to retain the PCI bus ownership whenever it initiates a transaction, in units of 250ns. This value is loaded from serial EEPROM as a result power-on or hardware reset.	From EEPROM	RO
15~8	IP	Interrupt Pin. This value indicates one of four interrupt request pins to which the STE10/100A is connected. 01h: means the STE10/100A always connects to INTA#.	01h	RO
7 ~ 0	IL	Interrupt Line. This value indicates the system interrupt request lines to which the INTA# of STE10/100A is routed. The BIOS will fill this field when it initializes and configures the system. The STE10/100A driver can use this value to determine priority and vector information.	0	R/W
CR16 (offset = 40h), DS - Driver space for special purpose				
31~16	---	Reserved		
15~8	DS	Driver space for implementation-specific purpose. Since this area won't be cleared upon software reset, an STE10/100A driver can use this R/W area as user-specified storage.	0	R/W
7 ~ 0	---	Reserved		
CR32 (offset = 80h), SIG - Signature of STE10/100A				

Table 6. Configuration registers description (continued)

Bit #	Name	Description	Default	RW type
31~16	DID	Device ID, the device ID number of the STE10/100A	2774h	RO
15~0	VID	Vendor ID, the vendor ID number of STMicroelectronics	104Ah	RO
CR48 (offset = c0h), PMR0, Power management register 0				
31 30 29 28 27	PSD3c, PSD3h, PSD2, PSD1, PSD0	PME_Support. The STE10/100A will assert PME# signal while in the D0, D1, D2, D3hot and D3cold power state. The STE10/100A supports Wake-up from the above five states. Bit 31 (support wake-up from D3cold) is loaded from EEPROM after power-up or hardware reset. To support the D3cold wake-up function, an auxiliary power source will be sensed during reset by the STE10/100A Vaux_detect pin. If sensed low, PSD3c will be set to 0; if sensed high, and if D3CS (bit 31of CSR18) is set (CSR18 bits 16~31 are recalled from EEPROM at reset), then bit 31 will be set to 1.	X1111b	RO
26	D2S	D2_Support. The STE10/100A supports the D2 Power management state.	1	RO
25	D1S	D1_Support. The STE10/100A supports the D1 Power management state.	1	RO
24~22	AUXC	Aux current. These three bits report the maximum 3.3Vaux current requirements for STE10/100A chip. If bit 31 of PMR0 is '1', the default value is 111b, meaning the STE10/100A needs 375 mA to support remote wake-up in D3cold power state. Otherwise, the default value is 000b, meaning the STE10/100A does not support remote wake-up from D3cold power state.	XXXb	RO
21	DSI	The device specific initialization bit indicates whether any special initialization of this function is required before the generic class device driver is able to use it. 0: indicates that the function does not require a device-specific initialization sequence following transition to the D0 uninitialized state.	0	RO
20	---	Reserved		
19	PMEC	PME Clock. Indicates that the STE10/100A does not rely on the presence of the PCI clock for PME# operation.	0	RO
18~16	VER	Version. The value of 010b indicates that the STE10/100A complies with revision 1.0a of the PCI power management interface specification.	010b	RO
15~8	NIP	Next item pointer. This value is always 0h, indicating that there are no additional items in the capabilities list.	00h	RO

Table 6. Configuration registers description (continued)

Bit #	Name	Description	Default	RW type
7~0	CAPID	Capability identifier. This value is always 01h, indicating the link list item as being the PCI power management registers.	01h	RO
CR49 (offset = c4h), PMR1, Power management register 1				
31~16	---	Reserved		
15	PMEST	PME_Status. This bit is set whenever the STE10/100A detects a wake-up event, regardless of the state of the PME-En bit. Writing a “1” to this bit will clear it, causing the STE10/100A to deassert PME# (if so enabled). Writing a “0” has no effect. If PSD3c (bit 31 of PMR0) is cleared (i.e. it does not support PME# generation from D3cold), this bit is by default 0; otherwise, PMEST is cleared upon power-up reset only and is not modified by either hardware or software reset.	X	R/W1C(1)
14,13	DSCAL	Data_Scale. Indicates the scaling factor to be used when interpreting the value of the data register. This field is required for any function that implements the data register. The STE10/100A does not support data register and Data_Scale.	00b	RO
12~9	DSEL	Data_Select. This four bit field is used to select which data is to be reported through the data register and Data_Scale field. This field is required for any function that implements the data register. The STE10/100A does not support Data_select.	0000b	R/W
8	PME_En	PME_En. When set, enables the STE10/100A to assert PME#. When cleared, disables the PME# assertion. If PSD3c (bit 31 of PMR0) is cleared (i.e. it does not support PME# generation from D3cold), this bit is by default 0; otherwise, PME_En is cleared upon power up reset only and is not modified by either hardware or software reset.	X	R/W

Table 6. Configuration registers description (continued)

Bit #	Name	Description	Default	RW type
7~2	---	Reserved	000000b	RO
1,0	PWRS	PowerState. This two bit field is used both to determine the current power state of the STE10/100A and to place the STE10/100A in a new power state. The definition of this field is given below. 00b - D0 01b - D1 10b - D2 11b - D3hot If software attempts to write an unsupported state to this field, the write operation will complete normally on the bus, but the data is discarded and no state change occurs.	00b	R/W

1. R/W1C: Read only and write one cleared

4.2 PCI control/status registers

Table 7. PCI control/status registers list

Offset from base address of CSR	Index	Name	Descriptions
00h	CSR0	PAR	PCI access register
08h	CSR1	TDR	Transmit demand register
10h	CSR2	RDR	Receive demand register
18h	CSR3	RDB	Receive descriptor base address
20h	CSR4	TDB	Transmit descriptor base address
28h	CSR5	SR	Status register
30h	CSR6	NAR	Network access register
38h	CSR7	IER	interrupt enable register
40h	CSR8	LPC	Lost packet counter
48h	CSR9	SPR	Serial port register
50h	CSR10	---	Reserved
58h	CSR11	TMR	Timer
60h	CSR12	---	Reserved
68h	CSR13	WCSR	Wake-up control/status register
70h	CSR14	WPDR	Wake-up pattern data register
78h	CSR15	WTMR	Watchdog timer
80h	CSR16	ACSR5	Status register 2
84h	CSR17	ACSR7	Interrupt enable register 2
88h	CSR18	CR	Command register
8ch	CSR19	PCIC	PCI bus performance counter
90h	CSR20	PMCSR	Power management command and status
94h	CSR21	---	Reserved
98h	CSR22	---	Reserved
9ch	CSR23	TXBR	Transmit burst counter/time-out register
a0h	CSR24	FROM	Flash(boot) ROM port
a4h	CSR25	PAR0	Physical address register 0
a8h	CSR26	PAR1	Physical address register 1
ach	CSR27	MAR0	Multicast address hash table register 0
b0h	CSR28	MAR1	Multicast address hash table register 1

Table 8. Control/status register description

Bit #	Name	Description	Default	RW type
CSR0 (offset = 00h), PAR - PCI access register				
31~25	---	Reserved		
24	MWIE	Memory write and invalidate enable. 1: enable STE10/100A to generate memory write invalidate command. The STE10/100A will generate this command while writing full cache lines. 0: disable generating memory write invalidate command. The STE10/100A will use memory write commands instead.	0	R/W*
23	MRLE	Memory read line enable. 1: enable STE10/100A to generate memory read line command when read access instruction reaches the cache line boundary. If the read access instruction doesn't reach the cache line boundary then the STE10/100A uses the memory read command instead.	0	R/W*
22	---	Reserved		
21	MRME	Memory read multiple enable. 1: enable STE10/100A to generate memory read multiple commands when reading a full cache line. If the memory is not cache-aligned, the STE10/100A uses the memory read command instead.	0	R/W*
20~19	---	Reserved		
18,17	TAP	Transmit auto-polling in transmit suspended state. 00: disable auto-polling (default) 01: polling own-bit every 200 us 10: polling own-bit every 800 us 11: polling own-bit every 1600 us	00	R/W*
16	---	Reserved		
15, 14	CAL	Cache alignment. Address boundary for data burst, set after reset 00: reserved (default) 01: 8 DW boundary alignment 10: 16 DW boundary alignment 11: 32 DW boundary alignment	00	R/W*
13 ~ 8	PBL	Programmable burst length. This value defines the maximum number of DW to be transferred in one DMA transaction. Value: 0 (unlimited), 1, 2, 4, 8, 16 (default), 32	000000	R/W*

Table 8. Control/status register description (continued)

Bit #	Name	Description	Default	RW type
7	BLE	Big or little endian selection. 0: little endian (for example INTEL) 1: big endian (only for data buffer)	0	R/W*
6 ~ 2	DSL	Descriptor skip length. Defines the gap between two descriptors in the units of DW.	0	R/W*
1	BAR	Bus arbitration 0: receive operations have higher priority 1: transmit operations have higher priority	0	R/W*
0	SWR	Software reset 1: Reset all internal hardware (excluding transceivers and configuration registers). This signal will be cleared by the STE10/100A itself after the reset process is completed.	0	R/W*
R/W* = Before writing the transmit and receive operations should be stopped.				
CSR1 (offset = 08h), TDR - Transmit demand register				
31~ 0	TPDM	Transmit poll demand. While the STE10/100A is in the suspended state, a write to this register (any value) will trigger the read-tx descriptor process, which checks the own-bit; if set, the transmit process is then started.	FFFFFFFFh	R/W*
R/W* = Before writing the transmit process should be in the suspended state				
CSR2 (offset = 10h), RDP - Receive demand register				
31 ~ 0	RPDM	Receive poll demand. While the STE10/100A is in the suspended state, a write to this register (any value) will trigger the read-rx-descriptor process, which checks the own-bit, if set, the process to move data from the FIFO to buffer is then started.	FFFFFFFFh	R/W*
R/W* = Before writing the receive process should be in the suspended state				
CSR3 (offset = 18h), RDB - Receive descriptor base address				
31~ 2	SAR	Start address of receive descriptor	0	R/W*
1, 0	RBND	Must be 00, DW boundary	00	RO
R/W* = Before writing the receive process should be stopped				
CSR4 (offset = 20h), TDB - Transmit descriptor base address				
31~ 2	SAT	Start address of transmit descriptor	0	R/W*
1, 0	TBND	Must be 00, DW boundary	00	RO
R/W* = Before writing the transmit process should be stopped				

Table 8. Control/status register description (continued)

Bit #	Name	Description	Default	RW type
CSR5 (offset = 28h), SR - Status register				
31~ 26	----	Reserved		
25~ 23	BET	Bus error type. This field is valid only when bit 13 of CSR5(fatal bus error) is set. There is no interrupt generated by this field. 000: parity error, 001: master abort, 010: target abort 011, 1xx: reserved	000	RO
22~ 20	TS	Transmit state. Reports the current transmission state only, no interrupt will be generated. 000: stop 001: read descriptor 010: transmitting 011: FIFO fill, read the data from memory and put into FIFO 100: reserved 101: reserved 110: suspended, unavailable transmit descriptor or FIFO overflow 111: write descriptor	000	RO
19~17	RS	Receive state. Reports current receive state only, no interrupt will be generated. 000: stop 001: read descriptor 010: check this packet and pre-fetch next descriptor 011: wait for receiving data 100: suspended 101: write descriptor 110: flush the current FIFO 111: FIFO drain, move data from receiving FIFO into memory	000	RO
16	NISS	Normal interrupt status summary. Set if any of the following bits of CSR5 are asserted: – TCI, transmit completed interrupt (bit 0) – TDU, transmit descriptor unavailable (bit 2) – RCI, receive completed interrupt (bit 6)	0	RO/LH*

Table 8. Control/status register description (continued)

Bit #	Name	Description	Default	RW type
15	AISS	Abnormal interrupt status summary. Set if any of the following bits of CSR5 are asserted: – TPS, transmit process stopped (bit 1) – TJT, transmit jabber timer time-out (bit 3) – TUF, transmit under-flow (bit 5) – RDU, receive descriptor unavailable (bit 7) – RPS, receive process stopped (bit 8) – RWT, receive watchdog time-out (bit 9) – GPTT, general purpose timer time-out (bit 11) – FBE, fatal bus error (bit 13)	0	RO/LH*
14	----	Reserved		
13	FBE	Fatal bus error. 1: on occurrence of parity error, master abort, or target abort (see bits 25~23 of CSR5). The STE10/100A will disable all bus access. A software reset is required to recover from a parity error.	0	RO/LH*
12	---	Reserved		
11	GPTT	General purpose timer timeout, based on CSR11 timer register	0	RO/LH*
10	---	Reserved		
9	RWT	Receive watchdog timeout, based on CSR15 watchdog timer register	0	RO/LH*
8	RPS	Receive process stopped, receive state = stop	0	RO/LH*
7	RDU	Receive descriptor unavailable. 1: when the next receive descriptor can not be obtained by the STE10/100A. The receive process is suspended in this situation. To restart the receive process, the ownership bit of the next receive descriptor should be set to STE10/100A and a receive poll demand command should be issued (if the receive poll demand is not issued, the receive process will resume when a new recognized frame is received).	0	RO/LH*
6	RCI	Receive completed interrupt. 1: when a frame reception is completed.	0	RO/LH*
5	TUF	Transmit under-flow. 1: when an under-flow condition occurs in the transmit FIFO during transmitting. The transmit process will enter the suspended state and report the under-flow error on bit 1 of TDES0.	0	RO/LH*

Table 8. Control/status register description (continued)

Bit #	Name	Description	Default	RW type
4	---	Reserved		
3	TJT	Transmit jabber timer time-out. 1: when the transmit jabber timer expires. The transmit processor will enter the stop state and TO (bit 14 of TDES0, transmit jabber time-out flag) will be asserted.	0	RO/LH*
2	TDU	Transmit descriptor unavailable. 1: when the next transmit descriptor can not be obtained by the STE10/100A. The transmission process is suspended in this situation. To restart the transmission process, the ownership bit of the next transmit descriptor should be set to STE10/100A and, if the transmit automatic polling is not enabled, a transmit poll demand command should then be issued.	0	RO/LH*
1	TPS	Transmit process stopped. 1: while transmit state = stop	0	RO/LH*
0	TCI	Transmit completed interrupt. 1: set when a frame transmission completes with IC (bit 31 of TDES1) asserted in the first transmit descriptor of the frame	0	RO/LH*
LH = High Latching and cleared by writing 1.				
CSR6 (offset = 30h), NAR - Network access register				
31~22	---	Reserved		
21	SF	Store and forward for transmit 0: disable 1: enable, ignore the transmit threshold setting	0	R/W*
20	---	Reserved		
19	SQE	SQE disable 0: enable SQE function for 10BASE-T operation. The STE10/100A provides SQE test function for 10BASE-T half duplex operation. 1: disable SQE function.	1	R/W*
18~16	-----	Reserved		
15~14	TR	Transmit threshold control 00: 128-bytes (100Mbps), 72-bytes (10Mbps) 01: 256-bytes (100Mbps), 96-bytes (10Mbps) 10: 512-bytes (100Mbps), 128-bytes (10Mbps) 11: 1024-bytes (100Mbps), 160-bytes (10Mbps)	00	R/W*
13	ST	Stop transmit 0: stop (default) 1: start	0	R/W

Table 8. Control/status register description (continued)

Bit #	Name	Description	Default	RW type
12	FC	Force collision mode 0: disable 1: generate collision upon transmit (for testing in loop-back mode)	0	R/W**
11, 10	OM	Operating mode 00: normal 01: MAC loop-back, regardless of contents of XLBEN (bit 14 of XR0, XCVR loop-back) 10,11: reserved	00	R/W**
9, 8	---	Reserved		
7	MM	Multicast mode 1: receive all multicast packets	0	R/W***
6	PR	Promiscuous mode 1: receive any good packet. 0: receive only the right destination address packets	1	R/W***
5	SBC	Stop back-off counter 1: back-off counter stops when carrier is active, and resumes when carrier is dropped. 0: back-off counter is not effected by carrier	0	R/W**
4	---	Reserved		
3	PB	Pass bad packet 1: receives any packets passing address filter, including runt packets, CRC error, truncated packets. For receiving all bad packets, PR (bit 6 of CSR6) should be set to 1. 0: filters all bad packets	0	R/W***
2	---	Reserved		
1	SR	Start/stop receive 0: receive processor will enter stop state after the current frame reception is completed. This value is effective only when the receive processor is in the running or suspending state. Note: In “Stop Receive” state, the PAUSE packet and remote wake up packet will not be affected and can be received if the corresponding function is enabled. 1: receive processor will enter running state.	0	R/W
0	---	Reserved		

W* = only write when the transmit processor stopped.

W** = only write when the transmit and receive processor both stopped.

W*** = only write when the receive processor stopped.

Table 8. Control/status register description (continued)

Bit #	Name	Description	Default	RW type
CSR7 (offset = 38h), IER - Interrupt enable register				
31~17	---	Reserved		
16	NIE	Normal interrupt enable. 1: enables all the normal interrupt bits (see bit 16 of CSR5).	0	R/W
15	AIE	Abnormal interrupt enable. 1: enables all the abnormal interrupt bits (see bit 15 of CSR5).	0	R/W
14	---	Reserved		
13	FBEIE	Fatal bus error interrupt enable. 1: this bit in conjunction with AIE (bit 15 of CSR7) will enable the fatal bus error interrupt.	0	R/W
12	---	Reserved		
11	GPTIE	General purpose timer interrupt enable. 1: this bit in conjunction with AIE (bit 15 of CSR7) will enable the general purpose timer expired interrupt.	0	R/W
10	---	Reserved		
9	RWTIE	Receive watchdog time-out interrupt enable 1: this bit in conjunction with AIE (bit 15 of CSR7) will enable the receive watchdog time-out interrupt	0	R/W
8	RSIE	Receive stopped interrupt enable. 1: this bit in conjunction with AIE (bit 15 of CSR7) will enable the receive stopped interrupt.	0	R/W
7	RUIE	Receive descriptor unavailable interrupt enable. 1: this bit in conjunction with AIE (bit 15 of CSR7) will enable the receive descriptor unavailable interrupt.	0	R/W
6	RCIE	Receive completed interrupt enable. 1: this bit in conjunction with NIE (bit 16 of CSR7) will enable the receive completed interrupt.	0	R/W
5	TUIE	Transmit under-flow interrupt enable. 1: this bit in conjunction with AIE (bit 15 of CSR7) will enable the transmit under-flow interrupt.	0	R/W
4	---	Reserved		
3	TJTTIE	Transmit jabber timer time-out interrupt enable. 1: this bit in conjunction with AIE (bit 15 of CSR7) will enable the transmit jabber timer time-out interrupt.	0	R/W

Table 8. Control/status register description (continued)

Bit #	Name	Description	Default	RW type
2	TDUIE	Transmit descriptor unavailable interrupt enable. 1: this bit in conjunction with NIE (bit 16 of CSR7) will enable the transmit descriptor unavailable interrupt.	0	R/W
1	TPSIE	Transmit processor stopped interrupt enable. 1: this bit in conjunction with AIE (bit 15 of CSR7) will enable the transmit processor stopped interrupt.	0	R/W
0	TCIE	Transmit completed interrupt enable. 1: this bit in conjunction with NIE (bit 16 of CSR7) will enable the transmit completed interrupt.	0	R/W
CSR8 (offset = 40h), LPC - Lost packet counter				
31~17	---	Reserved		
16	LPCO	Lost packet counter overflow. 1: when lost packet counter overflow occurs. Cleared after read.	0	RO/LH
15~0	LPC	Lost packet counter. The counter is incremented whenever a packet is discarded as a result of no host receive descriptors being available. Cleared after read.	0	RO/LH
CSR9 (offset = 48h), SPR - Serial port register				
31~15	---	Reserved		
14	SRC	Serial EEPROM read control. When set, enables read access from EEPROM, when SRS (CSR9 bit 11) is also set.	0	R/W
13	SWC	Serial EEPROM write control. When set, enables write access to EEPROM, when SRS (CSR9 bit 11) is also set.	0	R/W
12	---	Reserved		
11	SRS	Serial EEPROM select. When set, enables access to the serial EEPROM (see description of CSR9 bit 14 and CSR9 bit 13).	0	R/W
10~4	---	Reserved		
3	SDO	Serial EEPROM data out. This bit serially shifts data from the EEPROM to the STE10/100A.	1	RO
2	SDI	Serial EEPROM data in. This bit serially shifts data from the STE10/100A to the EEPROM.	1	R/W

Table 8. Control/status register description (continued)

Bit #	Name	Description	Default	RW type
1	SCLK	Serial EEPROM clock. High/Low this bit to provide the clock signal for EEPROM.	1	R/W
0	SCS	Serial EEPROM chip select. 1: selects the serial EEPROM chip.	1	R/W
CSR11 (offset = 58h), TMR - General - Purpose timer				
31~17	---	Reserved		
16	COM	Continuous operation mode. 1: sets the general-purpose timer in continuous operating mode.	0	R/W
15~0	GTV	General-purpose timer value. Sets the counter value. This is a count-down counter with a cycle time of 204us.	0	R/W
CSR13 (offset = 68h), WCSR – Wake-up control/status register				
31	---	Reserved		
30	CRCT	CRC-16 type 0: Initial contents = 0000h 1: Initial contents = FFFFh	0	R/W
29	WP1E	Wake-up pattern one matched enable	0	R/W
28	WP2E	Wake-up pattern two matched enable	0	R/W
27	WP3E	Wake-up pattern three matched enable	0	R/W
26	WP4E	Wake-up pattern four matched enable	0	R/W
25	WP5E	Wake-up pattern five matched enable	0	R/W
24-18	---	Reserved		
17	LinkOFF	Link off detect enable. The STE10/100A will set the LSC bit of CSR13 after it has detected that link status has switched from ON to OFF.	0	R/W
16	LinkON	Link on detect enable. The STE10/100A will set the LSC bit of CSR13 after it has detected that link status has switched from OFF to ON.	0	R/W
15-11	---	Reserved		
10	WFRE	Wake-up frame received enable. The STE10/100A will include the “Wake-up Frame Received” event in its set of wake-up events. If this bit is set, STE10/100A will assert PMEST bit of PMR1 (CR49) after STE10/100A has received a matched wake-up frame.	0	R/W

Table 8. Control/status register description (continued)

Bit #	Name	Description	Default	RW type
9	MPRE	Magic packet received enable. The STE10/100A will include the “Magic Packet Received” event in its set of wake-up events. If this bit is set, STE10/100A will assert PMEST bit of PMR1 (CR49) after STE10/100A has received a Magic packet.	Default 1 if PM & WOL bits of CSR 18 are both enabled.	R/W
8	LSCE	Link status changed enable. The STE10/100A will include the “Link status changed” event in its set of wake-up events. If this bit is set, STE10/100A will assert PMEST bit of PMR1 after STE10/100A has detected a link status changed event.	0	R/W
7-3	---	Reserved		
2	WFR	Wake-up frame received, 1: Indicates STE10/100A has received a wake-up frame. It is cleared by writing a 1 or upon power-up reset. It is not affected by a hardware or software reset.	X	R/W1C*
1	MPR	Magic packet received, 1: Indicates STE10/100A has received a magic packet. It is cleared by writing a 1 or upon power-up reset. It is not affected by a hardware or software reset.	X	R/W1C*
0	LSC	Link status changed, 1: Indicates STE10/100A has detected a link status change event. It is cleared by writing a 1 or upon power-up reset. It is not affected by a hardware or software reset.	X	R/W1C*

R/W1C*: Read only and write one cleared.

CSR14 (offset = 70h), WPDR – Wake-up pattern data register

Offset	31 16	15 8	7 0
0000h	Wake-up pattern 1 mask bits 31:0		
0004h	Wake-up pattern 1 mask bits 63:32		
0008h	Wake-up pattern 1 mask bits 95:64		
000ch	Wake-up pattern 1 mask bits 127:96		
0010h	CRC16 of pattern 1	Reserved	Wake-up pattern 1 offset
0014h	Wake-up pattern 2 mask bits 31:0		
0018h	Wake-up pattern 2 mask bits 63:32		
001ch	Wake-up pattern 2 mask bits 95:64		
0020h	Wake-up pattern 2 mask bits 127:96		

Table 8. Control/status register description (continued)

Bit #	Name	Description	Default	RW type
0024h		CRC16 of pattern 2	Reserved	Wake-up pattern 2 offset
0028h		Wake-up pattern 3 mask bits 31:0		
002ch		Wake-up pattern 3 mask bits 63:32		
0030h		Wake-up pattern 3 mask bits 95:64		
0034h		Wake-up pattern 3 mask bits 127:96		
0038h		CRC16 of pattern 3	Reserved	Wake-up pattern 3 offset
003ch		Wake-up pattern 4 mask bits 31:0		
0040h		Wake-up pattern 4 mask bits 63:32		
0044h		Wake-up pattern 4 mask bits 95:64		
0048h		Wake-up pattern 4 mask bits 127:96		
004ch		CRC16 of pattern 4	Reserved	Wake-up pattern 4 offset
0050h		Wake-up pattern 5 mask bits 31:0		
0054h		Wake-up pattern 5 mask bits 63:32		
0058h		Wake-up pattern 5 mask bits 95:64		
005ch		Wake-up pattern 5 mask bits 127:96		
0060h		CRC16 of pattern 5	Reserved	Wake-up pattern 5 offset
Offset value is from 0-255 (8-bit width). To load the whole wake-up frame filtering information, consecutive 25 long words write operation to CSR14 should be done.				
CSR15 (offset = 78h), WTMR - Watchdog timer				
31~6	---	Reserved		
5	RWR	Receive watchdog release. The time (in bit-times) from sensing dropped carrier to releasing watchdog timer. 0: 24 bit-times 1: 48 bit-times		
4	RWD	Receive watchdog disable 0: If the received packet's length exceeds 2560 bytes, the watchdog timer will expire. 1: disable the receive watchdog.		
3	---	Reserved		

Table 8. Control/status register description (continued)

Bit #	Name	Description	Default	RW type
2	JCLK	Jabber clock 0: cut off transmission after 2.6 ms (100Mbps) or 26 ms (10Mbps). 1: cut off transmission after 2560 byte-time.		
1	NJ	Non-Jabber 0: if jabber expires, re-enable transmit function after 42 ms (100Mbps) or 420ms (10Mbps). 1: immediately re-enable the transmit function after jabber expires.		
0	JBD	Jabber disable 1: disable transmit jabber function		
CSR16 (offset = 80h), ACSR5 - Assistant CSR5 (Status register 2)				
31	TEIS	Transmit early interrupt status Transmit early interrupt status is set to 1 when TEIE (bit 31 of CSR17 set) is enabled and the transmitted packet is moved from descriptors to the TX-FIFO buffer. This bit is cleared by writing a 1.	0	RO/LH*
30	REIS	Receive early interrupt status. Receive early interrupt status is set to 1 when REIE (CSR17 bit 30) is enabled and the received packet has filled up its first receive descriptor. This bit is cleared by writing a 1.	0	RO/LH*
29	XIS	Transceiver (XCVR) interrupt status. Formed by the logical OR of XR8 bits 6~0.	1	RO/LH*
28	TDIS	Transmit deferred interrupt status.	0	RO/LH*
27	---	Reserved		
26	PFR	PAUSE frame received interrupt status. 1: indicates receipt of a PAUSE frame while the PAUSE function is enabled.	0	RO/LH*
25~ 23	BET	Bus error type. This field is valid only when FBE (CSR5 bit 13, fatal bus error) is set. There is no interrupt generated by this field. 000: parity error, 001: master abort, 010: target abort. 011, 1xx: reserved	000	RO

Table 8. Control/status register description (continued)

Bit #	Name	Description	Default	RW type
22~ 20	TS	Transmit state. Reports the current transmission state only, no interrupt will be generated. 000: stop 001: read descriptor 010: transmitting 011: FIFO fill, read the data from memory and put into FIFO 100: reserved 101: reserved 110: suspended, unavailable transmit descriptor or FIFO overflow 111: write descriptor	000	RO
19~17	RS	Receive state. Reports current receive state only, no interrupt will be generated. 000: stop 001: read descriptor 010: check this packet and pre-fetch next descriptor 011: wait for receiving data 100: suspended 101: write descriptor 110: flush the current FIFO 111: FIFO drain, move data from receiving FIFO into memory	000	RO
16	ANISS	Added normal interrupt status summary. 1: whenever any of the added normal interrupts occur.	0	RO/LH*
15	AAISS	Added abnormal interrupt status summary. 1: whenever any of the added abnormal interrupts occur.	1	RO/LH*
14~0		These bits are the same as the status register of CSR5, and are accessible through either CSR5 or CSR16.		
LH* = High Latching and cleared by writing 1				
CSR17 (offset = 84h), ACSR7- Assistant CSR7 (Interrupt enable register 2)				
31	TEIE	Transmit early interrupt enable	0	R/W
30	REIE	Receive early interrupt enable	0	R/W
29	XIE	Transceiver (XCVR) interrupt enable	0	R/W
28	TDIE	Transmit deferred interrupt enable	0	R/W
27	---	Reserved		
26	PFRIE	PAUSE frame received interrupt enable	0	R/W
25~17	---	Reserved		

Table 8. Control/status register description (continued)

Bit #	Name	Description	Default	RW type
16	ANISE	Added normal interrupt summary enable. 1: adds the interrupts of bits 30 and 31 of ACSR7 (CSR17) to the normal interrupt summary (bit 16 of CSR5).	0	R/W
15	AAIE	Added abnormal interrupt summary enable. 1: adds the interrupt of bits 27, 28, and 29 of ACSR7 (CSR17) to the abnormal interrupt summary (bit 16 of CSR5).	0	R/W
14~0		These bits are the same as the interrupt enable register of CSR7, and are accessible through either CSR7 or CSR16.		
CSR18 (offset = 88h), CR - Command register bit31 to bit16 automatically recall from EEPROM				
31	D3CS	D3cold power state wake up support. If this bit is reset then bit 31 of PMR0 will be reset to '0'. If this bit is asserted and an auxiliary power source is detected then bit 31 of PMR0 will be set to '1'.	0 from EEPROM	R/W
30-28	AUXCL	Aux. current load. These three bits report the maximum 3.3Vaux current requirements for STE10/100A chip. If bit 31 of PMR0 is '1', the default value is 111b, which means the STE10/100A need 375 mA to support remote wake-up in D3cold power state. Otherwise, the default value is 000b, which means the STE10/100A does not support remote wake-up from D3cold power state.	000b from EEPROM	R/W
27-24	--	Reserved		
23	4LEDmode_on	This bit is used to control the LED mode selection. If this bit is reset, mode 1 (3 LEDs) is selected; the LEDs definition is: - 100/10 speed - Link/activity - Full duplex/collision If this bit is set, mode 2 (4 LEDs) is selected; the LEDs definition is: - 100 link - 10 link - Activity - Full duplex/collision	0 from EEPROM	R/W
22, 21	RFS	Receive FIFO size control 11: 1K bytes 10: 2K bytes 01,00: reserved	10 from EEPROM	R/W
20	---	Reserved		

Table 8. Control/status register description (continued)

Bit #	Name	Description	Default	RW type
19	PM	Power management. Enables the STE10/100A power management abilities. When this bit is set into “0” the STE10/100A will set the Cap_Ptr register to zero, indicating no PCI compliant power management capabilities. The value of this bit will be mapped to NC (CR1 bit 20). In PCI power management mode, the wake up frames include “Magic Packet”, “Unicast”, and “Muliticast”.	X from EEPROM	RO
18	WOL	Wake on LAN mode enable. When this bit is set to ‘1’, then the STE10/100A enters wake on LAN mode and enters the sleep state. Once the STE10/100A enters the sleep state, it remains there until: the wake up event occurs, the WOL bit is cleared, or a reset (software or hardware) happens. In wake on LAN mode the wake-up frame is “Magic Packet” only.	X from EEPROM	R/W
17~7	---	Reserved		
6	RWP	Reset wake-up pattern data register pointer	0	R/W
5	PAUSE	Disable or enable the PAUSE function for flow control. The default value of PAUSE is determined by the result of auto-negotiation. The driver software can overwrite this bit to enable or disable it after the auto-negotiation has completed. 0: PAUSE function is disabled. 1: PAUSE function is enabled	Depends on the result of auto-negotiation	R/W
4	RTE	Receive threshold enable. 1: the receive FIFO threshold is enabled. 0: disable the receive FIFO threshold selection in DRT (bits 3~2), and the receive threshold is set to the default 64 bytes.	0	R/W
3~2	DRT	Drain receive threshold 00: 32 bytes (8 DW) 01: 64 bytes (16 DW) 10: store-and -forward 11: reserved	01	R/W
1	SINT	Software interrupt.	0	R/W
0	ATUR	1: enable automatically transmit-underrun recovery.	0	R/W

Table 8. Control/status register description (continued)

Bit #	Name	Description	Default	RW type
CSR19 (offset = 8ch), PCIC - PCI bus performance counter				
31~16	CLKCNT	The number of PCI clocks from read request asserted to access completed. This PCI clock count is accumulated for all the read command cycles from the last CSR19 read to the current CSR19 read.	0	RO*
15~8	---	Reserved		
7~0	DWCNT	The number of double words accessed by the last bus master. This double word count is accumulated for all bus master data transactions from the last CSR19 read to the current CSR19 read.	0	RO*
RO* = Read only and cleared by reading.				
CSR20 (offset = 90h), PMCSR - Power management command and status (The same register value mapping to CR49-PMR1)				
31~16	---	Reserved		
15	PMES	PME_Status. This bit is set whenever the STE10/100A detects a wake up event, regardless of the state of the PME-En bit. Writing a “1” to this bit will clear it, causing the STE10/100A to deassert PME# (if so enabled). Writing a “0” has no effect.	0	RO
14,13	DSCA..	Data_Scale. Indicates the scaling factor to be used when interpreting the value of the data register. This field is required for any function that implements the data register. The STE10/100A does not support data register and Data_Scale.	00b	RO
12~9	DSEL	Data_Select. This four bit field is used to select which data is to be reported through the data register and Data_Scale field. This field is required for any function that implements the data register. The STE10/100A does not support Data_select.	0000b	RO
8	PME_En	PME_En. When set, enables the STE10/100A to assert PME#. When cleared, disables the PME# assertion.	0	RO
7~2	---	Reserved	000000b	RO

Table 8. Control/status register description (continued)

Bit #	Name	Description	Default	RW type
1,0	PWRS	PowerState, this two-bit field is used both to determine the current power state of the STE10/100A and to set the STE10/100A into a new power state. The definition of this field is given below. 00b - D0 01b - D1 10b - D2 11b - D3hot If software attempts to write an unsupported state to this field, the write operation will complete normally on the bus, but the data is discarded and no state change occurs.	00b	RO
CSR23 (offset = 9ch), TXBR - Transmit burst count / time-out				
31~21	---	Reserved	1	
20~16	TBCNT	Transmit burst count Specifies the number of consecutive successful transmit burst writes to complete before the transmit completed interrupt will be generated.	0	R/W
15~12	---	Reserved	1	
11~0	TTO	Transmit time-out = (deferred time + back-off time). When TDIE (ACSR7 bit 28) is set, the timer is decreased in increments of 2.56us (@100M) or 25.6us (@10M). If the timer expires before another packet transmit begins, then the TDIE interrupt will be generated.	0	R/W
CSR24 (offset = a0h), FROM - Flash ROM (also the boot ROM) port				
31	bra16_on	This bit is only valid when 4 LEDmode_on (CSR18 bit 23) is set. In this case, when bra16_on is set, pin 87 functions as brA16; otherwise it functions as LED pin – fd/col.	1	R/W
30~28	---	Reserved		
27	REN	Read enable. Clear if read data is ready in DATA, bit7-0 of FROM.	0	R/W
26	WEN	Write enable. Cleared if write completed.	0	R/W
25	---	Reserved		
24~8	ADDR	Flash ROM address	0	R/W
7~0	DATA	Read/Write data of flash ROM	0	R/W

Table 8. Control/status register description (continued)

Bit #	Name	Description	Default	RW type
CSR25 (offset = a4h), PAR0 - Physical address register 0 automatically recalled from EEPROM				
31~24	PAB3	Physical address byte 3	From EEPROM	R/W
23~16	PAB2	Physical address byte 2	From EEPROM	R/W
15~8	PAB1	Physical address byte 1	From EEPROM	R/W
7~0	PAB0	Physical address byte 0	From EEPROM	R/W
CSR26 (offset = a8h), PAR1 - Physical address register 1 automatically recalled from EEPROM				
31~24	---	Reserved		
23~16	---	Reserved		
15~8	PAB5	Physical address byte 5	From EEPROM	R/W
7~0	PAB4	Physical address byte 4	From EEPROM	R/W
For example, physical address = 00-00-e8-11-22-33 - PAR0= 11 e8 00 00 - PAR1= XX XX 33 22 - PAR0 and PAR1 are readable, but can be written only if the receive state is in stopped (CSR5 bits 19-17=000).				
CSR27 (offset = ach), MAR0 - Multicast address register 0				
31~24	MAB3	Multicast address byte 3 (hash table 31:24)	00h	R/W
23~16	MAB2	Multicast address byte 2 (hash table 23:16)	00h	R/W
15~8	MAB1	Multicast address byte 1 (hash table 15:8)	00h	R/W
7~0	MAB0	Multicast address byte 0 (hash table 7:0)	00h	R/W
CSR28 (offset = b0h), MAR1 - Multicast address register 1				
31~24	MAB7	Multicast address byte 7 (hash table 63:56)	00h	R/W
23~16	MAB6	Multicast address byte 6 (hash table 55:48)	00h	R/W
15~8	MAB5	Multicast address byte 5 (hash table 47:40)	00h	R/W
7~0	MAB4	Multicast address byte 4 (hash table 39:32)	00h	R/W
MAR0 and MAR1 are readable, but can be written only if the receive state is in stopped(CSR5 bit19-17=000)				

4.3 Transceiver(XCVR) registers

There are 11 16-bit registers supporting the transceiver portion of STE10/100A, including 7 basic registers defined according to clause 22 “Reconciliation Sublayer and Media Independent Interface” and clause 28 “Physical Layer link signaling for 10 Mb/s and 100 Mb/s auto-negotiation on twisted pair” of the IEEE802.3u standard. In addition, 4 special registers are provided for advanced chip control and status.

Note: Since only double word access is supported for register R/W in the STE10/100A, the higher word (bit 31~16) of the XCVR registers (XR0~XR10) should be ignored.

Table 9. Transceiver registers list

Offset from base address of CSR	Reg. index	Name	Register descriptions
b4h	XR0	XCR	XCVR control register
b8h	XR1	XSR	XCVR status register
bch	XR2	PID1	PHY identifier 1
c0h	XR3	PID2	PHY identifier 2
c4h	XR4	ANA	Auto-negotiation advertisement register
c8h	XR5	ANLPA	Auto-negotiation link partner ability register
cch	XR6	ANE	Auto-negotiation expansion register
d0h	XR7	XMC	XCVR mode control register
d4h	XR8	XCIIS	XCVR configuration information and interrupt status register
d8h	XR9	XIE	XCVR interrupt enable register
dch	XR10	100CTR	100BASE-TX PHY control/status register

Table 10. Transceiver registers description

Bit #	Name	Description	Default	RW type
XR0(offset = b4h) - XCR, XCVR control register. The default value is chosen as listed below.				
15	XRST	Transceiver reset control. 1: reset transceiver. This bit will be cleared by STE10/100A after transceiver reset has completed.	0	R/W
14	XLBEN	Transceiver loop-back mode select. 1: transceiver loop-back mode is selected. OM (CSR6 bits 11,10) of must contain 00.	0	R/W
13	SPSEL	Network speed select. This bit will be ignored if Auto-negotiation is enabled (ANEN, XR0 bit 12). 1:100Mbps is selected. 0:10Mbps is selected.	1	R/W
12	ANEN	Auto-negotiation ability control. 1: Auto-negotiation function is enabled. 0: Auto-negotiation is disabled.	1	R/W
11	PDEN	Power down mode control. 1: transceiver power-down mode is selected. In this mode, the STE10/100A transceivers are turned off.	0	R/W
10	---	reserved	0	RO
9	RSAN	Re-start auto-negotiation process control. 1: Auto-negotiation process will be restarted. This bit will be cleared by STE10/100A after the Auto-negotiation has restarted.	0	R/W
8	DPSEL	Full/half duplex mode select. 1: full duplex mode is selected. This bit will be ignored if auto-negotiation is enabled (ANEN, XR0 bit 12).	0	R/W
7	COLEN	Collision test control. 1: collision test is enabled.	0	R/W
6~0	---	Reserved	0	RO
R/W = Read/Write able. RO = Read only.				
XR1(offset = b8h) - XSR, XCVR status register. All the bits of this register are read only.				
15	T4	100BASE-T4 ability. Always 0, since STE10/100A has no T4 ability.	0	RO
14	TXFD	100BASE-TX full duplex ability. Always 1, since STE10/100A has 100BASE-TX full duplex ability.	1	RO
13	TXHD	100BASE-TX half duplex ability. Always 1, since STE10/100A has 100BASE-TX half duplex ability.	1	RO

Table 10. Transceiver registers description (continued)

Bit #	Name	Description	Default	RW type
12	10FD	10BASE-T full duplex ability. Always 1, since STE10/100A has 10Base-T full duplex ability.	1	RO
11	10HD	10BASE-T half duplex ability. Always 1, since STE10/100A has 10Base-T half duplex ability.	1	RO
10~6	---	Reserved	0	RO
5	ANC	Auto-negotiation completed. 0: Auto-negotiation process incomplete. 1: Auto-negotiation process complete.	0	RO
4	RF	Result of remote fault detection. 0: no remote fault condition detected. 1: remote fault condition detected.	0	RO/LH*
3	AN	Auto-negotiation ability. Always 1, since STE10/100A has auto-negotiation ability.	1	RO
2	LINK	Link status. 0: a link failure condition occured. Readin clears this bit. 1: valid link established.	0	RO/LL*
1	JAB	Jabber detection. 1: jabber condition detected (10Base-T only).	0	RO/LH*
0	EXT	Extended register support. Always 1, since STE10/100A supports extended register	1	RO
LL* = Latching Low and clear by read. LH* = Latching High and clear by read.				
XR2(offset = bch) - PID1, PHY identifier 1				
15~0	PHYID1	Part one of PHY identifier. Assigned to the 3rd to 18th bits of the Organizationally Unique Identifier (The ST OUI is 0080E1 hex).	1C04h	RO
XR3(offset = c0h) - PID2, PHY identifier 2				
15~10	PHYID2	Part two of PHY identifier. Assigned to the 19th to 24th bits of the organizationally unique identifier (OUI).	000000b	RO
9~4	MODEL	Model number of STE10/100A. 6-bit manufacturer's model number.	000001b	RO
3~0	REV	Revision number of STE10/100A. 4-bits manufacturer's revision number.	0000b	RO

Table 10. Transceiver registers description (continued)

Bit #	Name	Description	Default	RW type
XR4(offset = c4h) - ANA, Auto-negotiation advertisement				
15	NXTPG	Next page ability. Always 0; STE10/100A does not provide next page ability.	0	RO
14	---	reserved		
13	RF	Remote fault function. 1: remote fault function present	0	R/W
12,11	---	Reserved		
10	FC	Flow control function ability. 1: supports PAUSE operation of flow control for full duplex link.	1	R/W
9	T4	100BASE-T4 ability. Always 0; STE10/100A does not provide 100BASE-T4 ability.	0	RO
8	TXF	100BASE-TX full duplex ability. 1: 100Base-TX full duplex ability supported	1	R/W
7	TXH	100BASE-TX half duplex ability. 1: 100Base-TX ability supported.	1	R/W
6	10F	10BASE-T full duplex ability. 1: 10Base-T full duplex ability supported.	1	R/W
5	10H	10BASE-T half duplex ability. 1: 10Base-T ability supported.	1	R/W
4~0	SF	Select field. Default 00001=IEEE 802.3	00001	RO
XR5(offset = c8h) - ANLP, Auto-negotiation link partner ability				
15	LPNP	Link partner next page ability. 0: link partner without next page ability. 1: link partner with next page ability.	0	RO
14	LPACK	Received link partner acknowledge. 0: link code word not yet received. 1: link partner successfully received STE10/100A's link code word.	0	RO
13	LPRF	Link partner's remote fault status. 0: no remote fault detected. 1: remote fault detected.	0	RO
12,11	---	Reserved	0	RO
10	LPFC	Link partner's flow control ability. 0: link partner without PAUSE function ability. 1, link partner with PAUSE function ability for full duplex link.	0	RO

Table 10. Transceiver registers description (continued)

Bit #	Name	Description	Default	RW type
9	LPT4	Link partner's 100BASE-T4 ability. 0: link partner without 100BASE-T4 ability. 1: link partner with 100BASE-T4 ability.	0	RO
8	LPTXF	Link partner's 100BASE-TX full duplex ability. 0: link partner without 100BASE-TX full duplex ability. 1: link partner with 100BASE-TX full duplex ability.	0	RO
7	LPTXH	Link partner's 100BASE-TX half duplex ability. 0: link partner without 100BASE-TX. 1: link partner with 100BASE-TX ability.	0	RO
6	LP10F	Link partner's 10BASE-T full duplex ability. 0: link partner without 10BASE-T full duplex ability. 1: link partner with 10BASE-T full duplex ability.	0	RO
5	LP10H	Link partner's 10BASE-T half duplex ability. 0: link partner without 10BASE-T ability. 1: link partner with 10BASE-T ability.	0	RO
4~0	LPSF	Link partner select field. Standard IEEE 802.3 = 00001	0	RO
XR6(offset = cch) - ANE, auto-negotiation expansion				
15~5	---	Reserved	0	RO
4	PDF	Parallel detection fault. 0: no fault detected. 1: a fault detected via parallel detection function.	0	RO/LH*
3	LPNP	Link partner's next page ability. 0: link partner without next page ability. 1: link partner with next page ability.	0	RO
2	NP	STE10/100A's next page ability. Always 0; STE10/100A does not support next page ability.	0	RO
1	PR	Page received. 0: no new page has been received. 1: a new page has been received.	0	RO/LH*
0	LPAN	Link partner auto-negotiation ability. 0: link partner has no auto-negotiation ability. 1: link partner has auto-negotiation ability.	0	RO
LH = High Latching and cleared by reading.				

Table 10. Transceiver registers description (continued)

Bit #	Name	Description	Default	RW type
XR7(offset = d0h) - XMC, XCVR mode control				
15~12	---	Reserved	0	RO
11	LD	Long distance mode of 10BASE-T. 0: normal squelch level. 1: reduced 10Base-T squelch level for extended cable length.	0	R/W
10~0	---	Reserved	0	RO

XR8(offset = d4h) - XCIIS, XCVR configuration information and interrupt status				
15~10	----	Reserved	0	RO
9	SPEED	Speed configuration setting. 0: the speed is 10Mb/s. 1: the speed is 100Mb/s.	1	RO
8	DUPLEX	Duplex configuration setting. 0: the duplex mode is half. 1: the duplex mode is full.	0	RO
7	PAUSE	PAUSE function configuration setting for flow control. 0: PAUSE function is disabled. 1: PAUSE function is enabled	0	RO
6	ANC	Auto-negotiation completed interrupt. 0: Auto-negotiation has not completed yet. 1: Auto-negotiation has completed.	0	RO/LH*
5	RFD	Remote fault detected interrupt. 0: there is no remote fault detected. 1: remote fault is detected.	0	RO/LH*
4	LS	Link fail interrupt. 0: link test status is up. 1: link is down.	0	RO/LH*
3	ANAR	Auto-negotiation acknowledge received interrupt. 0: there is no link code word received. 1: link code word is receive from link partner.	0	RO/LH*
2	PDF	Parallel detection fault interrupt. 0: there is no parallel detection fault. 1: parallel detection is fault.	0	RO/LH*
1	ANPR	Auto-negotiation page received interrupt. 0: there is no auto-negotiation page received. 1: auto-negotiation page is received.	0	RO/LH*

Table 10. Transceiver registers description (continued)

Bit #	Name	Description	Default	RW type
0	REF	Receive error full interrupt. 0: the receive error number is less than 64. 1: 64 error packets is received.	0	RO/LH*
LH = High Latching and cleared by reading.				
XR9(offset = d8h) - XIE, XCVR interrupt enable register				
15~7	---	Reserved		
6	ANCE	Auto-negotiation completed interrupt enable. 0: disable auto-negotiation completed interrupt. 1: enable auto-negotiation complete interrupt.	0	R/W
5	RFE	Remote fault detected interrupt enable. 0: disable remote fault detection interrupt. 1: enable remote fault detection interrupt.	0	R/W
4	LDE	Link down interrupt enable. 0: disable link fail interrupt. 1: enable link fail interrupt.	0	R/W
3	ANAE	Auto-negotiation acknowledge interrupt enable. 0: disable link partner acknowledge interrupt 1: enable link partner acknowledge interrupt.	0	R/W
2	PDFE	Parallel detection fault interrupt enable. 0: disable fault parallel detection interrupt. 1: enable fault parallel detection interrupt.	0	R/W
1	ANPE	Auto-negotiation page received interrupt enable. 0: disable auto-negotiation page received interrupt. 1: enable auto-negotiation page received interrupt.	0	R/W
0	REFE	RX_ERR full interrupt enable. 0: disable rx_err full interrupt. 1: enable rx_err interrupt.	0	R/W
XR10(offset = dch) - 100CTR, 100BASE-TX control register				
15,14	---	Reserved		
13	DISRER	Disable the RX_ERR counter. 0: the receive error counter - RX_ERR is enabled. 1: the receive error counter - RX_ERR is disabled.	0	R/W
12	ANC	Auto-negotiation completed. This bit is the same as bit 5 of XR1. 0: the auto-negotiation process has not completed yet. 1: the auto-negotiation process has completed.	0	RO

Table 10. Transceiver registers description (continued)

Bit #	Name	Description	Default	RW type
11, 10	---	Reserved	1	
9	ENRLB	Enable remote loop-back function. 1: enable remote loop-back (CSR6 bits 11 and 10 must be 00).	0	R/W
8	ENDCR	Enable DC restoration. 0: disable DC restoration. 1: enable DC restoration.	1	R/W
7	ENRZI	Enable the conversions between NRZ and NRZI. 0: disable the data conversion between NRZ and NRZI. 1: enable the data conversion of NRZI to NRZ in receiving and NRZ to NRZI in transmitting.	1	R/W
6	---	Reserved		
5	ISOTX	Transmit Isolation. When 1, isolate from MII and tx+/-. This bit must be 0 for normal operation.	0	R/W
4~2	CMODE	Reports current transceiver operating mode. 000: in auto-negotiation 001: 10Base-T half duplex 010: 100Base-TX half duplex 011: reserved 100: reserved 101: 10Base-T full duplex 110: 100Base-TX full duplex 111: isolation, auto-negotiation disable	000	RO
1	DISMLT	Disable MLT3. 0: the MLT3 encoder and decoder are enabled. 1: the MLT3 encoder and decoder are bypassed.	0	R/W
0	DISCRM	Disable scramble. 0: the scrambler and de-scrambler is enabled. 1: the scrambler and de-scrambler are disabled.	0	R/W

4.4 Descriptors and buffer management

The STE10/100A provides receive and transmit descriptors for packet buffering and management.

4.4.1 Receive descriptor

Table 11. Receive descriptor table

	31				0
RDES0	Own	Status			
RDES1		---	Control	Buffer2 byte-count	Buffer1 byte-count
RDSE2	Buffer1 address (DW boundary)				
RDSE3	Buffer2 address (DW boundary)				

Note: Descriptors and receive buffers addresses must be long-word aligned

Table 12. Receive descriptor description

Bit#	Name	Description
RDES0		
31	OWN	Own bit 1: indicates that newly received data can be put into this descriptor 0: Host has not yet processed the received data currently in this descriptor.
30-16	FL	Frame length, including CRC. This field is valid only in a frame's last descriptor.
15	ES	Error summary. Logical OR of the following bits: 0: overflow 1: CRC error 6: late collision 7: frame too long 11: runt packet 14: descriptor error This field is valid only in a frame's last descriptor.
14	DE	Descriptor error. This bit is valid only in a frame's last descriptor. 1: the current valid descriptor is unable to contain the packet being currently received. The packet is truncated.
13-12	DT	Data type 00: normal 01: MAC loop-back 10: Transceiver loop-back 11: remote loop-back These bits are valid only in a frame's last descriptor.
11	RF	Runt frame (packet length < 64 bytes). This bit is valid only in a frame's last descriptor.
10	MF	Multicast frame. This bit is valid only in a frame's last descriptor.

Table 12. Receive descriptor description (continued)

Bit#	Name	Description
9	FS	First descriptor
8	LS	Last descriptor
7	TL	Packet too long (packet length > 1518 bytes). This bit is valid only in a frame's last descriptor.
6	CS	Late collision. Set when collision is active after 64 bytes. This bit is valid only in a frame's last descriptor
5	FT	Frame type. This bit is valid only in a frame's last descriptor. 0: 802.3 type 1: Ethernet type
4	RW	Receive watchdog (refer to CSR15, bit 4). This bit is valid only in a frame's last descriptor.
3	reserved	Default = 0
2	DB	Dribble bit. This bit is valid only in a frame's last descriptor 1: Packet length is not integer multiple of 8-bit
1	CE	1: CRC error. This bit is valid only in a frame's last descriptor
0	OF	1: Overflow. This bit is valid only in a frame's last descriptor
RDES1		
31~26	---	Reserved
25	RER	Receive end of ring. Indicates this descriptor is last, return to base address of descriptor
24	RCH	Second address chain Used for chain structure, indicating the buffer 2 address is the next descriptor address. Ring mode takes precedence over chained mode
23~22	---	Reserved
21~11	RBS2	Buffer 2 size (DW boundary)
10~ 0	RBS1	Buffer 1 size (DW boundary)
RDES2		
31~0	RBA1	Receive buffer address 1. This buffer address should be double word aligned.
RDES3		
31~0	RBA2	Receive buffer address 2. This buffer address should be double word aligned.

4.4.2 Transmit descriptor

Table 13. Receive descriptor table

	31				0
TDES0	Own	Status			
TDES1		---	Control	Buffer2 byte-count	Buffer1 byte-count
TDSE2	Buffer1 address				
TDSE3	Buffer2 address				

Table 14. Transmit descriptor description

Bit#	Name	Description
TDSE0		
31	OWN	Own bit 1: Indicates this descriptor is ready to transmit 0: No transmit data in this descriptor.
30-24	---	Reserved
23-22	UR	Under-run count
21-16	---	Reserved
15	ES	Error summary. Logical OR of the following bits: 1: under-run error 8: excessive collision 9: late collision 10: no carrier 11: loss carrier 14: jabber time-out
14	TO	Transmit jabber time-out
13-12	-----	Reserved
11	LO	Loss of carrier
10	NC	No carrier
9	LC	Late collision
8	EC	Excessive collision
7	HF	Heartbeat fail
6-3	CC	Collision count
2	-----	Reserved
1	UF	Under-run error
0	DE	Deferred
TDES1		
31	IC	Interrupt completed
30	LS	Last descriptor

Table 14. Transmit descriptor description (continued)

Bit#	Name	Description
29	FS	First descriptor
28,27	---	Reserved
26	AC	Disable add CRC function
25	TER	End of ring
24	TCH	2nd address chain. Indicates that the buffer 2 address is the next descriptor address
23	DPD	Disable padding function
22	---	Reserved
21-11	TBS2	Buffer 2 size
10-0	TBS1	Buffer 1 size
TDES2		
31~0	BA1	Buffer address 1. No alignment limitations imposed on the transmission buffer address.
TDES3		
31~0	BA2	Buffer address 2. No alignment limitations imposed on the transmission buffer address.

5 General EEPROM format description

Table 15. Connection type definition

Offset	Length	Description
0	2	STE10/100A signature: **0x81**, **0x09**
2	1	Format major version: **0x02,** old ROM format version **0x01** is for STE10/100A-MAC only.
3	1	Format minor version: **0x00**
4	4	Reserved
8	6	IEEE network address: **ID1**, **ID2**, **ID3**, **ID4**, **ID5**, **ID6**
E	1	IEEE ID checksum1: **Sm0**=0, **carry**=0 **SUM**=**Sm6** where **Smi**=(**Smi-1**<<1)+(**carry** from shift)^**IDi**
F	1	IEEE ID checksum2: Reserved, should be **zero.**
10	1	PHY type, **0xFF**: **Internal** PHY (STE10/100A only)
11	1	Reserved, should be **zero**
12	2	Default connection type, see Table 15
14	0B	Reserved, should be **zero**
1F	1	Flow control field, **00**: Disable flow control function, **01**: Enable flow control function.
20	2	PCI device ID
22	2	PCI vendor ID
24	2	PCI subsystem ID
26	2	PCI subsystem vendor ID
28	1	**MIN_GNT** value
29	1	**MAX_LAT** value
2A	4	Cardbus **CIS** pointer
2E	2	CSR18 (**CR**) bit 31-16 recall data
30	4E	Reserved, should be **zero**
7E	2	CheckSum, the least significant two bytes of **FCS** for data stored in offset 0..7D of EEPROM

Table 16. Connection type definition

Name	Description
0xFFFF	Software driver default
0x0100	Auto-negotiation
0x0200	Power-on auto-detection
0x0400	Auto sense
0x0000	10BaseT
0x0001	BNC
0x0002	AUI
0x0003	100BaseTx
0x0004	100BaseT4
0x0005	100BaseFx
0x0010	10BaseT full duplex
0x0013	100BaseTx full duplex
0x0015	100BaseFx full duplex

6 Electrical specifications and timings

Table 17. Absolute maximum ratings

Parameter	Value
Supply voltage(Vcc)	-0.5 V to 7.0 V
Input voltage	-0.5 V to VCC + 0.5 V
Output voltage	-0.5 V to VCC + 0.5 V
Storage temperature	-65 °C to 150 °C(-85° F to 302° F)
Ambient temperature	0° C to 70° C (32° F to 158° F)
ESD protection	2000V

Table 18. General DC specifications

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Units
General DC						
Vcc	Supply voltage		3.14	3.3	3.46	V
Icc	Power supply			130		mA
PCI interface DC specifications						
Vilp	Input LOW voltage		-0.5		0.8	V
Vihp	Input HIGH voltage		2.0		5.5	V
Iilp	Input LOW leakage current	Vin =.8V	-10		10	µA
Iihp	Input HIGH leakage current	Vin = 2.0V	-10		10	µA
Volp	Output LOW voltage	Iout =3mA/6mA	.		.55	V
Vohp	Output HIGH voltage	Iout =-2mA	2.4			V
Cinp	Input pin capacitance		5		8	pF
Cclkp	CLK pin capacitance		5		8	pF
Cidsel	IDSEL pin capacitance		5		8	pF
Lpinp	Pin inductance		N/A			nH
Flash/EEPROM interface DC specifications						
Vilf	Input LOW voltage		-0.5		0.8	V
Vihf	Input HIGH voltage		2.0		5.5	V
Iif	Input leakage current		-10		10	µA
Volf	Output LOW voltage	Iout=3mA,6mA			.55	V
Vohf	Output HIGH voltage	Iout=-2mA	2.4			V
Cinf	Input pin capacitance		5		8	pF

Table 18. General DC specifications (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Units
10BASE-T voltage/current characteristics						
Vida10	Input differential accept peak voltage	5MHz ~ 10MHz	585		3100	mV
Vidr10	Input differential reject peak voltage	5MHz ~ 10MHz	0		585	mV
Vod10	Output differential peak voltage		2200		2800	V
100BASE-TX voltage/current Characteristics						
Vida100	Input differential accept peak voltage		200		1000	mV
Vidr100	Input differential reject peak voltage		0		200	mV
Vod100	Output differential peak voltage		950		1050	V

Table 19. AC specifications

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Units
PCI signaling AC specifications						
Ioh(AC)	Switching current high	Vout=.7Vcc	-32Vcc			mA
Iol(AC)	Switching current low	Vout=.18Vcc			38Vcc	mA
Icl	Low clamp current	-3<Vin<-1	-25+(Vin+1)/.015			mA
Tr	Unloaded output rise time		1		4	V/ns
Tf	Unloaded output fall time		1		4	V/ns

6.1 Timing specifications

Table 20. PCI clock specifications

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Units
Tc	Clock cycle time		30		50	ns
Th	Clock high time		11		--	ns
Tl	Clock low time		11		--	ns
	Clock slew rate		1		4	V/ns

Figure 16. PCI clock waveform

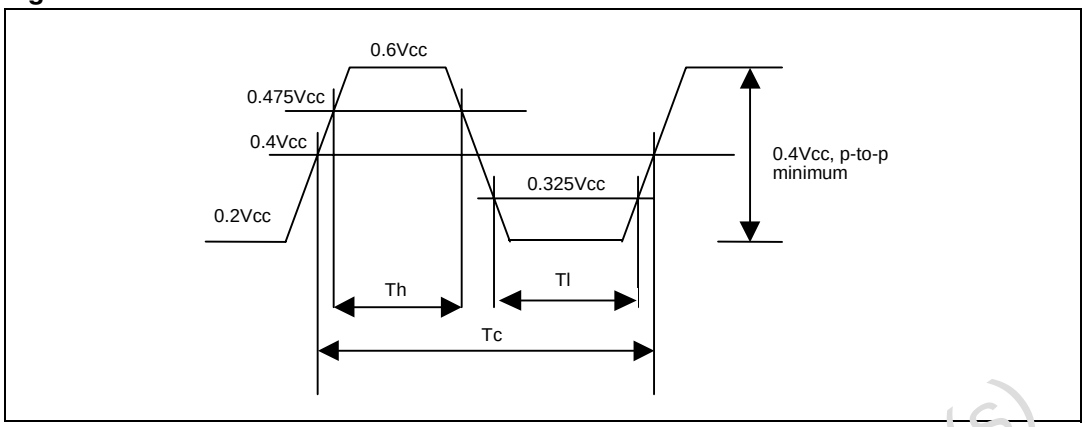


Table 21. X1 specifications

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Units
TX1d	X1 duty cycle		45	50	55	%
TX1p	X1 period			30		ns
TX1t	X1 tolerance				+ / - 50	PPM
$TX1C_L$	X1 load capacitance				18	pF

Table 22. PCI timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Units
Tval	Clock to signal valid delay (bussed signals)		2		11	ns
Tval(ptp)	Clock to signal valid delay (point to point)		2		11	ns
Ton	Float to active delay		2			ns
Toff	Active to float delay				28	ns
Tsu	Input set up time to clock (bussed signals)		7			ns
Tsu(ptp)	Input set up time to clock (point to point)		10,12			ns
Th	Input hold time from clock		0			ns
Th	Input hold time from clock		0			ns
Trst	Reset active time after power stable		1			ms
Trst-clk	Reset active time after clk stable		100			µs
Trst-off	Reset active to output float delay				40	ns

Figure 17. PCI timings

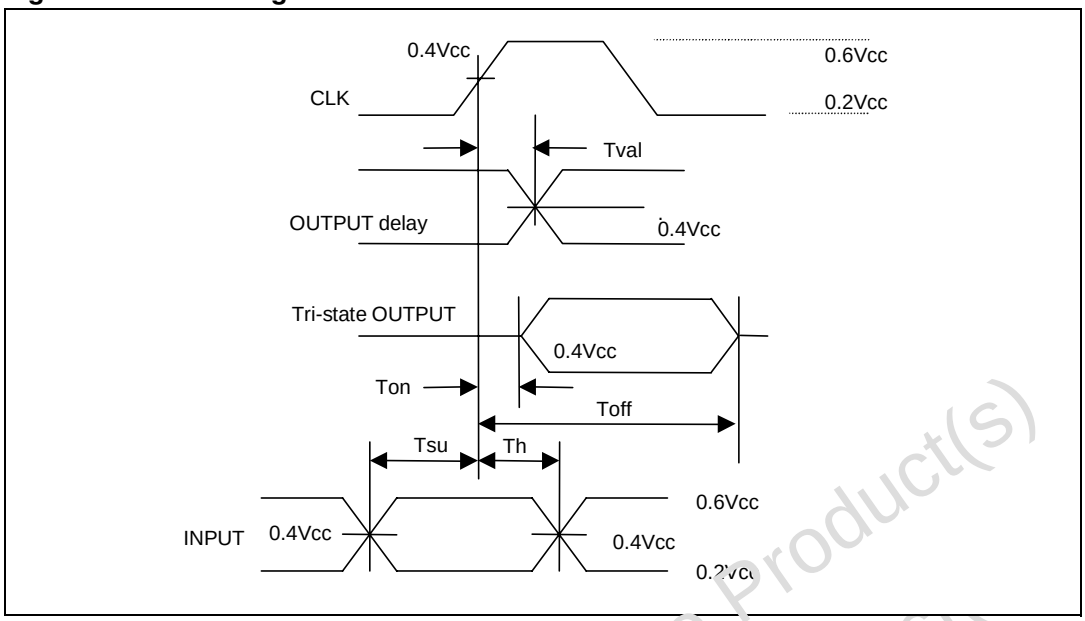


Table 23. Flash interface timings

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Units
Tfcyc	Read/write cycle time					ns
Tfce	Address to read data setup time					ns
Tfce	CS# to read data setup time					ns
Tfoe	OE# active to read data setup time					ns
Tfdf	OE# inactive to data driven delay time					ns
Tfas	Address setup time before WE#					ns
Tfah	Address hold time after WE#					ns
Tfcs	CS# setup time before WE#					ns
Tfch	Address hold time after WE#					ns
Tfds	Data setup time					ns
Tfdh	Data hold time					ns
Tfwpw	Write pulse width					ns
Tfwph	Write pulse width high					ns
Tfasc	Address setup time before CS#					ns
Tfahc	Address hold time after CS#					ns

Figure 18. Flash write timings

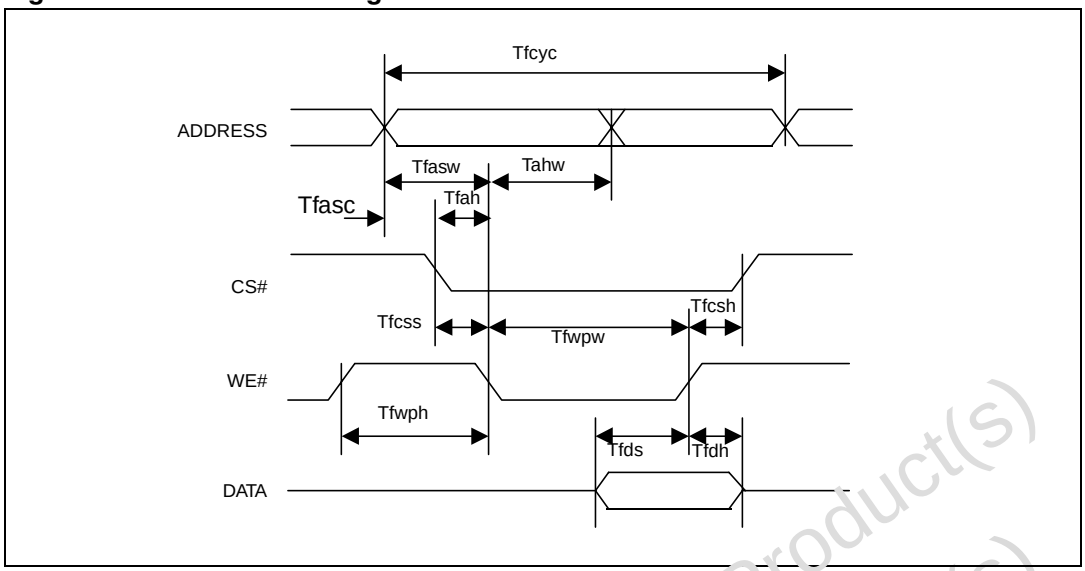


Figure 19. Flash read timings

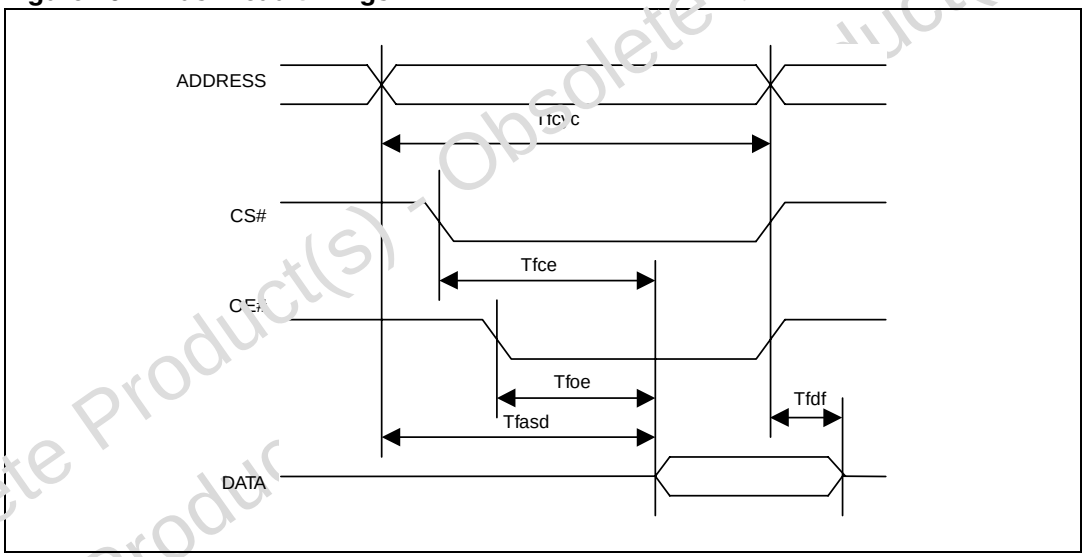


Table 24. EEPROM Interface Timings

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Units
Tscf	Serial clock frequency	Tscf - 1.4 µs		714		kHz
Tecss	Delay from CS high to SK high		0.1	1.7		µs
Tecsh	Delay from SK low to CS low		200	650		ns
Tedts	Setup time of DI to SK		200	600		ns
Tedth	Hold time of DI after SK		0	700		ns
Tecsl	CS low time		0.5	1.1		µs

Figure 20. Serial EEPROM timings

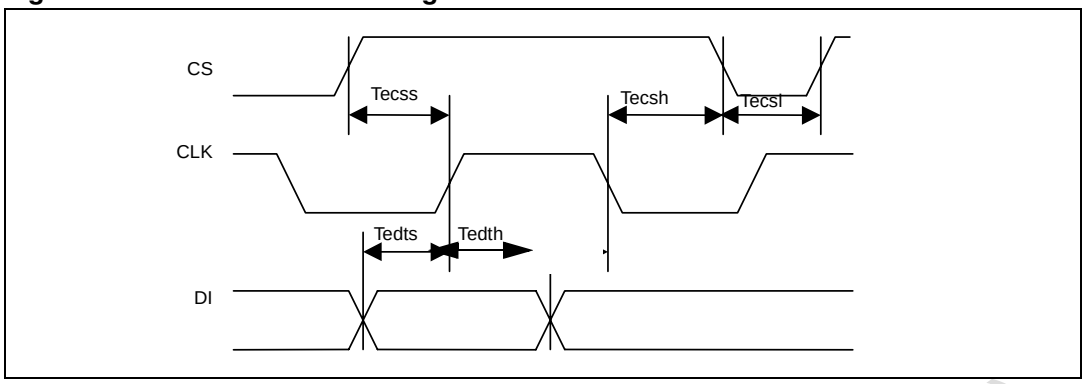


Table 25. 10BASE-T normal link pulse (NLP) timings specifications

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Units
Tnpw	NLP width	10Mbps		100		ns
Tnpc	NLP period	10Mbps	8		24	ms

Figure 21. Normal link pulse timings

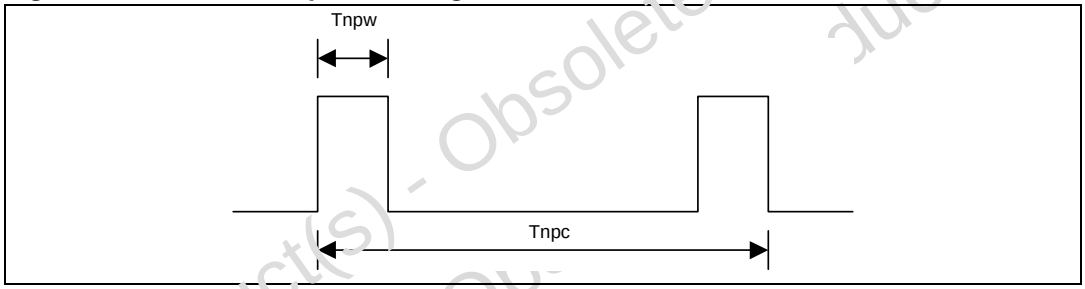


Table 26. Auto negotiation fast link pulse (FLP) timings specifications

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Units
Tflpw	FLP Width			100		ns
Tflcpp	Clock pulse to clock pulse period		111	125	139	µs
Tflcpd	Clock pulse to data pulse period		55.5	62.5	69.5	µs
-	Number of pulses in one burst		17		33	#
Tflbw	Burst width			2		ms
Tflbp	FLP burst period		8	16	24	ms

Figure 22. Fast link pulse timings

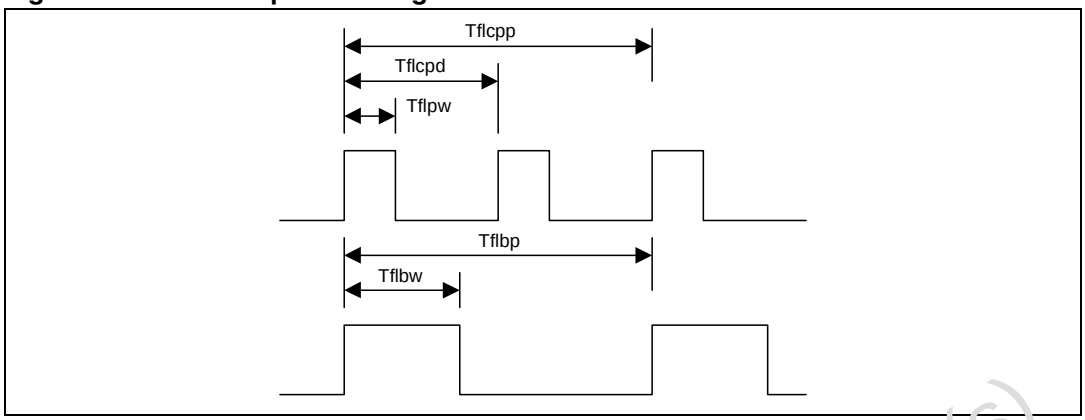


Table 27. 100BASE-TX transmitter AC timings specification

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Units
Tjit	TDP-TDN differential output peak jitter				1.4	ps

7 Package mechanical data

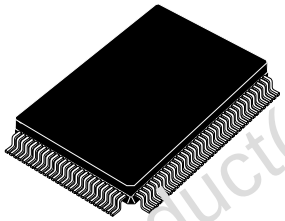
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 23. Package mechanical data

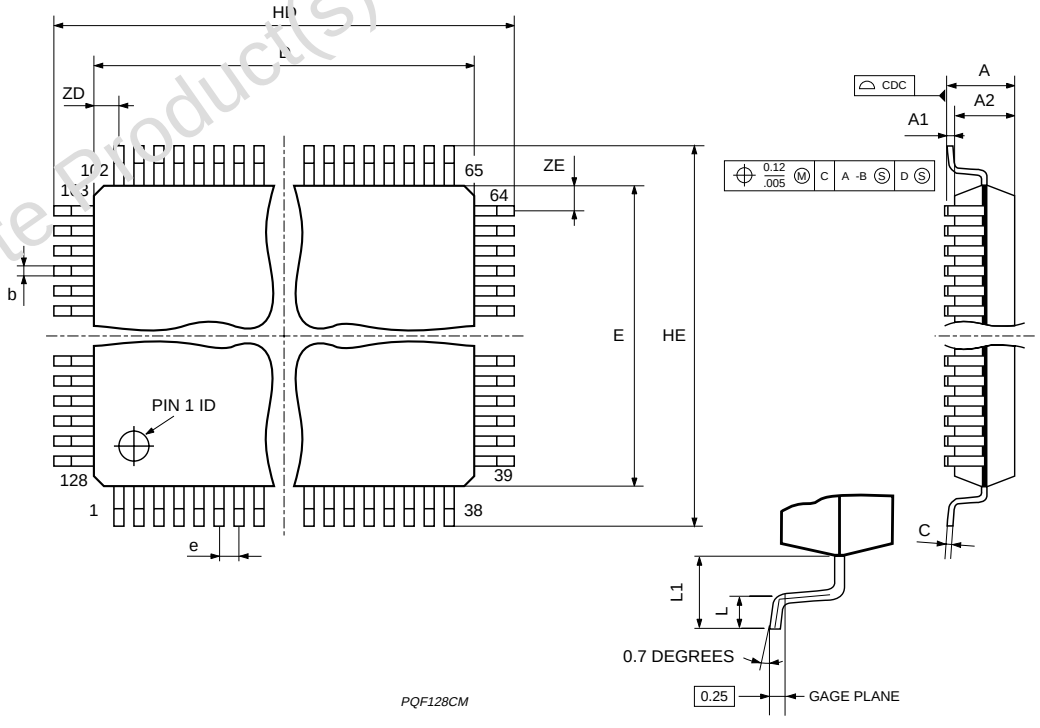
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.04	3.40		0.12	0.134
A1	0.25	0.33		0.010	0.013	
A2	2.57	2.71	2.87	0.101	0.107	0.113
b	0.13		0.28	0.005		0.011
C	0.13		0.23	0.005		0.009
D		20			0.787	
E		14			0.551	
e		0.5			0.02	
HD		23.2			0.913	
HE		17.2			0.677	
L	0.73	0.88	1/03	0.029	0.035	0.041
L1		1.60			0.063	
ZD		0.75			0.03	
ZE		0.75			0.03	
ccc			0.12			0.005
Angle	0°(min.), 7°(max.)					

L dimension is measured at gauge plane at 0.25 above the seating plane

OUTLINE AND MECHANICAL DATA



PQFP128 (14x20x2.7mm)



8 Ordering information

Table 28. Order codes

Part number	Package
E-STE10/100A	PQFP128 (14mm x 20mm x 2.7mm)

9 Revision history

Table 29. Document revision history

Date	Revision	Changes
06-Nov-2002	7	Previous release (as revision A07)
28-Feb-2007	8	Removed the STE10/100E order code and updated the ordering information.

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