



STE180NE10

N-channel 100V - 4.5mΩ - 180A - ISOTOP
STripFET™ Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STE180NE10	100V	<6mΩ	180A

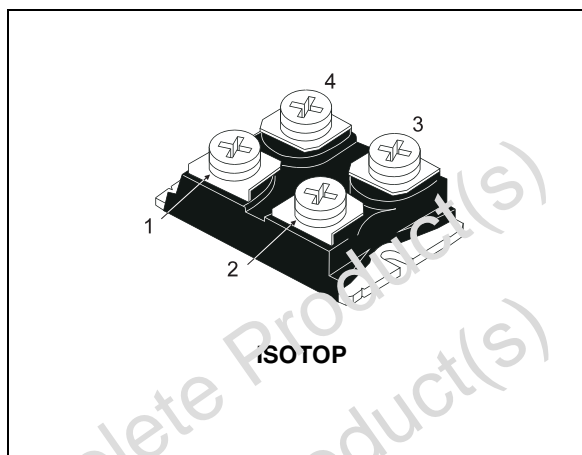
- 100% avalanche tested
- Low intrinsic capacitance
- Gate charge minimized
- Reduced voltage spread

Description

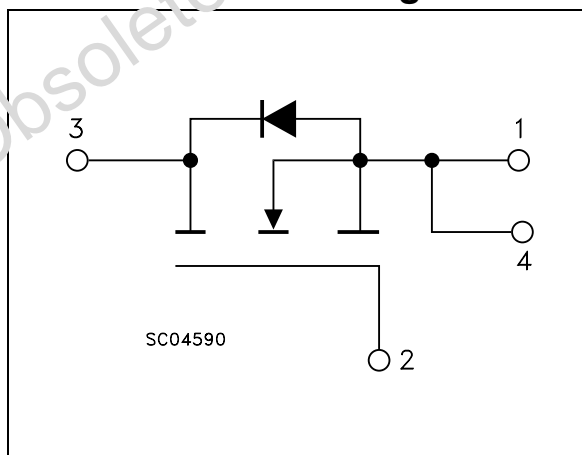
This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps, therefore a remarkable manufacturing reproducibility.

Applications

- Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STE180NE10	E180NE10	ISOTOP	Tube

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Obsolete Product(s) - Obsolete Product(s)
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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	100	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20k\Omega$)	100	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	180	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	119	A
$I_{DM}^{(1)}$	Drain current (pulsed)	360	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	360	W
	Derating factor	2.38	W/ $^\circ\text{C}$
V_{ISO}	Insulation withstand voltage (AC-RMS)	2500	V
T_j T_{stg}	Operating junction temperature storage temperature	-55 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area

Table 2. Thermal data

$R_{thj-case}$	Thermal resistance junction-case max	0.37	$^\circ\text{C}/\text{W}$
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Table 3. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	60	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 25\text{ V}$)	720	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1mA, V _{GS} = 0	100			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = max rating V _{DS} = max rating, T _C = 125°C			4 40	μA μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 20V			± 100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250μA	2	3	4	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10V, I _D = 40A		4.5	6	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward transconductance	V _{DS} > I _{D(on)} × R _{DS(on)max} I _D = 80 A	30			S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} = 25V, f = 1MHz, V _{GS} = 0		21 2.5 0.9		nF nF nF
t _{d(on)} t _r t _{d(off)} t _f	Turn-on delay time Rise time Turn-off delay time Fall time	V _{DD} = 90V, I _D = 490A R _G = 4.7Ω V _{GS} = 10V (see Figure 12)		100 600 430 440		ns ns ns ns
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V _{DD} = 80V, I _D = 180A, V _{GS} = 10V, R _G = 4.7Ω (see Figure 13)		585 120 210	795	nC nC nC

1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5%.

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				180 540	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 180A, V_{GS} = 0$			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 100A,$ $di/dt = 100A/\mu s,$ $V_{DD} = 50V, T_j = 150^\circ C$ (see Figure 14)		235 1.65 14		ns μC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

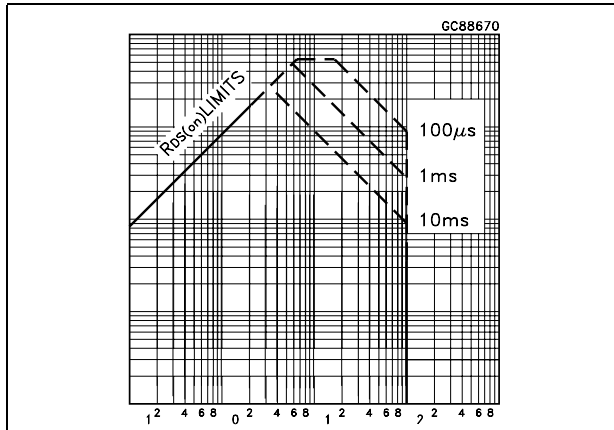


Figure 2. Thermal impedance

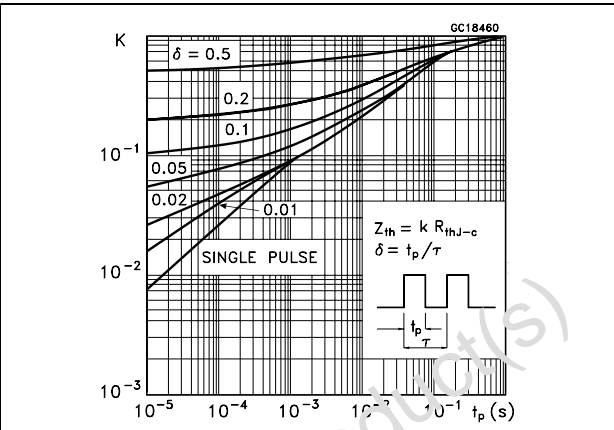


Figure 3. Output characteristics

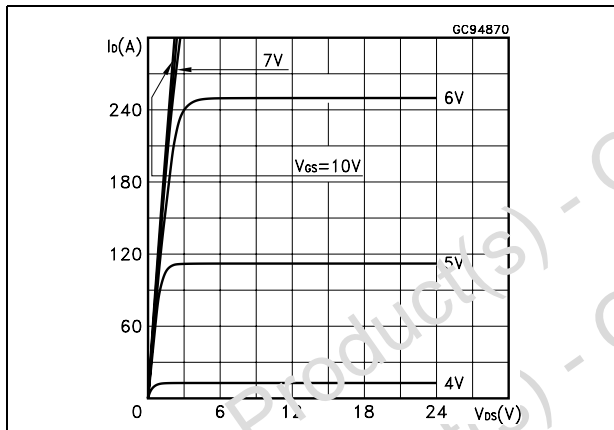


Figure 4. Transfer characteristics

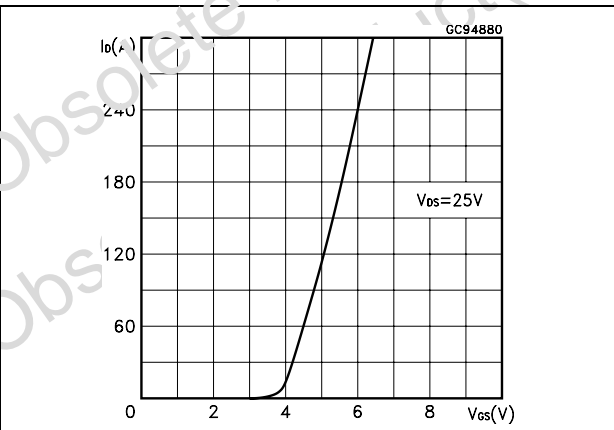


Figure 5. Transconductance

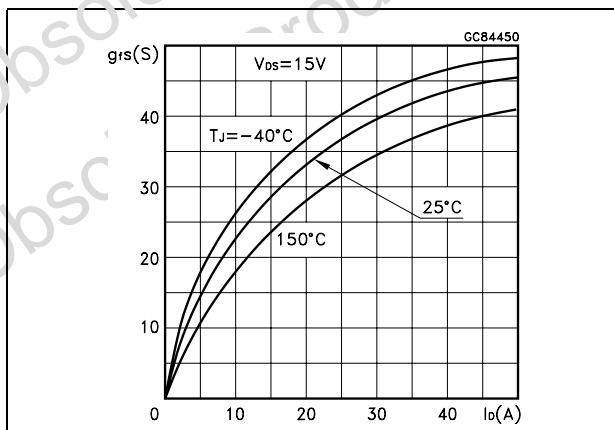


Figure 6. Static drain-source on resistance

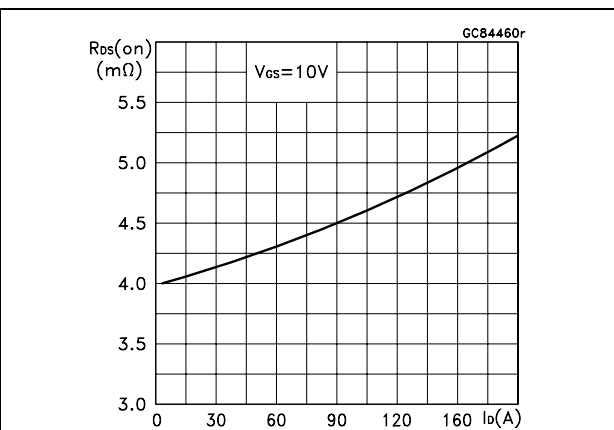


Figure 7. Gate charge vs. gate-source voltage Figure 8. Capacitance variations

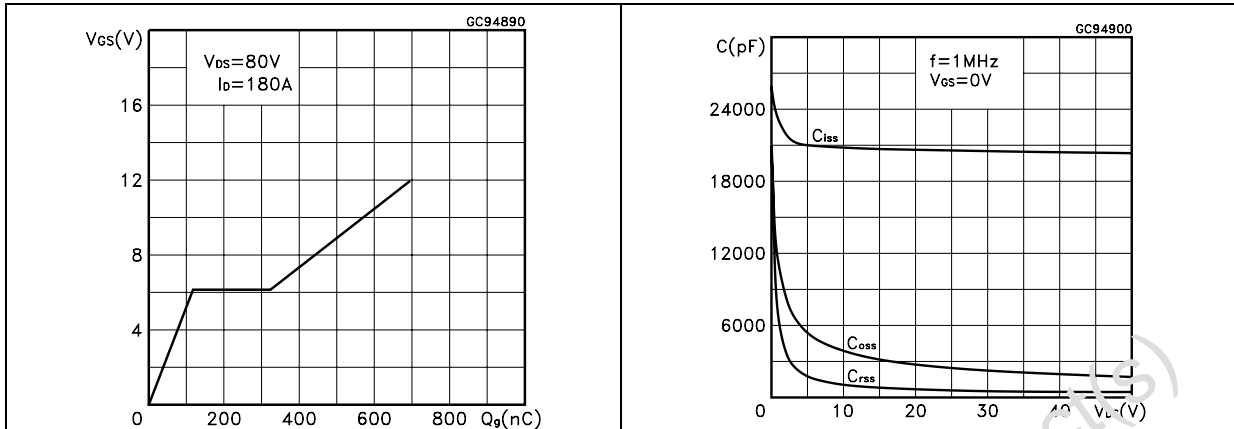


Figure 9. Normalized gate threshold voltage vs. temperature Figure 10. Normalized on resistance vs. temperature

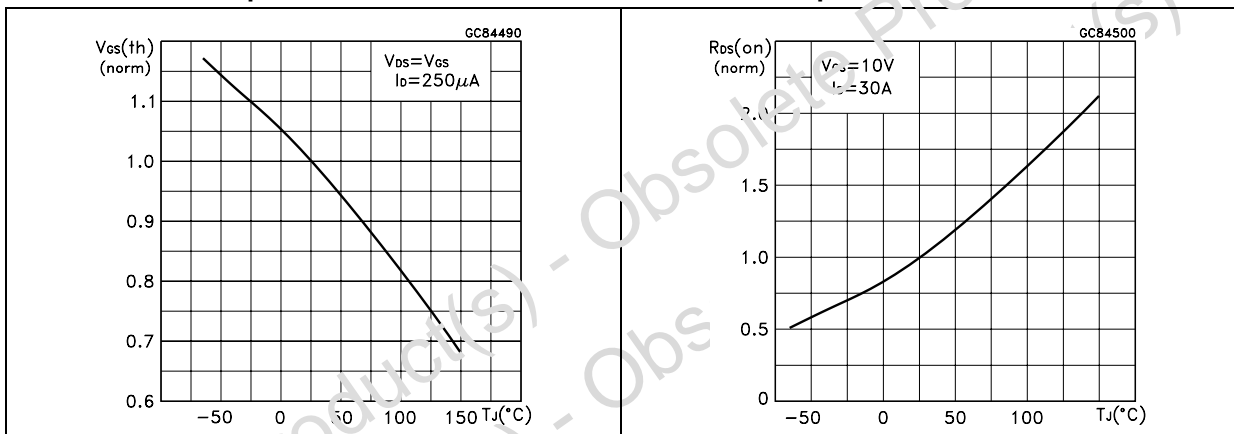
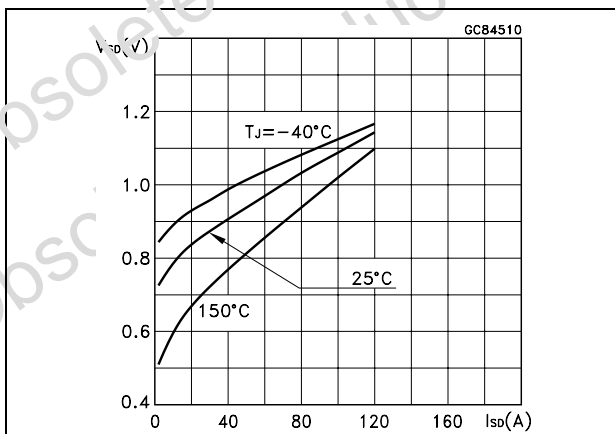


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load

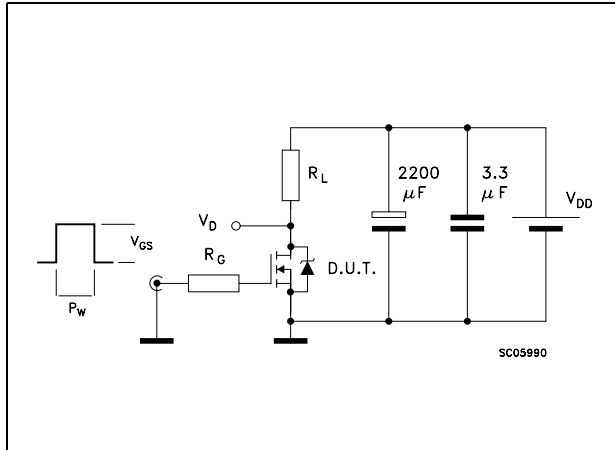


Figure 13. Gate charge test circuit

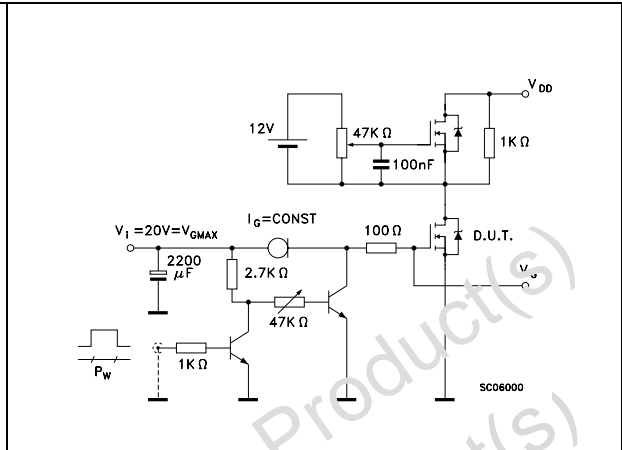


Figure 14. Test circuit for inductive load switching and diode recovery times

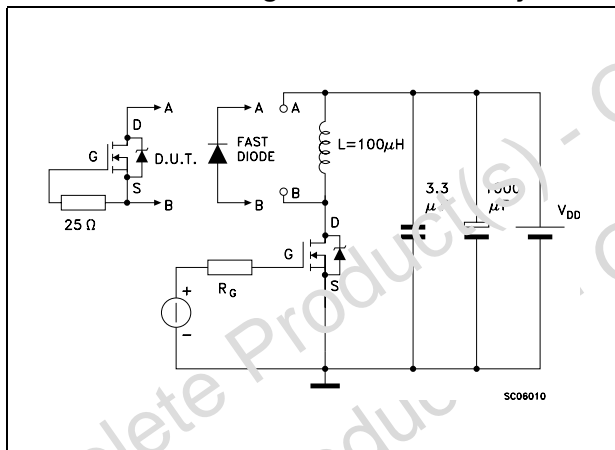


Figure 15. Unclamped Inductive load test circuit

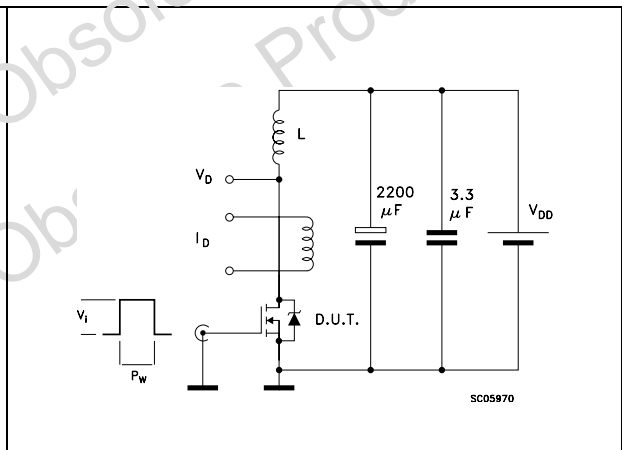


Figure 16. Unclamped inductive waveform

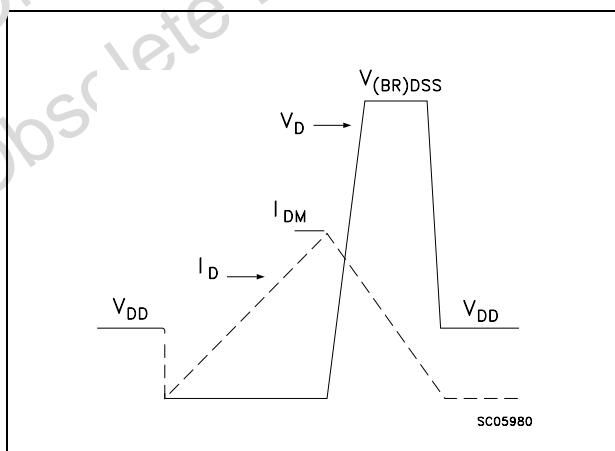
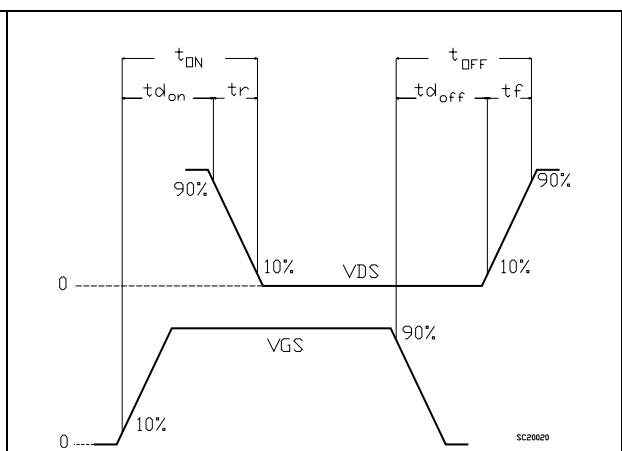


Figure 17. Switching time waveform



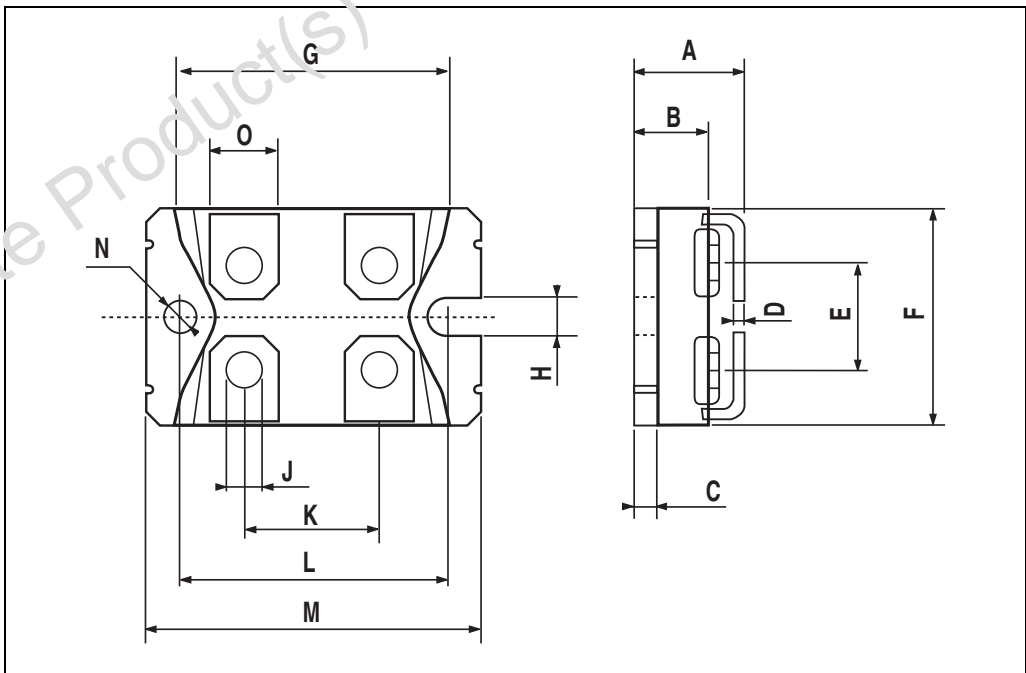
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

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ISOTOP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	11.8		12.2	0.466		0.480
B	8.9		9.1	0.350		0.358
C	1.95		2.05	0.076		0.080
D	0.75		0.85	0.029		0.033
E	12.6		12.8	0.496		0.502
F	25.15		25.5	0.990		1.003
G	31.5		31.7	1.240		1.248
H	4			0.157		
J	4.1		4.3	0.161		0.169
K	14.9		15.1	0.583		0.594
L	30.1		30.3	1.185		1.193
M	37.8		38.2	1.488		1.503
N	4			0.157		
O	7.8		8.2	0.307		0.322



5 Revision history

Table 7. Revision history

Date	Revision	Changes
09-Sep-2004	4	Complete document
03-Aug-2006	5	New template, no content change
20-Feb-2007	6	Typo mistake on page 1

Obsolete Product(s) - Obsolete Product(s)
Obsolete Product(s) - Obsolete Product(s)

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