



16-BIT LOW VOLTAGE ROMLESS MCU

DATASHEET

■ High Performance 16-bit CPU

- CPU Frequency: 0 to 50 MHz
- 40ns instruction cycle time at 50-MHz CPU clock
- 4-stage pipeline
- Register-based design with multiple variable register banks
- Enhanced boolean bit manipulation facilities
- Additional instructions to support HLL and operating systems
- Single-cycle context switching support
- 1024 bytes on-Chip special function register area

■ Memory Organisation

- 1KByte on-chip RAM
- Up to 16 MBytes linear address space for code and data (1 MByte with SSP used)

■ External Memory Interface

- Programmable external bus characteristics for different address ranges
- 8-bit or 16-bit external data bus
- Multiplexed or demultiplexed external address/data buses
- Five programmable chip-select signals
- Hold and hold-acknowledge bus arbitration support

■ One Channel PWM Unit

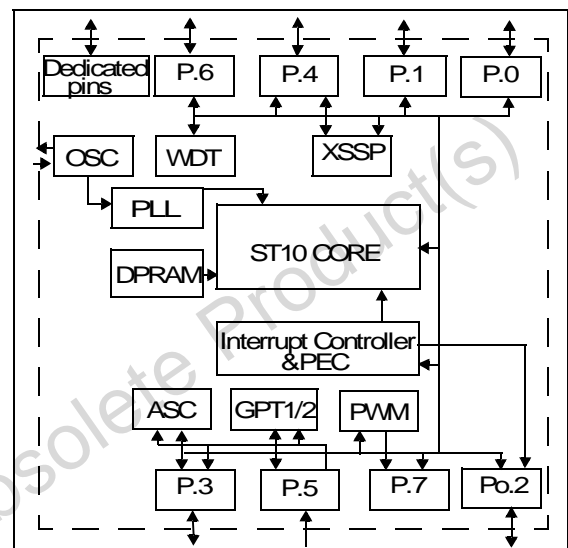
■ Fail Safe Protection

- Programmable watchdog timer
- Oscillator Watchdog

■ Interrupt

- 8-channel interrupt-driven single-cycle data transfer facilities via peripheral event controller (PEC)
- 16-priority-level interrupt system with 17 sources, sample-rate down to 40 ns

■ Timers



- Two multi-functional general purpose timer units with 5 timers
- Clock Generation via on-chip PLL, or via direct or prescaled clock input

■ Serial Channels

- Synchronous/asynchronous
- High-speed-synchronous serial port SSP

■ Up to 77 general purpose I/O lines

■ No bootstrap loader

■ Electrical Characteristics

- 5V Tolerant I/Os
- 5V Fail-Safe Inputs (Port 5)
- Power: 3.3 Volt +/-0.3V
- Idle and power down modes

■ Support

- C-compilers, macro-assembler packages, emulators, evaluation boards, HLL-debuggers, simulators, logic analyser disassemblers, programming boards

■ Package

- 100-Pin Thin Quad Flat Pack (TQFP)

Table of Contents

| | |
|---|-----------|
| 1 PIN DESCRIPTION | 4 |
| 2 FUNCTIONAL DESCRIPTION | 11 |
| 3 MEMORY MAPPING | 12 |
| 4 CENTRAL PROCESSING UNIT | 13 |
| 5 INTERRUPT AND TRAP FUNCTIONS | 14 |
| 5.1 INTERRUPT SOURCES | 15 |
| 5.2 HARDWARE TRAPS | 16 |
| 6 PARALLEL PORTS | 17 |
| 7 EXTERNAL BUS CONTROLLER | 17 |
| 8 PWM MODULE | 18 |
| 9 GENERAL PURPOSE TIMERS | 19 |
| 9.1 GPT1 | 19 |
| 9.2 GPT2 | 21 |
| 10 SERIAL CHANNELS | 22 |
| 11 WATCHDOG TIMER | 24 |
| 12 SYSTEM RESET | 25 |
| 13 POWER REDUCTION MODES | 26 |
| 14 SPECIAL FUNCTION REGISTERS | 26 |
| 15 ELECTRICAL CHARACTERISTICS | 31 |
| 15.1 ABSOLUTE MAXIMUM RATINGS | 31 |
| 15.2 DC CHARACTERISTICS | 33 |

Table of Contents

| | |
|--|-----------|
| 15.3 AC CHARACTERISTICS | 36 |
| 15.3.1 Cpu Clock Generation Mechanisms | 38 |
| 15.3.2 Memory Cycle Variables | 42 |
| 15.3.3 Multiplexed Bus | 43 |
| 15.3.4 Demultiplexed Bus | 50 |
| 15.3.5 CLKOUT and $\overline{\text{READY}}$ /READY | 57 |
| 15.3.6 External Bus Arbitration | 60 |
| 15.3.7 External Hardware Reset | 63 |
| 15.3.8 Synchronous Serial Port Timing | 66 |
| 16 PACKAGE MECHANICAL DATA | 68 |
| 17 ORDERING INFORMATION | 68 |

ST10R172L - PIN DESCRIPTION

1 PIN DESCRIPTION

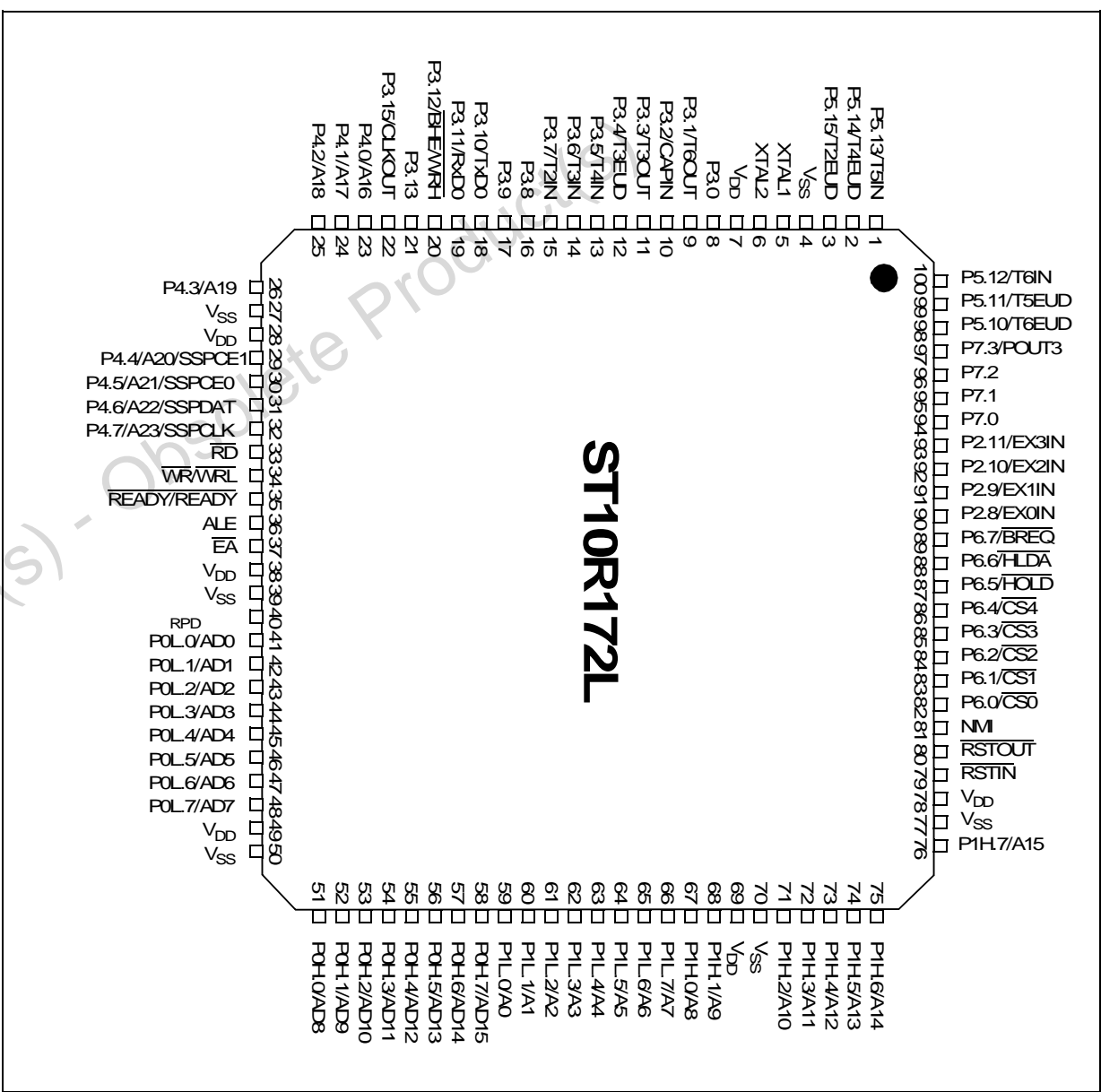


Figure 1 TQFP-100 pin configuration (top view)

| Symbol | Pin Number (TQFP) | Input (I) Output (O) | Kind ¹⁾ | Function |
|-----------------|--|---------------------------------|--|--|
| P5.10 –P5.15 | 98-100 1- 3 98 99 100 1 2 3 | I I I I I I I | 5S 5S 5S 5S 5S 5S 5S | 6-bit input-only port with Schmitt-Trigger characteristics. Port 5 pins also serve as timer inputs: P5.10 T6EUD GPT2 Timer T6 Ext.Up/Down Ctrl.Input P5.11 T5EUD GPT2 Timer T5 Ext.Up/Down Ctrl.Input P5.12 T6IN GPT2 Timer T6 Count Input P5.13 T5IN GPT2 Timer T5 Count Input P5.14 T4EUD GPT1 Timer T4 Ext.Up/Down Ctrl.Input P5.15 T2EUD GPT1 Timer T2 Ext.Up/Down Ctrl.Input |
| XTAL1 | 5 | I | 3T | XTAL1: Input to the oscillator amplifier and internal clock generator |
| XTAL2 | 6 | O | 3T | XTAL2: Output of the oscillator amplifier circuit. To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Observe minimum and maximum high/low and rise/fall times specified in the AC Characteristics. |

Table 1 Pin definitions

ST10R172L - PIN DESCRIPTION

| Symbol | Pin Number (TQFP) | Input (I) Output (O) | Kind ¹⁾ | Function |
|-----------------|----------------------|-------------------------|--------------------|--|
| P3.0 – P3.13 | 8-21 | I/O | 5T | A 15-bit (P3.14 is missing) bidirectional I/O port. Port 3 is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 3 outputs can be configured as push/pull or open drain drivers. The following pins have alternate functions: |
| P3.15 | 22 | I/O | 5T | |
| | | | | |
| | 9 | O | 5T | P3.1 T6OUT GPT2 Timer T6 toggle latch output |
| | 10 | I | 5T | P3.2 CAPIN GPT2 Register CAPREL capture input |
| | 11 | O | 5T | P3.3 T3OUT GPT1 Timer T3 toggle latch output |
| | 12 | I | 5T | P3.4 T3EUD GPT1 Timer T3 ext.up/down ctrl.input |
| | 13 | I | 5T | P3.5 T4IN GPT1 Timer T4 input for count/gate/reload/capture |
| | 14 | I | 5T | P3.6 T3IN GPT1 Timer T3 count/gate input |
| | 15 | I | 5T | P3.7 T2IN GPT1 Timer T2 input for count/gate/reload/capture |
| | 18 | O | 5T | P3.10 TxD0 ASC0 clock/data output (asyn./syn.) |
| | 19 | I/O | 5T | P3.11 RxD0 ASC0 data input (asyn.) or I/O (syn.) |
| | 20 | O | 5T | P3.12 $\overline{\text{BHE}}$ Ext. Memory High Byte Enable Signal |
| | | O | 5T | $\overline{\text{WRH}}$ Ext. Memory High Byte Write Strobe |
| | 22 | O | 5T | P3.15 CLKOUT System clock output (=CPU clock) |

Table 1 Pin definitions

| Symbol | Pin Number (TQFP) | Input (I) Output (O) | Kind ⁽¹⁾ | Function |
|---|----------------------|-------------------------|---------------------|--|
| P4.0– P4.7 | 23-26 29-32- | I/O | 5T | An 8-bit bidirectional I/O port. Port 8 is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 4 can be used to output the segment address lines for external bus configuration. |
| | 23 | O | 5T | P4.0 A16 Least Significant Segment Addr. Line |
| | ... | ... | ... | ... |
| | 26 | O | 5T | P4.3 A19 Segment Address Line |
| | 29 | O | 5T | P4.4 A20 Segment Address Line |
| | | O | 5T | SSPCE1 Chip Enable Line 1 |
| | 30 | O | 5T | P4.5 A21 Segment Address Line |
| | | O | 5T | SSPCE0 SSPChip Enable Line 0 |
| | 31 | O | 5T | P4.6 A22 Segment Address Line |
| | | I/O | 5T | SSPDAT SSP Data Input/Output Line |
| | 32 | O | 5T | P4.7 A23 Most Significant Segment Addr. Line |
| | | O | 5T | SSPCLK SSP Clock Output Line |
| $\overline{\text{RD}}$ | 33 | O | 5T | External Memory Read Strobe. RD is activated for every external instruction or data read access. |
| $\overline{\text{WR/}}$ $\overline{\text{WRL}}$ | 34 | O | 5T | External Memory Write Strobe. In WR-mode, this pin is activated for every external data write access. In WRL-mode, this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in the SYSCON register for mode selection. |
| $\overline{\text{READY/}}$ $\overline{\text{READY}}$ | 35 | I | 5T | Ready Input. Active level is programmable. When the Ready function is enabled, the selected inactive level at this pin during an external memory access will force the insertion of memory cycle time waitstates until the pin returns to the selected active level. Polarity is programmable. |

Table 1 Pin definitions

ST10R172L - PIN DESCRIPTION

| Symbol | Pin Number (TQFP) | Input (I) Output (O) | Kind ¹⁾ | Function | | | | | | | | | | | | | | | | | | |
|--|-------------------------------|-------------------------|--------------------|---|------------------|-------|--------|----------------|---------|---------|----------------|-----|----------|------------------|-------|--------|----------------|-----------|-----------|----------------|----------|------------|
| ALE | 36 | O | 5T | Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes. | | | | | | | | | | | | | | | | | | |
| \overline{EA} | 37 | I | 5T | External Access Enable pin. Low level at this pin during and after reset forces the ST10R172L to begin instruction execution out of external memory. A high level forces execution out of the internal ROM. The ST10R172L must have this pin tied to '0'. | | | | | | | | | | | | | | | | | | |
| PORT0: P0L.0– P0L.7, P0H.0 - P0H.7 | 41 - 48 51 - 58 | I/O | 5T | <p>PORT0 has two 8-bit bidirectional I/O ports P0L and P0H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state.</p> <p>For external bus configuration, PORT0 acts as address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes.</p> <p>Demultiplexed bus modes</p> <table><tr><td>Data Path Width:</td><td>8-bit</td><td>16-bit</td></tr><tr><td>P0L.0 – P0L.7:</td><td>D0 – D7</td><td>D0 - D7</td></tr><tr><td>P0H.0 – P0H.7:</td><td>I/O</td><td>D8 - D15</td></tr></table> <p>Multiplexed bus modes</p> <table><tr><td>Data Path Width:</td><td>8-bit</td><td>16-bit</td></tr><tr><td>P0L.0 – P0L.7:</td><td>AD0 – AD7</td><td>AD0 - AD7</td></tr><tr><td>P0H.0 – P0H.7:</td><td>A8 – A15</td><td>AD8 – AD15</td></tr></table> | Data Path Width: | 8-bit | 16-bit | P0L.0 – P0L.7: | D0 – D7 | D0 - D7 | P0H.0 – P0H.7: | I/O | D8 - D15 | Data Path Width: | 8-bit | 16-bit | P0L.0 – P0L.7: | AD0 – AD7 | AD0 - AD7 | P0H.0 – P0H.7: | A8 – A15 | AD8 – AD15 |
| Data Path Width: | 8-bit | 16-bit | | | | | | | | | | | | | | | | | | | | |
| P0L.0 – P0L.7: | D0 – D7 | D0 - D7 | | | | | | | | | | | | | | | | | | | | |
| P0H.0 – P0H.7: | I/O | D8 - D15 | | | | | | | | | | | | | | | | | | | | |
| Data Path Width: | 8-bit | 16-bit | | | | | | | | | | | | | | | | | | | | |
| P0L.0 – P0L.7: | AD0 – AD7 | AD0 - AD7 | | | | | | | | | | | | | | | | | | | | |
| P0H.0 – P0H.7: | A8 – A15 | AD8 – AD15 | | | | | | | | | | | | | | | | | | | | |
| PORT1: P1L.0– P1L.7, P1H.0 - P1H.7 | 59- 66 67, 68 71-76 | I/O | 5T | <p>PORT1 has two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. PORT1 acts as a 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode.</p> | | | | | | | | | | | | | | | | | | |

Table 1 Pin definitions

| Symbol | Pin Number (TQFP) | Input (I) Output (O) | Kind ¹⁾ | Function |
|----------------------------|----------------------|-------------------------|--------------------|--|
| $\overline{\text{RSTIN}}$ | 79 | I | 5T | Reset Input with Schmitt-Trigger characteristics. Resets the device when a low level is applied for a specified duration while the oscillator is running. An internal pullup resistor enables power-on reset using only a capacitor connected to V_{SS} . With a bonding option, the $\overline{\text{RSTIN}}$ pin can also be pulled-down for 512 internal clock cycles for hardware, software or watchdog timer triggered resets |
| $\overline{\text{RSTOUT}}$ | 80 | O | 5T | Internal Reset Indication Output. This pin is set to a low level when the part is executes hardware-, software- or watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed. |
| $\overline{\text{NMI}}$ | 81 | I | 5S | Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. If it is not used, $\overline{\text{NMI}}$ should be pulled high externally. |
| P6.0- P6.7 | 82-89 | I/O | 5T | An 8-bit bidirectional I/O port. Port 6 is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 6 outputs can be configured as push/pull or open drain drivers. The following Port 6 pins have alternate functions: |
| | 82 | O | 5T | P6.0 $\overline{\text{CS0}}$ Chip Select 0 Output |
| | ... | ... | ... | |
| | 86 | O | 5T | P6.4 $\overline{\text{CS4}}$ Chip Select 4 Output |
| | 87 | I | 5T | P6.5 $\overline{\text{HOLD}}$ External Master Hold Request Input (Master mode: O, Slave mode: I) |
| | 88 | I/O | 5T | P6.6 $\overline{\text{HLDA}}$ Hold Acknowledge Output |
| | 89 | O | 5T | P6.7 $\overline{\text{BREQ}}$ Bus Request Output |

Table 1 Pin definitions

ST10R172L - PIN DESCRIPTION

| Symbol | Pin Number (TQFP) | Input (I) Output (O) | Kind ¹⁾ | Function |
|-----------------|-----------------------------|-------------------------|--------------------|--|
| P2.8 – P2.11 | 90 - 93 | I/O | 5T | Port 2 is a 4-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 2 outputs can be configured as push/pull or open drain drivers. The following Port 2 pins have alternate functions: |
| | 90 | I | 5T | P2.8 EX0IN Fast External Interrupt 0 Input |
| | ... | ... | ... | |
| | 93 | I | 5T | P2.11 EX3IN Fast External Interrupt 3 Input |
| P7.0 – P7.3 | 94 - 97 | I/O | 5T | Port 7 is a 4-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 7 outputs can be configured as push/pull or open drain drivers. The following Port 7 pins have alternate functions: |
| | 97 | O | 5T | P7.3 POUT3 PWM (Channel 3) Output |
| RPD | 40 | I/O | 5T | Input timing pin for the return from powerdown circuit and power-up asynchronous reset. |
| V _{DD} | 7, 28, 38, 49, 69, 78 | - | PO | Digital supply voltage. |
| V _{SS} | 4, 27, 39, 50, 70, 77 | - | PO | Digital ground. |

Table 1 Pin definitions

- 1) The following I/O kinds are used. Refer to *ELECTRICAL CHARACTERISTICS* on page 31 for a detailed description.

PO: Power pin

3T: 3 V tolerant pin (voltage max. respect to V_{SS} is -0.5 to V_{DD} + 0.5)

5V: 5 V tolerant pin (voltage max. respect to V_{SS} is -0.5 to 5.5 only if chip is powered)

5S: 5 V tolerant and fail-safe pin (-0.5-5.5 max. voltage w.r.t. V_{SS} even if chip is not powered).

2 FUNCTIONAL DESCRIPTION

ST10R172L architecture combines the advantages of both RISC and CISC processors with an advanced peripheral subsystem. The following block diagram overviews the different on-chip components and the internal bus structure.

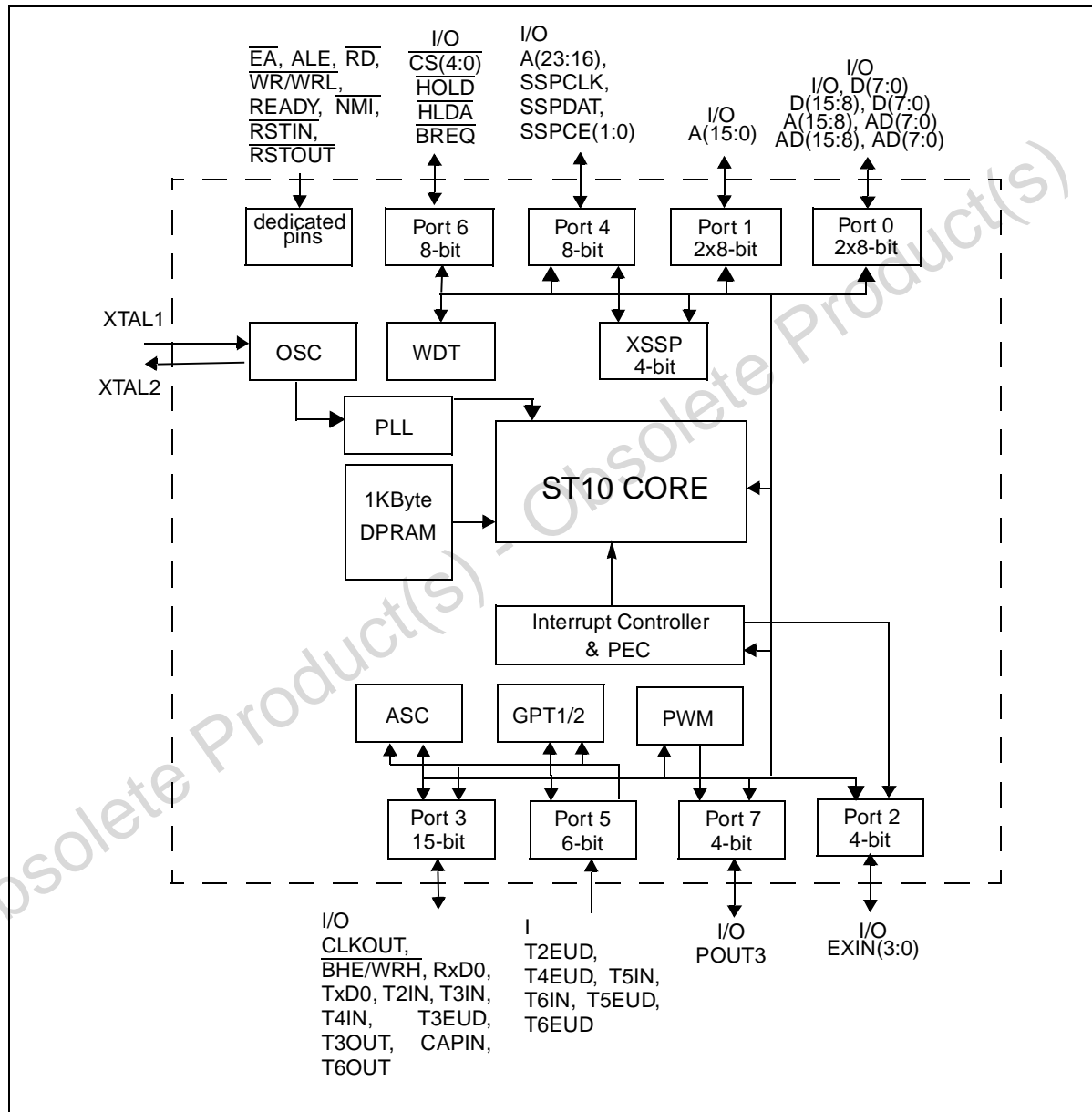


Figure 2 Block diagram

3 MEMORY MAPPING

The ST10R172L is a ROMless device, the internal RAM space is 1 KByte. The RAM address space is used for variables, register banks, the system stack, the PEC pointers (in 00'FCE0h - 00'FCFFh) and the bit-addressable space (in 00'FD00h - 00'FDFFh).

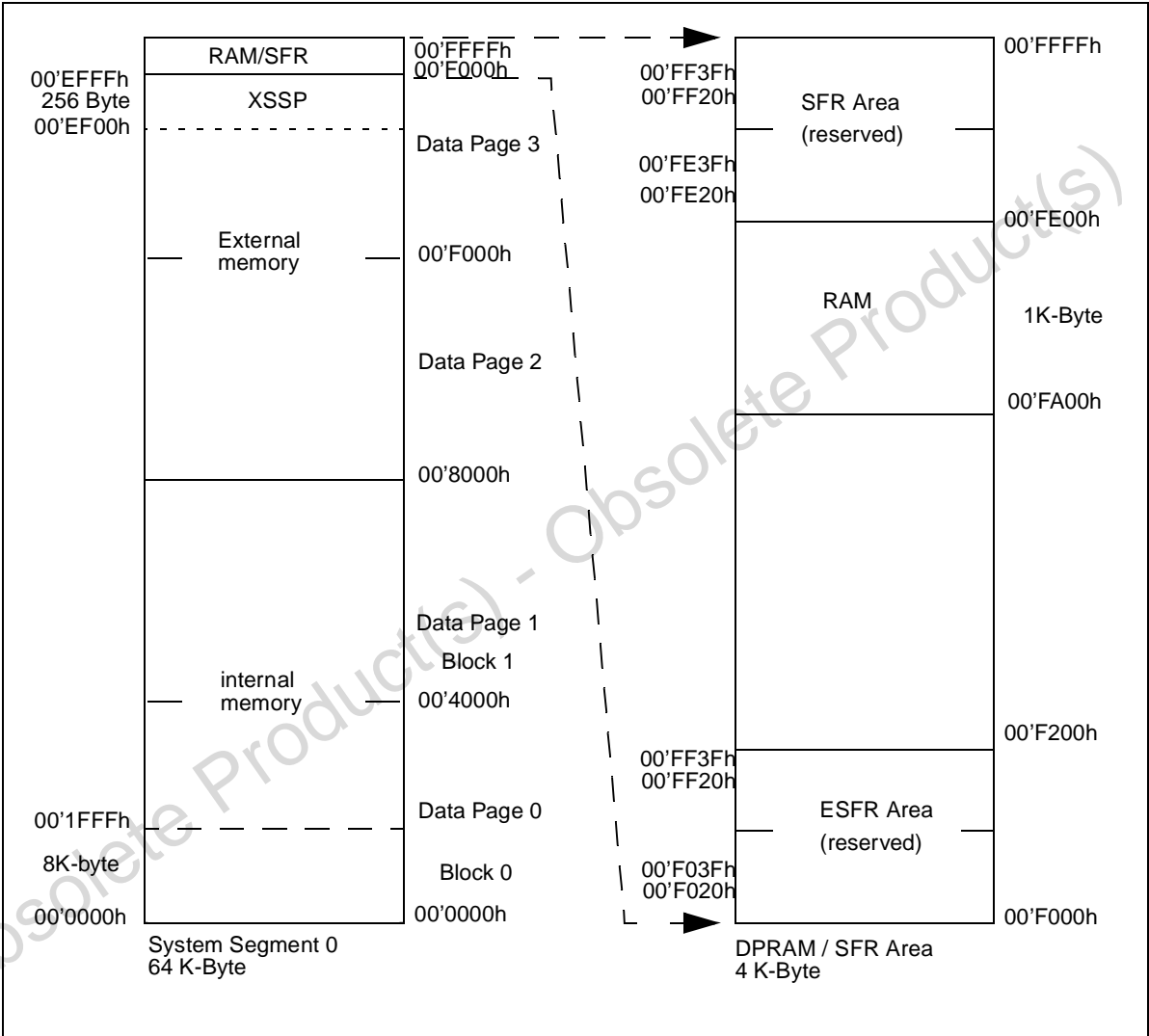


Figure 3 Memory map

4 CENTRAL PROCESSING UNIT

The main core of the CPU contains a 4-stage instruction pipeline, a separate multiply and divide unit, a bit-mask generator and a barrel shifter. Most instructions can be executed in one machine cycle requiring 40ns at 50MHz CPU clock.

The CPU includes an actual register context consisting of 16 wordwide GPRs physically located in the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, one register bank may overlap others.

A system stack of up to 1024 bytes is provided as a storage for temporary data. The system stack is allocated in the on-chip RAM area, and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are compared against the stack pointer value during each stack access to detect stack overflow or underflow.

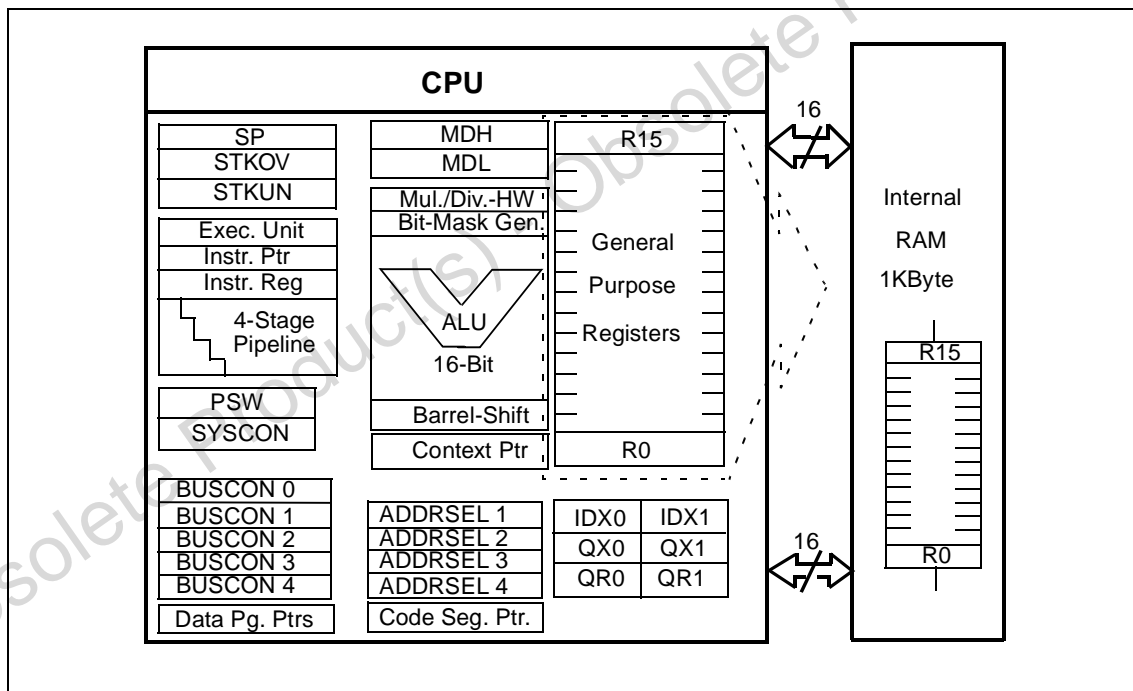


Figure 4 CPU block diagram

5 INTERRUPT AND TRAP FUNCTIONS

The architecture of the ST10R172L supports several mechanisms for fast and flexible response to the service requests that can be generated from various sources, internal or external to the microcontroller. Any of these interrupt requests can be programmed to be serviced, either by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In a standard interrupt service, program execution is suspended and a branch to the interrupt service routine is performed. For a PEC service, just one cycle is 'stolen' from the current CPU activity. A PEC service is a single, byte or word data transfer between any two memory locations, with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is decremented for each PEC service, except in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source-related vector location. PEC services are very well suited, for example, to the transmission or reception of blocks of data. The ST10R172L has 8 PEC channels, each of which offers fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield, exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher priority service request. For standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs, feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number.

5.1 Interrupt Sources

| Source of Interrupt or PEC Service Request | Request Flag | Enable Flag | Interrupt Vector | Vector Location | Trap Number |
|--|--------------|-------------|------------------|-----------------|-------------|
| External Interrupt 0 | CC8IR | CC8IE | CC8INT | 60h | 18h |
| External Interrupt 1 | CC9IR | CC9IE | CC9INT | 64h | 19h |
| External Interrupt 2 | CC10IR | CC10IE | CC10INT | 68h | 1Ah |
| External Interrupt 3 | CC11IR | CC11IE | CC11INT | 6Ch | 1Bh |
| GPT1 Timer 2 | T2IR | T2IE | T2INT | 88h | 22h |
| GPT1 Timer 3 | T3IR | T3IE | T3INT | 8Ch | 23h |
| GPT1 Timer 4 | T4IR | T4IE | T4INT | 90h | 24h |
| GPT2 Timer 5 | T5IR | T5IE | T5INT | 94h | 25h |
| GPT2 Timer 6 | T6IR | T6IE | T6INT | 98h | 26h |
| GPT2 CAPREL Register | CRIR | CRIE | CRINT | 9Ch | 27h |
| ASC0 Transmit | S0TIR | S0TIE | S0TINT | A8h | 2Ah |
| ASC0 Transmit Buffer | S0TBIR | S0TBIE | S0TBINT | 11Ch | 47h |
| ASC0 Receive | S0RIR | S0RIE | S0RINT | ACh | 2Bh |
| ASC0 Error | S0EIR | S0EIE | S0EINT | B0h | 2Ch |
| PWM Channel 3 | PWMIR | PWMIE | PWMINT | FCh | 3Fh |
| SSP Interrupt | XP1IR | XP1IE | XP1INT | 104h | 41h |
| PLL Unlock | XP3IR | XP3IE | XP3INT | 10Ch | 43h |

Table 2 List of possible interrupt sources, flags, vector and trap numbers

5.2 Hardware traps

Exceptions or error conditions that arise during run-time are called Hardware Traps. Hardware traps cause immediate non-maskable system reaction similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can not normally be interrupted by standard or PEC interrupts. The following table shows all of the possible exceptions or error conditions that can arise during run-time:

| Exception Condition | Trap Flag | Trap Vector | Vector Location | Trap Number | Trap Priority |
|-----------------------------|-----------|-------------|--|-----------------|----------------------|
| Reset Functions: | | | | | |
| Hardware Reset | | RESET | 00'0000h | 00h | III |
| Software Reset | | RESET | 00'0000h | 00h | III |
| Watchdog Timer Overflow | | RESET | 00'0000h | 00h | III |
| Class A Hardware Traps: | | | | | |
| Non-Maskable Interrupt | NMI | NMITRAP | 00'0008h | 02h | II |
| Stack Overflow | STKOF | STOTRAP | 00'0010h | 04h | II |
| Stack Underflow | STKUF | STUTRAP | 00'0018h | 06h | II |
| Class B Hardware Traps: | | | | | |
| Undefined opcode | UNDOPC | BTRAP | 00'0028h | 0Ah | I |
| Protected instruction fault | PRTFLT | BTRAP | 00'0028h | 0Ah | I |
| Illegal word operand access | ILLOPA | BTRAP | 00'0028h | 0Ah | I |
| Illegal instruction access | ILLINA | BTRAP | 00'0028h | 0Ah | I |
| Illegal external bus access | ILLBUS | BTRAP | 00'0028h | 0Ah | I |
| Reserved | | | [2Ch – 3Ch] | [0Bh – 0Fh] | |
| Software Traps | | | | | |
| TRAP Instruction | | | Any [00'0000h – 00'01FCh] steps of 4h | Any [00h – 7Fh] | Current CPU Priority |

Table 3 Exceptions or error conditions

6 PARALLEL PORTS

The ST10R172L provides up to 77 I/O lines organized into 7 input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs by direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of three I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation by control registers. During the internal reset, all port pins are configured as inputs.

All port lines have programmable alternate input or output functions associated with them. PORT0 and PORT1 may be used as address and data lines when accessing external memory, while Port 4 outputs the additional segment address bits A23/19/17...A16 in systems where segmentation is enabled to access more than 64 KBytes of memory. Port 6 provides optional bus arbitration signals (BREQ, HLDA, HOLD) and chip select signals. Port 3 includes alternate functions of timers, serial interfaces, the optional bus control signal \overline{BHE} and the system clock output (CLKOUT). Port 5 is used for timer control signals. Port 2 lines can be used as fast external interrupt lines. Port 7 includes alternate function for the PWM signal. All port lines that are not used for these alternate functions may be used as general purpose I/O lines.

7 EXTERNAL BUS CONTROLLER

All external memory accesses are performed by the on-chip External Bus Controller which can be programmed either to single chip mode when no external memory is required, or to the following external memory access modes:

| | |
|----------------------------|------------------------------|
| 16-bit data, demultiplexed | 16-/18-/20-/24-bit addresses |
| 16-bit data, multiplexed | 16-/18-/20-/24-bit addresses |
| 8-bit data, multiplexed | 16-/18-/20-/24-bit addresses |
| 8-bit data, demultiplexed | 16-/18-/20-/24-bit addresses |

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/output on PORT0/POL, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output.

Memory cycle time, memory tri-state time, length of ALE and read write delay are programmable so that a wide range of different memory types and external peripherals can be used. Up to 4 independent address windows can be defined (via ADDRSELx / BUSCONx register pairs) to access different resources with different bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 etc. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0. Up to 5 external \overline{CS} signals (4 windows plus default) can be generated to reduce external glue logic. Access to very slow memories is supported by the READY function.

A $\overline{HOLD}/\overline{HLDA}$ protocol is available for bus arbitration so that external resources can be shared with other bus masters. In slave mode, the slave controller can be connected to another master controller without glue logic. For applications which require less than 16 MBytes

of external memory space, the address space can be restricted to 1 MByte, 256 KByte or to 64 KByte.

8 PWM MODULE

A 1-channel Pulse Width Modulation (PWM) Module operates on channel 3. The pulse width modulation module can generate up to four PWM output signals using edge-aligned or centre-aligned PWM. In addition, the PWM module can generate PWM burst signals and single shot outputs. The table below shows the PWM frequencies for different resolutions. The level of the output signals is selectable and the PWM module can generate interrupt requests.

| Mode 0 edge aligned | Resolution | 8-bit | 10-bit | 12-bit | 14-bit | 16-bit |
|----------------------------------|-------------------|--------------|---------------|---------------|---------------|---------------|
| CPU clock/1 | 20ns | 195.3 KHz | 48.83KHz | 12.21KHz | 3.052KHz | 762.9Hz |
| CPU clock/64 | 1.28ns | 3.052KHz | 762.9Hz | 190.7Hz | 47.68Hz | 11.92Hz |
| Mode 1 center aligned | Resolution | 8-bit | 10-bit | 12-bit | 14-bit | 16-bit |
| CPU clock/1 | 20ns | 97.66KHz | 24.41KHz | 6.104KHz | 1.525KHz | 381.5Hz |
| CPU clock/64 | 1.28ns | 1.525Hz | 381.5 Hz | 95.37Hz | 23.84Hz | 0Hz |

Table 4 PWM unit frequencies and resolution at 50MHz CPU clock

9 GENERAL PURPOSE TIMERS

The GPTs are flexible multifunctional timer/counters used for time-related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation or pulse multiplication. The GPT unit contains five 16-bit timers, organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

9.1 GPT1

Each of the three timers T2, T3, T4 of the GPT1 module can be configured individually for one of four basic modes of operation: **timer, gated timer, counter mode and incremental interface mode**. In timer mode, the input clock for a timer is derived from the CPU clock, divided by a programmable prescaler. In counter mode, the timer is clocked in reference to external events. Pulse width or duty cycle measurement is supported in gated timer mode where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. Table 5 GPT1 timer input frequencies, resolution and periods lists the timer input frequencies, resolution and periods for each pre-scaler option at 50MHz CPU clock. This also applies to the Gated Timer Mode of T3 and to the auxiliary timers T2 and T4 in Timer and Gated Timer Mode

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD).

In Incremental Interface Mode, the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B by their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals so that the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has output toggle latches (TxOTL) which changes state on each timer over-flow/underflow. The state of this latch may be output on port pins (TxOUT) e. g. for time out monitoring of external hardware components, or may be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

| $F_{CPU}=50\text{MHz}$ | Timer input selection | | | | | | | |
|------------------------|-----------------------|-----------|------------|--------------------|--------------------|--------------------|---------------------|---------------------|
| | 000b | 001b | 010b | 011b | 100b | 101b | 110b | 111b |
| Prescaler Factor | 8 | 16 | 32 | 64 | 128 | 256 | 512 | 1024 |
| Input Frequency | 6.25 MHz | 3.125 MHz | 1.5625 MHz | 781 KHz | 391 KHz | 195 KHz | 97.5 KHz | 48.83 KHz |
| Resolution | 160ns | 320ns | 640ns | 1.28 μs | 2.56 μs | 5.12 μs | 10.24 μs | 20.48 μs |
| Period | 10.49ms | 20.97ms | 41.94ms | 83.88ms | 168ms | 336ms | 672ms | 1.342s |

Table 5 GPT1 timer input frequencies, resolution and periods

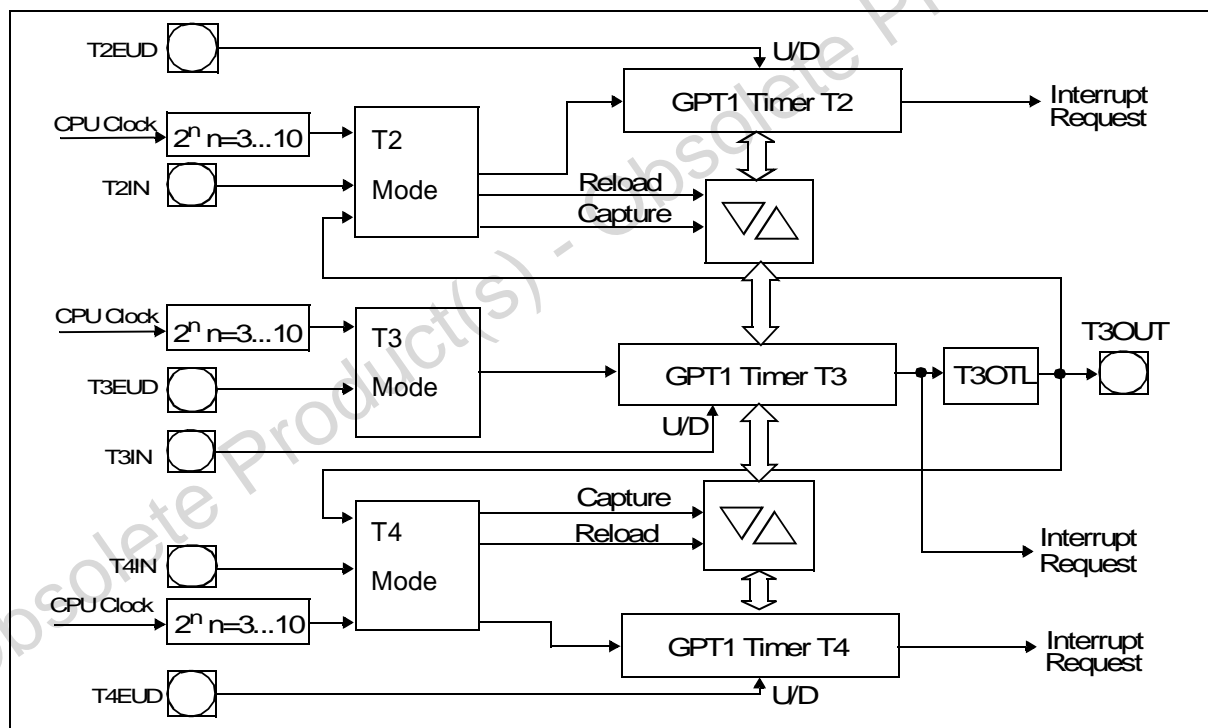


Figure 5 GPT1 block diagram

9.2 GPT2

The GPT2 module provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock derived from the CPU clock via a programmable prescaler or with external signals. The count direction (up/down) for each timer is programmable by software or altered dynamically by an external signal on a port pin (TxEUD). Concatenation of the timers is supported by the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of T6OTL may be used to clock timer T5, or may be output on a port pin T6OUT. The overflows/underflows of timer T6 reload the CAPREL register. The CAPREL register captures the contents of T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows absolute time differences to be measured or pulse multiplication to be performed without software overhead.

| F_{CPU}=50MHz | Timer input selection | | | | | | | |
|------------------------------|------------------------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| | 000b | 001b | 010b | 011b | 100b | 101b | 110b | 111b |
| Prescaler Factor | 4 | 8 | 16 | 32 | 64 | 128 | 256 | 512 |
| Input Frequency | 12.5 MHz | 6.25 MHz | 3.125 MHz | 1.563 MHz | 781 KHz | 391 KHz | 195 KHz | 97.6 KHz |
| Resolution | 80ns | 160ns | 320ns | 640ns | 1.28 us | 2.56 us | 5.12 us | 10.24 us |
| Period | 5.24ms | 10.49ms | 20.97ms | 41.94ms | 83.88ms | 167.7ms | 335.5ms | 671ms |

Table 6 GPT2 timer input frequencies, resolution and periods

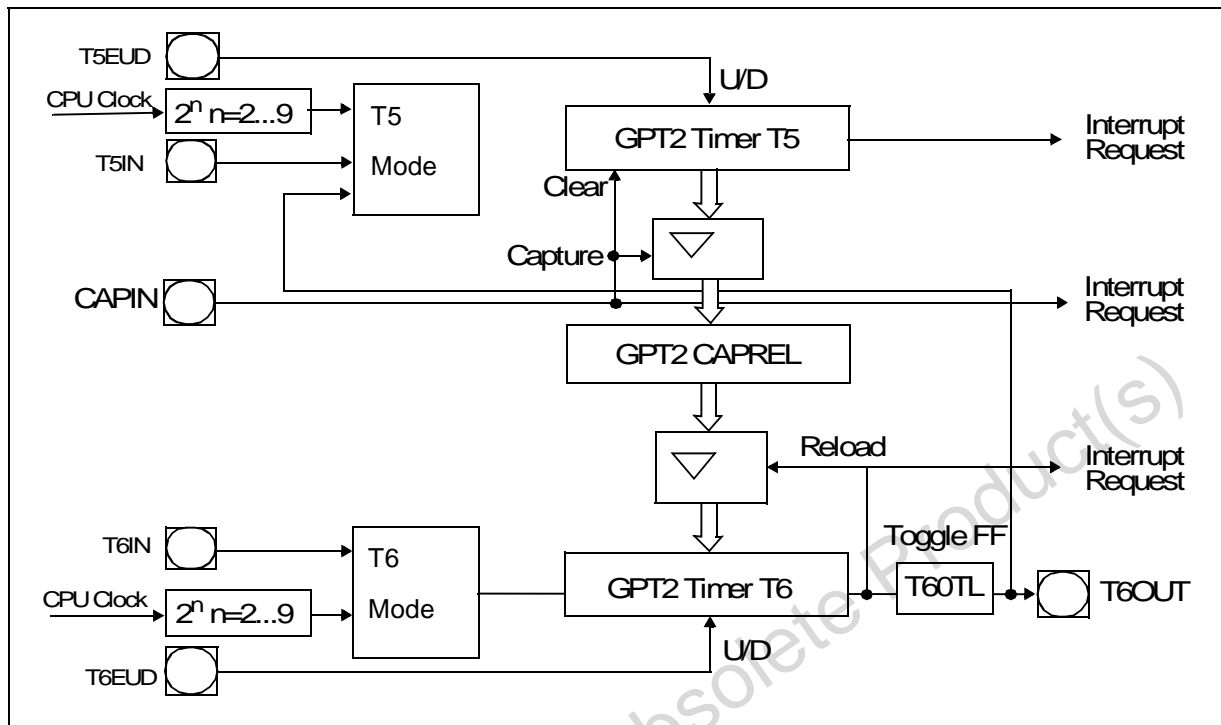


Figure 6 GPT2 block diagram

10 SERIAL CHANNELS

Serial communication with other microcontrollers, processors, terminals or external peripheral components is provided by two serial interfaces with different functionality, an Asynchronous/Synchronous Serial Channel (ASC0) and a Synchronous Serial Port (SSP).

ASC0

A dedicated baud rate generator sets up standard baud rates without oscillator tuning. 3 separate interrupt vectors are provided for transmission, reception, and erroneous reception. In asynchronous mode, 8- or 9-bit data frames are transmitted or received, preceded by a start bit and terminated by one or two stop bits. For multiprocessor communication, a mechanism to distinguish address from data bytes has been included (8-bit data + wake up bit mode).

In synchronous mode, the ASC0 transmits or receives bytes (8 bits) synchronously to a shift clock which is generated by the ASC0. The ASC0 always shifts the LSB first. A loop back option is available for testing purposes.

A number of optional hardware error detection capabilities have been included to increase the reliability of data transfers. A parity bit can be generated automatically on transmission, or checked on reception. Framing error detection recognizes data frames with missing stop bits. An overrun error is generated if the last character received was not read out of the receive buffer register at the time the reception of a new character is complete. The table below lists

various commonly used baud rates together with the required reload values and the deviation errors compared to the intended baudrate.

| S0BRS = '0', f _{CPU} = 50MHz | | | S0BRS = '1', f _{CPU} = 50MHz | | |
|---------------------------------------|-----------------|---------------------------------------|---------------------------------------|-----------------|---------------------------------------|
| Baud Rate (Baud) | Deviation Error | Reload Value | Baud Rate (Baud) | Deviation Error | Reload Value |
| 1562500 | 0.0% / 0.0% | 0000 _H / 0000 _H | 1041666 | 0.0% / 0.0% | 0000 _H / 0000 _H |
| 56000 | +3.3% / -0.4% | 001A _H / 001B _H | 56000 | +3.3% / -2.1% | 0011 _H / 0012 _H |
| 38400 | +1.7% / -0.8% | 0027 _H / 0028 _H | 38400 | +0.5% / -3.1% | 001A _H / 001B _H |
| 19200 | +0.5% / -0.8% | 0050 _H / 0051 _H | 19200 | +0.5% / -1.4% | 0035 _H / 0036 _H |
| 9600 | +0.5% / -0.1% | 00A1 _H / 00A2 _H | 9600 | +0.5% / -0.5% | 006B _H / 006C _H |
| 4800 | +0.2% / -0.1% | 0144 _H / 0145 _H | 4800 | 0.0% / -0.5% | 00D8 _H / 00D9 _H |
| 2400 | 0.0% / -0.1% | 028A _H / 028B _H | 2400 | 0.0% / -0.2% | 01B1 _H / 01B2 _H |
| 1200 | 0.0% / -0.1% | 0515 _H / 0516 _H | 1200 | 0.0% / -0.1% | 0363 _H / 0364 _H |
| 600 | 0.0% / 0.0% | 0A2B _H / 0A2C _H | 600 | 0.0% / -0.1% | 06C7 _H / 06C8 _H |
| 190 | +0.4% / +0.4% | 1FFF _H / 1FFF _H | 75 | 0.0% / 0.0% | 363F _H / 3640 _H |
| | | | 127 | +0.1% / +0.1% | 1FFF _H / 1FFF _H |

Table 7 Commonly used baud rates, required reload values and deviation errors

SSP transmits 1...3 bytes or receives 1 byte after sending 1...3 bytes synchronously to a shift clock which is generated by the SSP. The SSP can start shifting with the LSB or with the MSB and is used to select shifting and latching clock edges, and clock polarity. Up to two chip select lines may be activated in order to direct data transfers to one or both of two peripheral devices.

When the SSP is enabled, the four upper pins of Port4 can not be used as general purpose IO. Note that the segment address selection done via the system start-up configuration during reset has priority and overrides the SSP functions on these pins.

| SSPCKS Value | | Synchronous baud rate |
|--------------|------------------------------------|-----------------------|
| 000 | SSP clock = CPU clock divided by 2 | 25 MBit/s |
| 001 | SSP clock = CPU clock divided by 4 | 12.5 MBit/s |
| 010 | SSP clock = CPU clock divided by 8 | 6.25 MBit/s |

Table 8 Synchronous baud rate and SSPCKS reload values

| SSPCKS Value | | Synchronous baud rate |
|--------------|--------------------------------------|-----------------------|
| 011 | SSP clock = CPU clock divided by 16 | 3.13 MBit/s |
| 100 | SSP clock = CPU clock divided by 32 | 1.56 MBit/s |
| 101 | SSP clock = CPU clock divided by 64 | 781 KBit/s |
| 110 | SSP clock = CPU clock divided by 128 | 391 KBit/s |
| 111 | SSP clock = CPU clock divided by 256 | 195 KBit/s |

Table 8 Synchronous baud rate and SSPCKS reload values

11 WATCHDOG TIMER

The Watchdog Timer is a fail-safe mechanism which limits the malfunction time of the controller. The Watchdog Timer is always enabled after device reset and can only be disabled in the time interval until the EINIT (end of initialization) instruction has been executed. In this way, the chip's start-up procedure is always monitored. The software must be designed to service the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to maintain the Watchdog Timer, it will overflow generating an internal hardware reset and pulling the $\overline{\text{RSTOUT}}$ pin low to reset external hardware components.

The Watchdog Timer is a 16-bit timer, clocked with the system clock divided either by 2 or by 128. The high byte of the Watchdog Timer register can be set to a pre-specified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded. The table below shows the watchdog time range which for a 50MHz CPU clock rounded to 3 significant figures.

| Reload value in WDTREL | Prescaler for f_{CPU} | |
|---------------------------|--------------------------------|-------------------|
| | 2 (WDTIN = '0') | 128 (WDTIN = '1') |
| FF _H | 10.24 μs | 655 μs |
| 00 _H | 2.62 ms | 168 ms |

Table 9 Watchdog timer range

12 SYSTEM RESET

The following type of reset are implemented on the ST10R172L:

Asynchronous hardware reset: Asynchronous reset does not require a stabilized clock signal on XTAL1 as it is not internally resynchronized, it resets the microcontroller into its default reset state. Asynchronous reset is required on chip power-up and can be used during catastrophic situations. The rising edge of the RSTIN pin is internally resynchronized before exiting the reset condition, therefore, only the entry to hardware reset is asynchronous.

Synchronous hardware reset (warm reset): A warm synchronous hardware reset is triggered when the reset input signal $\overline{\text{RSTIN}}$ is latched low and Vpp pin is high. The I/Os are immediately (asynchronously) set in high impedance, $\overline{\text{RSTOUT}}$ is driven low. After $\overline{\text{RSTIN}}$ negation is detected, a short transition period elapses, during which pending internal hold states are cancelled and any current internal access cycles are completed, external bus cycles are aborted. Then, the internal reset sequence is active for 1024 TCL (512 CPU clock cycles). During this reset sequence, if bit BDRSTEN was previously set by software (bit 3 in SYSCON register), $\overline{\text{RSTIN}}$ pin is driven low and internal reset signal is asserted to reset the microcontroller in its default state. Note that after all reset sequence, bit BDRSTEN is cleared. After the reset sequence has been completed, the $\overline{\text{RSTIN}}$ input is sampled. When the reset input signal is active at that time the internal reset condition is prolonged until $\overline{\text{RSTIN}}$ becomes inactive.

Software reset: The reset sequence can be triggered at any time by the protected instruction SRST (software reset). This instruction can be executed deliberately within a program, e.g. to leave bootstrap loader mode, or on a hardware trap that reveals a system failure. As for a synchronous hardware reset, if bit BDRSTEN was previously set by software (bit 3 in SYSCON register), the reset sequence lasts 1024 TCL (512 CPU clock cycles), and drives the $\overline{\text{RSTIN}}$ pin low.

Watchdog timer reset: When the watchdog timer is not disabled during the initialization or serviced regularly during program execution it will overflow and trigger the reset sequence. Unlike hardware and software resets, the watchdog reset completes a running external bus cycle if this bus cycle does not use $\overline{\text{READY}}$, or if $\overline{\text{READY}}$ is sampled active (low) after the programmed waitstates. When $\overline{\text{READY}}$ is sampled inactive (high) after the programmed waitstates the running external bus cycle is aborted. Then the internal reset sequence is started. The watchdog reset cannot occur while the ST10R172L is in bootstrap loader mode.

Bidirectional reset: The bidirectional reset is activated by setting bit BDRSTEN (bit 3 in SYSCON register). This reset makes the watchdog timer reset and software reset externally visible. It is active for the duration of an internal reset sequences caused by a watchdog timer reset and software reset. Therefore, the bidirectional reset transforms an internal watchdog timer reset or software reset into an external hardware reset with a minimum duration of 1024 TCL.

13 POWER REDUCTION MODES

Two different power reduction modes with different levels of power reduction can be entered under software control.

In **Idle mode** the CPU is stopped, while the peripherals continue their operation. Idle mode can be terminated by any reset or interrupt request.

In **Power Down mode** both the CPU and the peripherals are stopped. Power Down mode can now be configured by software in order to be terminated only by a hardware reset or by an external interrupt source on fast external interrupt pins.

All external bus actions are completed before Idle or Power Down mode is entered. However, Idle or Power Down mode is **not** entered if READY is enabled, but has not been activated (driven low for negative polarity, or driven high for positive polarity) during the last bus access.

14 SPECIAL FUNCTION REGISTERS

The following table lists all ST10R172L SFRs in alphabetical order. Bit-addressable SFRs are marked with the letter “b” in column “Name”. SFRs within the Extended SFR-Space (ESFRs) are marked with the letter “E” in column “Physical Address”.

An SFR can be specified by its individual mnemonic name. Depending on the selected addressing mode, an SFR can be accessed by its physical address (using the Data Page Pointers), or by its short 8-bit address (without using the Data Page Pointers).

| Name | Physical Address | 8-Bit Address | Description | Reset Value |
|-----------|------------------|---------------|----------------------------------|-------------|
| ADDRSEL1 | FE18h | 0Ch | Address Select Register 1 | 0000h |
| ADDRSEL2 | FE1Ah | 0Dh | Address Select Register 2 | 0000h |
| ADDRSEL3 | FE1Ch | 0Eh | Address Select Register 3 | 0000h |
| ADDRSEL4 | FE1Eh | 0Fh | Address Select Register 4 | 0000h |
| BUSCON0 b | FF0Ch | 86h | Bus Configuration Register 0 | 0XX0h |
| BUSCON1 b | FF14h | 8Ah | Bus Configuration Register 1 | 0000h |
| BUSCON2 b | FF16h | 8Bh | Bus Configuration Register 2 | 0000h |
| BUSCON3 b | FF18h | 8Ch | Bus Configuration Register 3 | 0000h |
| BUSCON4 b | FF1Ah | 8Dh | Bus Configuration Register 4 | 0000h |
| CAPREL | FE4Ah | 25h | GPT2 Capture/Reload Register | 0000h |
| CC8IC b | FF88h | C4h | EX0IN Interrupt Control Register | 0000h |

Table 10 Special functional registers

ST10R172L - SPECIAL FUNCTION REGISTERS

| Name | | Physical Address | 8-Bit Address | Description | Reset Value |
|---------|---|------------------|---------------|---|-------------|
| CC9IC | b | FF8Ah | C5h | EX1IN Interrupt Control Register | 0000h |
| CC10IC | b | FF8Ch | C6h | EX2IN Interrupt Control Register | 0000h |
| CC11IC | b | FF8Eh | C7h | EX3IN Interrupt Control Register | 0000h |
| CP | | FE10h | 08h | CPU Context Pointer Register | FC00h |
| CRIC | b | FF6Ah | B5h | GPT2 CAPREL Interrupt Control Register | 0000h |
| CSP | | FE08h | 04h | CPU Code Segment Pointer Register (read only) | 0000h |
| DP0L | b | F100h E | 80h | P0L Direction Control Register | 00h |
| DP0H | b | F102h E | 81h | P0h Direction Control Register | 00h |
| DP1L | b | F104h E | 82h | P1L Direction Control Register | 00h |
| DP1H | b | F106h E | 83h | P1h Direction Control Register | 00h |
| DP2 | b | FFC2h | E1h | Port 2 Direction Control Register | -0--h |
| DP3 | b | FFC6h | E3h | Port 3 Direction Control Register | 0000h |
| DP4 | b | FFCAh | E5h | Port 4 Direction Control Register | 00h |
| DP6 | b | FFCEh | E7h | Port 6 Direction Control Register | 00h |
| DP7 | b | FFD2h | E9h | Port 7 Direction Control Register | -0h |
| DPP0 | | FE00h | 00h | CPU Data Page Pointer 0 Register (10 bits) | 0000h |
| DPP1 | | FE02h | 01h | CPU Data Page Pointer 1 Register (10 bits) | 0001h |
| DPP2 | | FE04h | 02h | CPU Data Page Pointer 2 Register (10 bits) | 0002h |
| DPP3 | | FE06h | 03h | CPU Data Page Pointer 3 Register (10 bits) | 0003h |
| EBUSCON | b | F10Eh E | 87H | Extended BUSCON register | 0000h |
| EXICON | b | F1C0h E | E0h | External Interrupt Control Register | 0000h |
| IDCHIP | | F07Ch E | 3Eh | Device Identifier Register | 1101h |
| IDMANUF | | F07Eh E | 3Fh | Manufacturer/Process Identifier Register | 0201h |
| IDMEM | | F07Ah E | 3Dh | On-chip Memory Identifier Register | 0000h |
| IDPROG | | F078h E | 3Ch | Programming Voltage Identifier Register | 0000h |
| MDC | b | FF0Eh | 87h | CPU Multiply Divide Control Register | 0000h |

Table 10 Special functional registers

ST10R172L - SPECIAL FUNCTION REGISTERS

| Name | | Physical Address | 8-Bit Address | Description | Reset Value |
|-------|---|------------------|---------------|--|-------------|
| MDH | | FE0Ch | 06h | CPU Multiply Divide Register – High Word | 0000h |
| MDL | | FE0Eh | 07h | CPU Multiply Divide Register – Low Word | 0000h |
| ODP2 | b | F1C2h E | E1h | Port 2 Open Drain Control Register | -0--h |
| ODP3 | b | F1C6h E | E3h | Port 3 Open Drain Control Register | 0000h |
| ODP6 | b | F1CEh E | E7h | Port 6 Open Drain Control Register | 00h |
| ODP7 | b | F1D2h E | E9h | Port 7 Open Drain Control Register | -0h |
| ONES | | FF1Eh | 8Fh | Constant Value 1's Register (read only) | FFFFh |
| P0L | b | FF00h | 80h | Port 0 Low Register (Lower half of PORT0) | 00h |
| P0H | b | FF02h | 81h | Port 0 High Register (Upper half of PORT0) | 00h |
| P1L | b | FF04h | 82h | Port 1 Low Register (Lower half of PORT1) | 00h |
| P1H | b | FF06h | 83h | Port 1 High Register (Upper half of PORT1) | 00h |
| P2 | b | FFC0h | E0h | Port 2 Register (4 bits) | -0--h |
| P3 | b | FFC4h | E2h | Port 3 Register | 0000h |
| P4 | b | FFC8h | E4h | Port 4 Register (8 bits) | 00h |
| P5 | b | FFA2h | D1h | Port 5 Register (read only) | XXXXh |
| P6 | b | FFCCh | E6h | Port 6 Register (8 bits) | 00h |
| P7 | b | FFD0h | E8h | Port 7 Register (4 bits) | -0h |
| PECC0 | | FEC0h | 60h | PEC Channel 0 Control Register | 0000h |
| PECC1 | | FEC2h | 61h | PEC Channel 1 Control Register | 0000h |
| PECC2 | | FEC4h | 62h | PEC Channel 2 Control Register | 0000h |
| PECC3 | | FEC6h | 63h | PEC Channel 3 Control Register | 0000h |
| PECC4 | | FEC8h | 64h | PEC Channel 4 Control Register | 0000h |
| PECC5 | | FECAh | 65h | PEC Channel 5 Control Register | 0000h |
| PECC6 | | FECCh | 66h | PEC Channel 6 Control Register | 0000h |
| PECC7 | | FECEh | 67h | PEC Channel 7 Control Register | 0000h |
| PP3 | | F03Eh E | 1Fh | PWM Module Period Register 3 | 0000h |

Table 10 Special functional registers

ST10R172L - SPECIAL FUNCTION REGISTERS

| Name | Physical Address | 8-Bit Address | Description | Reset Value |
|---------|------------------|---------------|--|---------------------|
| PSW | b FF10h | 88h | CPU Program Status Word | 0000h |
| PW3 | FE36h | 1Bh | PWM Module Pulse Width Register 3 | 0000h |
| PWMCON0 | b FF30h | 98h | PWM Module Control Register 0 | 0000h |
| PWMCON1 | b FF32h | 99h | PWM Module Control Register 1 | 0000h |
| PWMIC | b F17Eh E | BFh | PWM Module Interrupt Control Register | 0000h |
| RP0H | b F108h E | 84h | System Start-up Configuration Register (Rd. only) | XXh |
| S0BG | FEB4h | 5Ah | Serial Channel 0 baud rate generator reload reg | 0000h |
| S0CON | b FFB0h | D8h | Serial Channel 0 Control Register | 0000h |
| S0EIC | b FF70h | B8h | Serial Channel 0 Error Interrupt Control Register | 0000h |
| S0RBUF | FEB2h | 59h | Serial Channel 0 receive buffer reg. (rd only) | XXh |
| S0RIC | b FF6Eh | B7h | Serial Channel 0 Receive Interrupt Control Reg. | 0000h |
| S0TBIC | b F19Ch E | CEh | Serial Channel 0 transmit buffer interrupt control reg | 0000h |
| S0TBUF | FEB0h | 58h | Serial Channel 0 transmit buffer register (wr only) | 00h |
| S0TIC | b FF6Ch | B6h | Serial Channel 0 Transmit Interrupt Control Register | 0000h |
| SP | FE12h | 09h | CPU System Stack Pointer Register | FC00h |
| SSPCON0 | EF00h X | --- | SSP Control Register 0 | 0000h |
| SSPCON1 | EF02h X | --- | SSP Control Register 1 | 0000h |
| SSPRTB | EF04h X | --- | SSP Receive/Transmit Buffer | XXXXh |
| SSPTBH | EF06h X | --- | SSP Transmit Buffer High | XXXXh |
| STKOV | FE14h | 0Ah | CPU Stack Overflow Pointer Register | FA00h |
| STKUN | FE16h | 0Bh | CPU Stack Underflow Pointer Register | FC00h |
| SYSCON | b FF12h | 89h | CPU System Configuration Register | 0xx0h ¹⁾ |
| T2 | FE40h | 20h | GPT1 Timer 2 Register | 0000h |
| T2CON | b FF40h | A0h | GPT1 Timer 2 Control Register | 0000h |
| T2IC | b FF60h | B0h | GPT1 Timer 2 Interrupt Control Register | 0000h |

Table 10 Special functional registers

ST10R172L - SPECIAL FUNCTION REGISTERS

| Name | | Physical Address | 8-Bit Address | Description | Reset Value |
|-------|---|------------------|---------------|---|---------------------|
| T3 | | FE42h | 21h | GPT1 Timer 3 Register | 0000h |
| T3CON | b | FF42h | A1h | GPT1 Timer 3 Control Register | 0000h |
| T3IC | b | FF62h | B1h | GPT1 Timer 3 Interrupt Control Register | 0000h |
| T4 | | FE44h | 22h | GPT1 Timer 4 Register | 0000h |
| T4CON | b | FF44h | A2h | GPT1 Timer 4 Control Register | 0000h |
| T4IC | b | FF64h | B2h | GPT1 Timer 4 Interrupt Control Register | 0000h |
| T5 | | FE46h | 23h | GPT2 Timer 5 Register | 0000h |
| T5CON | b | FF46h | A3h | GPT2 Timer 5 Control Register | 0000h |
| T5IC | b | FF66h | B3h | GPT2 Timer 5 Interrupt Control Register | 0000h |
| T6 | | FE48h | 24h | GPT2 Timer 6 Register | 0000h |
| T6CON | b | FF48h | A4h | GPT2 Timer 6 Control Register | 0000h |
| T6IC | b | FF68h | B4h | GPT2 Timer 6 Interrupt Control Register | 0000h |
| TFR | b | FFACh | D6h | Trap Flag Register | 0000h |
| WDT | | FEAEh | 57h | Watchdog Timer Register (read only) | 0000h |
| WDTCN | | FFAEh | D7h | Watchdog Timer Control Register | 000xh ²⁾ |
| XP1IC | b | F18Eh E | C7h | SSP Interrupt Control Register | 0000h |
| XP3IC | b | F19Eh E | CFh | PLL unlock Interrupt Control Register | 0000h |
| ZEROS | b | FF1Ch | 8Eh | Constant Value 0's Register (read only) | 0000h |

Table 10 Special functional registers

Note 1. The system configuration is selected during reset.

Note 2. Bit WDTR indicates a watchdog timer triggered reset.

15 ELECTRICAL CHARACTERISTICS

15.1 Absolute Maximum Ratings

- Ambient temperature under bias (T_A): -40°C to +85 °C
- Storage temperature (T_{ST}): - 65 to +150 °C
- Voltage on V_{DD} pins with respect to ground (V_{SS}): - 0.5 to +4.0 V
- Voltage on any pin with respect to ground (V_{SS}): -0.5 to $V_{DD} + 0.5$ V
- Voltage on any 5V tolerant pin with respect to ground (V_{SS}): -0.5 to 5.5 V
- Voltage on any 5V fail-safe pin with respect to ground (V_{SS}): -0.5 to 5.5 V
- Input current on any pin during overload condition: -10 to +10 mA
- Absolute sum of all input currents during overload condition: |100 mA|
- Power dissipation: 1.0 W

Note Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on pins with respect to ground (V_{SS}) must not exceed the values defined by the Absolute Maximum Ratings.

The parameters listed in this section represent both the ST10R172L controller characteristics and the system requirements. To aid parameters interpretation in design evaluation, the a symbol column is marked:

CC for **C**ontroller **C**haracteristics: The ST10R172L logic provides signals with the respective timing characteristics.

SR for **S**ystem Requirement: The external system must provide signals with the respective timing characteristics to the ST10R172L.

Remarks on 5 volt tolerant (5T) and 5 volt fail-safe (5S) pins

The 5V tolerant input and output pins can sustain an absolute maximum external voltage of 5.5V.

However, signals on unterminated bus lines might have overshoot above 5.5V, presenting latchup and hot carrier risks. While these risks are under evaluation, observe the following security recommendations:

- Maximum peak voltage on 5V tolerant pin with respect to ground (V_{SS})= +6 V
- If the ringing of the external signal exceeds 6V, then clip the signal to the 5V supply.

Power supply failure condition

The power supply failure condition is a state where the chip is NOT supplied but is connected to active signal lines. There are several cases:

- 3.3V external lines on 3.3V (3T) pin on the non powered chip:NOT Acceptable
- 3.3V external lines on 5V tolerant (5T) pin on the non powered chip: Acceptable
The 5V tolerant buffer do not leak: external signals not altered. No reliability problem.
- 3.3V external lines on 5V fail-safe (5S) pin on the non powered chip: Acceptable
The 5V tolerant buffer do not leak: external signals not altered. No reliability problem.
- 5.5V external lines on 5V tolerant (5T) pin on the non powered chip: Acceptable
For VERY SHORT times only: the buffers do not leak (external signals not altered) but there is a fast degradation of the gate oxides in the buffers. The total maximum time under this stress condition is 2 days. This limits this configuration to short power-up/down sequences. For 10 year life time, the maximum duty factor is 1/1800 allowing e.g. a maximum stress duration of 48 seconds per day.
- 5.5V external lines on 5V fail-safe (5S) pin on the non powered chip: Acceptable
- 6V transient signals on 5V tolerant (5T) pin on the non powered chip: ...NOT Acceptable
- 6V transient signals on 5V fail-safe (5S) pin on the non powered chip:..... Acceptable

15.2 DC Characteristics

$$V_{DD} = 3.3V \pm 0.3V \quad V_{SS} = 0V$$

$$\text{Reset active} \quad T_A = -40^\circ\text{C to } +85^\circ\text{C}$$

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|---|--------------------------|--------------|--------------------------|--------------------------------|---|
| | | min. | max. | | |
| Input low voltage | V_{IL} SR | -0.3 | 0.8 | V | — |
| Input high voltage (all except \overline{RSTIN} and XTAL1) | V_{IH} SR | 2.0 | $V_{DD} + 0.3$ | V | — |
| Input high voltage \overline{RSTIN} , RPD | V_{IH1} SR | $0.6 V_{DD}$ | $V_{DD} + 0.3$ | V | — |
| Input high voltage XTAL1 | V_{IH2} SR | $0.7 V_{DD}$ | $V_{DD} + 0.3$ | V | — |
| Output low voltage (ALE, \overline{RD} , \overline{WR} , \overline{BHE} , CLKOUT, \overline{RSTIN} , \overline{RSTOUT} , CSX) | V_{OL} CC | — | 0.4 | V | $I_{OL} = 4\text{ mA}$ |
| Output low voltage (all other outputs) | V_{OL1} CC | — | 0.4 | V | $I_{OL1} = 2\text{ mA}$ |
| Output high voltage ALE, \overline{RD} , \overline{WR} , \overline{BHE} , CLKOUT, \overline{RSTIN} , \overline{RSTOUT} , CSX) | V_{OH} CC | 2.4 | — | V | $I_{OH} = -4\text{ mA}$ |
| Output high voltage ¹⁾ (all other outputs) | V_{OH1} CC | 2.4 | — | V | $I_{OH} = -2\text{ mA}$ |
| Input leakage current (3T pins) | I_{OZ} CC | — | ± 10 | μA | $0V < V_{IN} < V_{DD}$ |
| Input leakage current (5T, 5S pins) | I_{OZ1} CC | — | ± 10 $\pm 100^7)$ | μA μA | $0V < V_{IN} < V_{DD}$ $V_{DD} < V_{IN} < 5.0V^7)$ |
| \overline{RSTIN} pull-up resistor ²⁾ | R_{RST} CC | 20 | 300 | $k\Omega$ | $V_{IN} = 0V$ |
| Read/Write pullup current ³⁾ | I_{RWH} ⁴⁾ | — | -40 | μA | $V_{OUT} = 2.4V$ |
| Read/Write pullup current ³⁾ | I_{RWL} ⁵⁾ | -500 | — | μA | $V_{OUT} = 0.4V$ |
| ALE pulldown current ³⁾ | I_{ALEL} ⁴⁾ | 40 | — | μA | $V_{OUT} = 0.4V$ |
| ALE pulldown current ³⁾ | I_{ALEH} ⁵⁾ | — | 500 | μA | $V_{OUT} = 2.4V$ |
| Port 6 (\overline{CS}) pullup current ³⁾ | I_{P6H} ⁴⁾ | — | -40 | μA | $V_{OUT} = 2.4V$ |
| Port 6 (\overline{CS}) pullup current ³⁾ | I_{P6L} ⁵⁾ | -500 | — | μA | $V_{OUT} = 0.4V$ |

Table 11 DC characteristics

ST10R172L - ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|---|------------------------|--------------|----------------------|------|---|
| | | min. | max. | | |
| PORT0 configuration current ³ | I_{P0H} ⁴ | – | -4 | μA | $V_{IN} = V_{IHmin}$ |
| | I_{P0L} ⁵ | -50 | – | μA | $V_{IN} = V_{ILmax}$ |
| RPD pulldown current ² | I_{RPD} ⁵ | 100 | 500 | μA | $V_{OUT} = V_{DD}$ |
| XTAL1 input current | I_{IL} CC | – | ±20 | μA | $0\text{ V} < V_{IN} < V_{DD}$ |
| Pin capacitance ⁶⁾ (digital inputs/outputs) | C_{IO} CC | – | 10 | pF | $f = 1\text{ MHz}$ $T_A = 25\text{ °C}$ |
| Power supply current | I_{CC} | – | $15 + 2.5 * f_{CPU}$ | mA | f_{CPU} in [MHz] ⁷⁾⁾ |
| Idle mode supply current | I_{ID} | – | $10 + 0.9 * f_{CPU}$ | mA | $\overline{RSTIN} = V_{IH1}$ f_{CPU} in [MHz] ⁷ |
| Power-down mode supply current | I_{PD} ⁸ | – | 200 | μA | $V_{DD} = 3.6\text{ V}$ ⁹ |

Table 11 DC characteristics

- 1) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the resulting voltage comes from the external circuitry.
- 2) This specification is only valid during reset, or interruptible power-down mode, after reception of an external interrupt signal that will wake up the CPU.
- 3) This specification is only valid during reset, hold or adapt-mode. Port 6 pins are only affected if they are used for \overline{CS} output and the open drain function is not enabled.
- 4) The maximum current may be drawn while the signal line remains inactive.
- 5) The minimum current must be drawn in order to drive the signal line active.
- 6) Not 100% tested, guaranteed by design characterization.
- 7) Supply current is a function of operating frequency as illustrated in Figure 7 on page 35. This parameter is tested at V_{DDmax} and 50 MHz CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH} with an infinite execution of NOP instruction fetched from external memory (16-bit demux bus mode, no waitstates, no memory tri-state waitstates, normal ALE).
- 8) Typical value at 25°C = 20μA.
- 9) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at $V_{DD} - 0.1\text{ V}$ to V_{DD} , $V_{REF} = 0\text{ V}$, all outputs (including pins configured as outputs) disconnected.

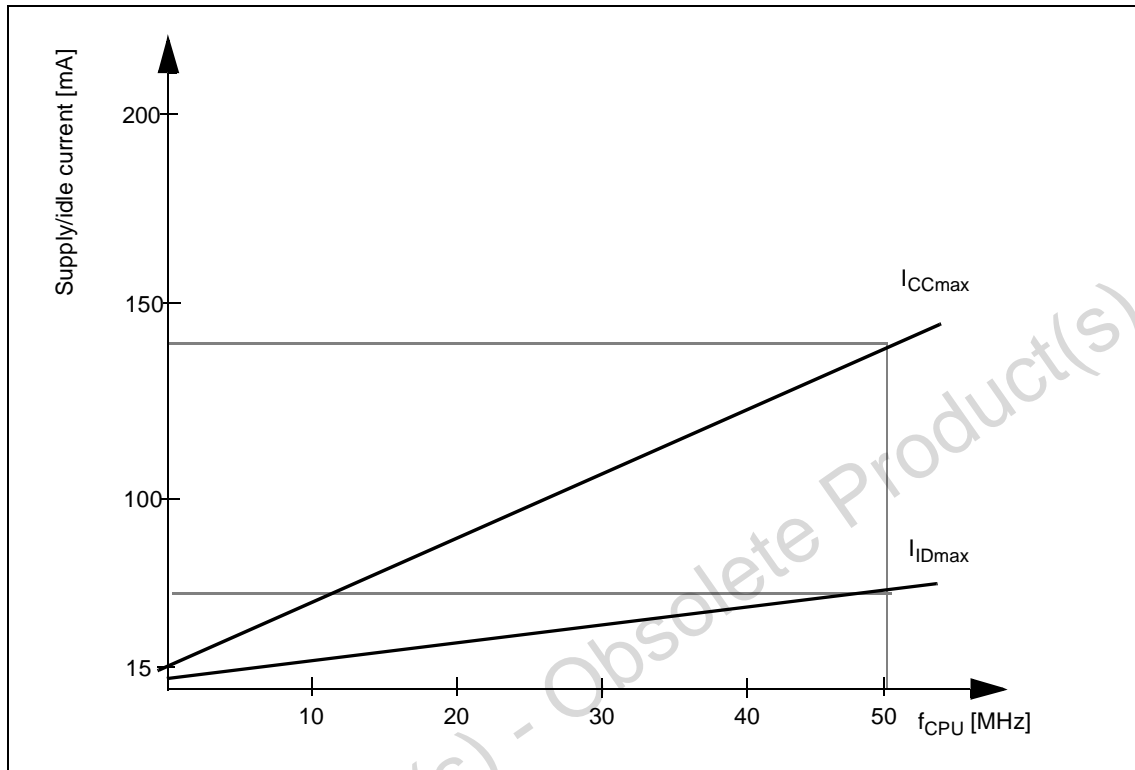


Figure 7 Supply/idle current vs operating frequency

15.3 AC Characteristics

Test conditions

- Input pulse levels: 0 to +3.0 V
- Input rise and fall times (10%-90%): 2.5 ns
- Input timing reference levels: +1.5 V
- Output timing reference levels: +1.5 V
- Output load: see Figure 9

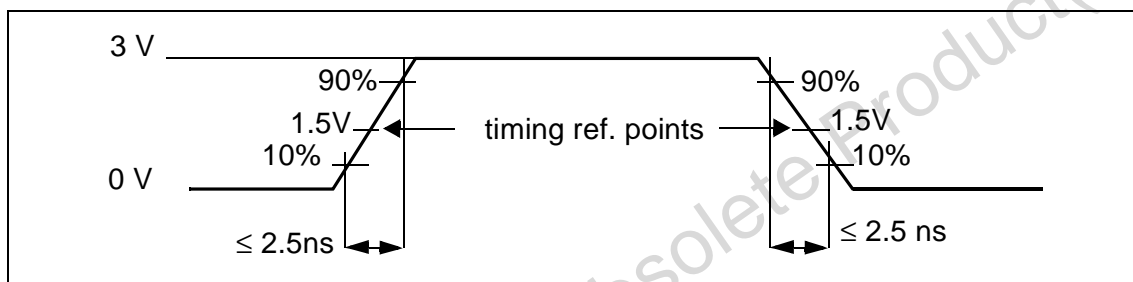


Figure 8 Input waveforms

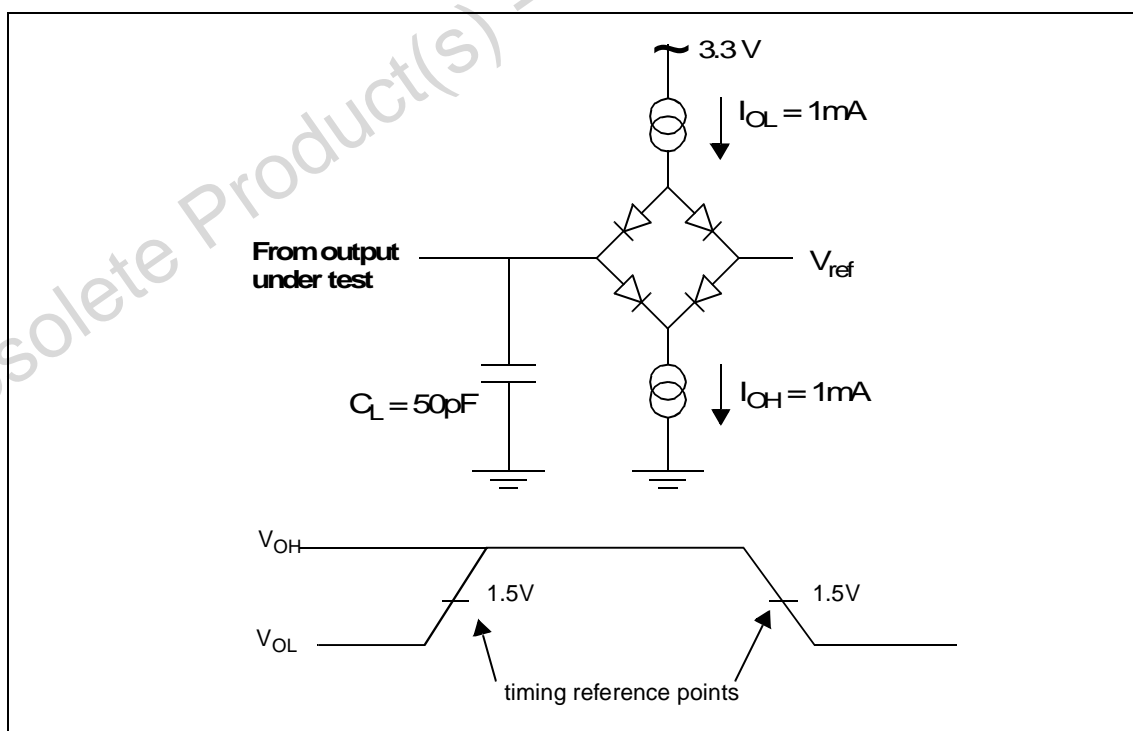


Figure 9 Output load circuit waveform

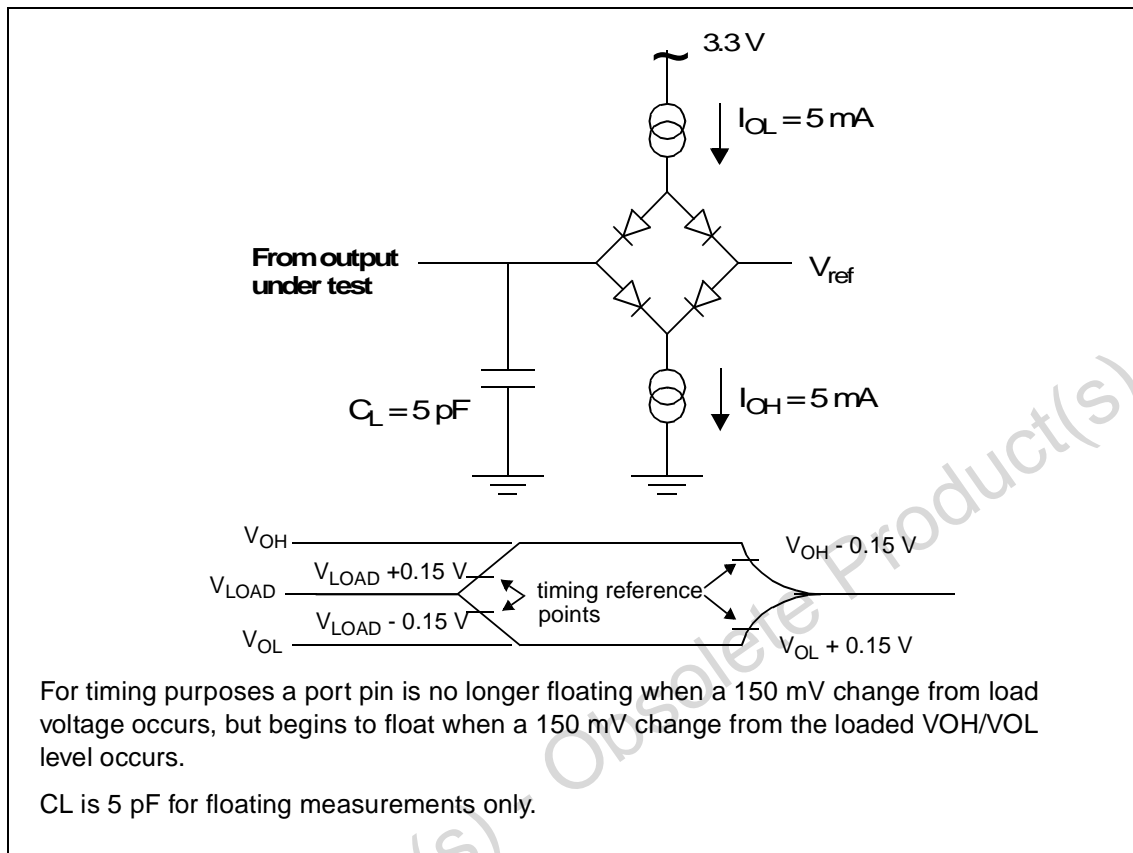


Figure 10 Float waveforms

15.3.1 Cpu Clock Generation Mechanisms

ST10R172L internal operation is controlled by the CPU clock f_{CPU} . Both edges of the CPU clock can trigger internal (e.g. pipeline) or external (e.g. bus cycles) operations. The external timing (AC Characteristics) specification therefore depends on the time between two consecutive edges of the CPU clock, called "TCL" (see figure below).

The CPU clock signal can be generated by different mechanisms. The duration of TCLs and their variation (and also the external timing) depends on the f_{CPU} generation mechanism. This must be considered when calculating ST10R172L timing.

The CPU clock generation mechanism is set during reset by the logic levels on pins P0.15-13 (P0H.7-5).

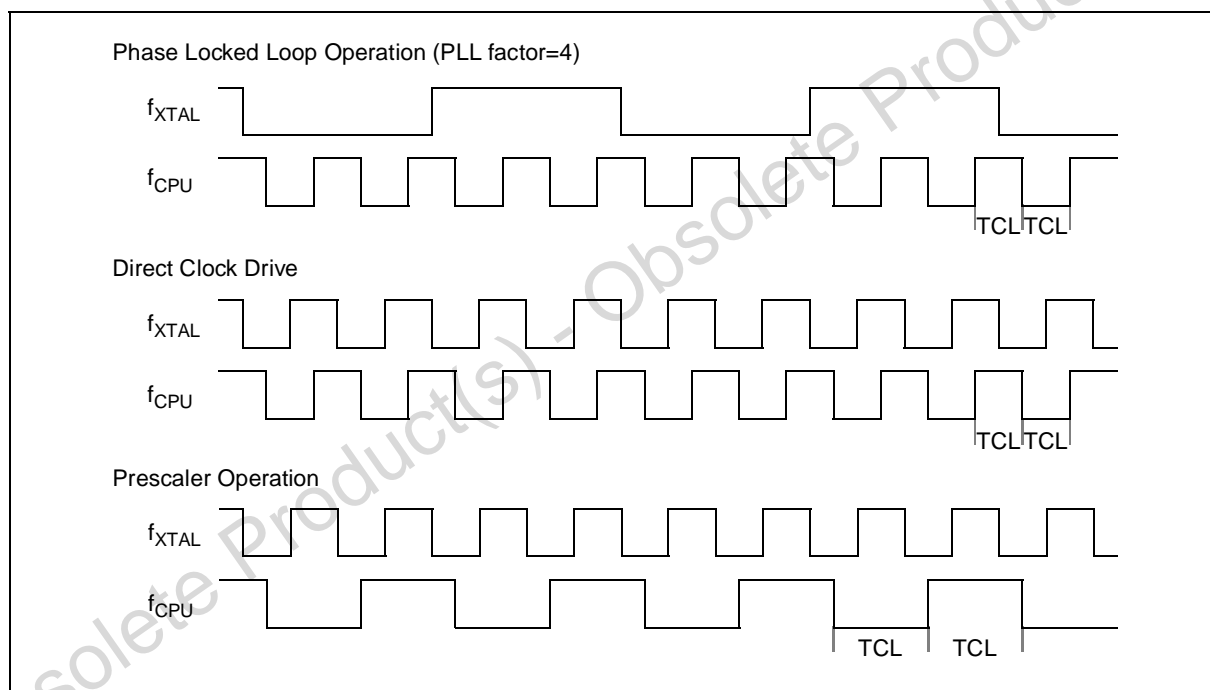


Figure 11 CPU clock generation mechanisms

| P0.15-13 (P0H.7-5) | CPU frequency $f_{CPU} = f_{XTAL} * F$ | External clock input range 10- 50MHz | Notes |
|--------------------|---|--|-----------------------|
| 1 1 1 | $F_{XTAL} * 4$ | 2.5 to 12.5 MHz | Default configuration |
| 1 1 0 | $F_{XTAL} * 3$ | 3.33 to 16.66 MHz | |
| 1 0 1 | $F_{XTAL} * 2$ | 5 to 25 MHz | |

Table 12 CPU clock generation mechanisms

| P0.15-13 (P0H.7-5) | | | CPU frequency $f_{CPU} = f_{XTAL} * F$ | External clock input range 10- 50MHz | Notes |
|--------------------|---|---|---|--|-----------------------------|
| 1 | 0 | 0 | $F_{XTAL} * 5$ | 2 to 10 MHz | |
| 0 | 1 | 1 | $F_{XTAL} * 1$ | 1 to 50 MHz | Direct drive ¹⁾ |
| 0 | 1 | 0 | $F_{XTAL} * 1.5$ | 6.66 to 33.33 MHz | |
| 0 | 0 | 1 | $F_{XTAL} / 2$ | 2 to 100 MHz | CPU clock via 2:1 prescaler |
| 0 | 0 | 0 | $F_{XTAL} * 2.5$ | 4 to 20 MHz | |

Table 12 CPU clock generation mechanisms

- 1) The maximum depends on the duty cycle of the external clock signal. The maximum input frequency is 25 MHz when using an external crystal oscillator, but higher frequencies can be applied with an external clock source.

Prescaler operation

Set when pins P0.15-13 (P0H.7-5) equal '001' during reset, the CPU clock is derived from the internal oscillator (input clock signal) by a 2:1 prescaler.

The frequency of f_{CPU} is half the frequency of f_{XTAL} and the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the period of the input clock f_{XTAL} .

The timings listed in the AC characteristics that refer to TCLs therefore can be calculated using the period of f_{XTAL} for any TCL.

Note that if the bit OWDDIS in SYSCON register is cleared, the PLL runs on its free-running frequency and delivers the clock signal for the Oscillator Watchdog. If bit OWDDIS is set, then the PLL is switched off.

Direct drive

When pins P0.15-13 (P0H.7-5) equal '011' during reset, the on-chip phase locked loop is disabled and the CPU clock is driven from the internal oscillator with the input clock signal. The frequency of f_{CPU} directly follows the frequency of f_{XTAL} so the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the duty cycle of the input clock f_{XTAL} .

The TCL timing below must be calculated using the minimum possible TCL which can be calculated by the formula: $TCL_{min} = 1/f_{XTAL} \times DC_{min}$ (DC = duty cycle)

For two consecutive TCLs the deviation caused by the duty cycle of f_{XTAL} is compensated so the duration of 2TCL is always $1/f_{XTAL}$. Therefore, the minimum value TCL_{min} has to be used only once for timings that require an odd number of TCLs (1,3,...). Timings that require an even number of TCLs (2,4,...) may use the formula: $2TCL = 1/f_{XTAL}$.

Note The address float timings in Multiplexed bus mode (t_{11} and t_{45}) use

$$TCL_{max} = 1/f_{XTAL} \times DC_{max} \text{ instead of } TCL_{min}.$$

Note that if the bit OWDDIS in SYSCON register is cleared, the PLL runs on its free-running frequency and delivers the clock signal for the Oscillator Watchdog. If bit OWDDIS is set, then the PLL is switched off.

Oscillator Watchdog (OWD)

When the clock option selected is direct drive or direct drive with prescaler, in order to provide a fail safe mechanism in case of a loss of the external clock, an oscillator watchdog is implemented as an additional functionality of the PLL circuitry. This oscillator watchdog operates as follows:

After a reset, the Oscillator Watchdog is enabled by default. To disable the OWD, set bit 4 of SYSCON register OWDDIS.

When the OWD is enabled, the PLL runs on its free-running frequency and increments the Oscillator Watchdog counter. On each transition of the XTAL1 pin, the Oscillator Watchdog is cleared. If an external clock failure occurs, then the Oscillator Watchdog counter overflows (after 16 PLL clock cycles). The CPU clock signal will be switched to the PLL free-running clock signal, and the Oscillator Watchdog Interrupt Request (XP3INT) is flagged. The CPU clock will not switch back to the external clock even if a valid external clock exists on XTAL1 pin. Only a hardware reset can switch the CPU clock source back to direct clock input.

When the OWD is disabled, the CPU clock is always fed from the oscillator input and the PLL is switched off to decrease power supply current.

Phase locked loop

For all other combinations of pins P0.15-13 (P0H.7-5) during reset the on-chip phase locked loop is enabled and provides the CPU clock. The PLL multiplies the input frequency by the factor F which is selected via the combination of pins P0.15-13 (i.e. $f_{CPU} = f_{XTAL} \times F$). With every F'th transition of f_{XTAL} the PLL circuit synchronizes the CPU clock to the input clock. In this way, f_{CPU} is constantly adjusted so it is locked to f_{XTAL} . The slight variation causes a jitter of f_{CPU} which affects individual TCL duration. Therefore, AC characteristics that refer to TCLs must be calculated using the minimum possible TCL.

The actual minimum value for TCL depends on the jitter of the PLL. As the PLL constantly adjusts its output frequency, it corresponds to the applied input frequency (crystal or oscillator). The relative deviation for periods of more than one TCL is lower than for one single TCL. For a period of $N \times$ TCL the minimum value is computed using the corresponding deviation D_N :

$$TCL_{min} = TCL_{NOM} \times (1 - |D_N|/100)$$
$$D_N = \pm(4 - N/15)[\%]$$

where N = number of consecutive TCLs and $1 \leq N \leq 40$. So for a period of 3 TCLs (i.e. $N = 3$):

$$\begin{aligned} D_3 &= 4 - 3/15 \\ &= 3,8\% \end{aligned}$$

and

$$\begin{aligned} 3TCL_{min} &= 3TCL_{NOM} \times (1 - 3,8/100) \\ &= 3TCL_{NOM} \times 0,962 (36.07\text{nsec @ } f_{cpu}=50\text{MHz}) \end{aligned}$$

PLL jitter is an important factor for bus cycles using waitstates and for the operation of timers, serial interfaces, etc. For slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

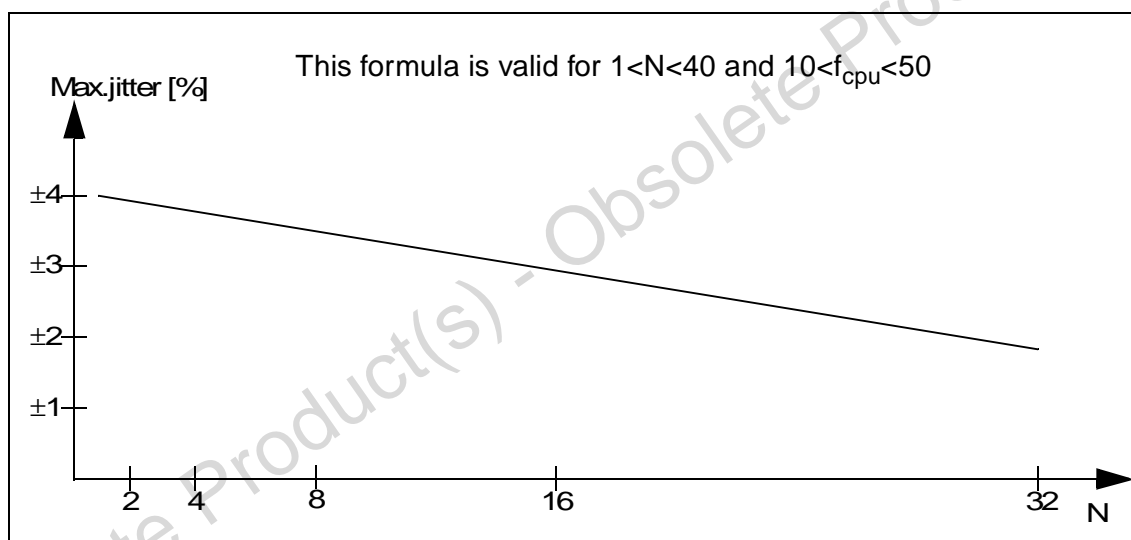


Figure 12 Approximated maximum PLL jitter

15.3.2 Memory Cycle Variables

The timing tables below use three variables derived from the BUSCONx registers and represent programmed memory cycle characteristics. Table 13 describes how these variables are computed.

| Description | Symbol | Values |
|------------------------------|--------|--------------------------------------|
| ALE Extension | t_A | $TCL * \langle ALECTL \rangle$ |
| Memory Cycle Time Waitstates | t_C | $2TCL * (15 - \langle MCTC \rangle)$ |
| Memory Tristate Time | t_F | $2TCL * (1 - \langle MTTC \rangle)$ |

Table 13 Memory cycle variables

15.3.3 Multiplexed Bus

$V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$ $V_{SS} = 0\text{ V}$ $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $C_L = 50\text{ pF}$

ALE cycle time = $6\text{ TCL} + 2t_A + t_C + t_F$ (60 ns at 50-MHz CPU clock without waitstates)

| Parameter | Symbol | | Max. CPU Clock = 50 MHz | | Variable CPU Clock 1/2TCL = 1 to 50 MHz | | Unit |
|--|----------|----|----------------------------|-------------------|--|---------------------------------|------|
| | | | min. | max. | min. | max. | |
| ALE high time | t_5 | CC | $7 + t_A$ | — | $\text{TCL} - 3 + t_A$ | — | ns |
| Address (P1, P4), $\overline{\text{BHE}}$ setup to ALE | t_6 | CC | $3 + t_A$ | — | $\text{TCL} - 7 + t_A$ | — | ns |
| Address (P0) setup to ALE | t_{6m} | CC | $5 + t_A$ | — | $\text{TCL} - 5 + t_A$ | — | ns |
| Address hold after ALE | t_7 | CC | $5 + t_A$ | — | $\text{TCL} - 5 + t_A$ | — | ns |
| ALE falling edge to $\overline{\text{RD}}$, $\overline{\text{WR}}$ (with RW-delay) | t_8 | CC | $5 + t_A$ | — | $\text{TCL} - 5 + t_A$ | — | ns |
| ALE falling edge to $\overline{\text{RD}}$, $\overline{\text{WR}}$ (no RW-delay) | t_9 | CC | $-5 + t_A$ | — | $-5 + t_A$ | — | ns |
| Address float after $\overline{\text{RD}}$, (with RW-delay) ¹⁾ | t_{10} | CC | — | 5^1 | — | 5^1 | ns |
| Address float after $\overline{\text{RD}}$, (no RW-delay) ¹⁾ | t_{11} | CC | — | 15^1 | — | $\text{TCL} + 5^1$ | ns |
| $\overline{\text{RD}}$, $\overline{\text{WR}}$ low time (with RW-delay) | t_{12} | CC | $13 + t_C$ | — | $2\text{TCL} - 7 + t_C$ | — | ns |
| $\overline{\text{RD}}$, $\overline{\text{WR}}$ low time (no RW-delay) | t_{13} | CC | $23 + t_C$ | — | $3\text{TCL} - 7 + t_C$ | — | ns |
| $\overline{\text{RD}}$ to valid data in (with RW-delay) | t_{14} | SR | — | $5 + t_C$ | — | $2\text{TCL} - 15 + t_C$ | ns |
| $\overline{\text{RD}}$ to valid data in (no RW-delay) | t_{15} | SR | — | $15 + t_C$ | — | $3\text{TCL} - 15 + t_C$ | ns |
| ALE low to valid data in | t_{16} | SR | — | $15 + t_A + t_C$ | — | $3\text{TCL} - 15 + t_A + t_C$ | ns |
| Address to valid data in | t_{17} | SR | — | $20 + 2t_A + t_C$ | — | $4\text{TCL} - 20 + 2t_A + t_C$ | ns |

Table 14 Multiplexed bus

ST10R172L - ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Max. CPU Clock = 50 MHz | | Variable CPU Clock 1/2TCL = 1 to 50 MHz | | Unit |
|---|---------------------|----------------------------|-------------------|--|--------------------------|------|
| | | min. | max. | min. | max. | |
| Data hold after \overline{RD} rising edge | t ₁₈ SR | 0 | — | 0 | — | ns |
| Data float after \overline{RD} rising edge ¹²⁾ | t ₁₉ SR | — | $15 + t_F^2$ | — | $2TCL - 5 + t_F^2$ | ns |
| Data valid to \overline{WR} | t ₂₂ CC | $13 + t_C$ | — | $2TCL - 7 + t_C$ | — | ns |
| Data hold after \overline{WR} | t ₂₃ CC | $13 + t_F$ | — | $2TCL - 7 + t_F$ | — | ns |
| ALE rising edge after \overline{RD} , \overline{WR} | t ₂₅ CC | $10 + t_F$ | — | $2TCL - 10 + t_F$ | — | ns |
| Address hold after \overline{RD} , \overline{WR} | t ₂₇ CC | $10 + t_F$ | — | $2TCL - 10 + t_F$ | — | ns |
| Latched \overline{CS} setup to ALE | t ₃₈ CC | $-7 + t_A$ | $3 + t_A$ | $-7 + t_A$ | $3 + t_A$ | ns |
| Unlatched \overline{CS} setup to ALE | t _{38u} CC | $3 + t_A$ | — | $TCL - 7 + t_A$ | — | ns |
| Latched \overline{CS} low to Valid Data In | t ₃₉ SR | — | $13 + t_C + 2t_A$ | — | $3TCL - 17 + t_C + 2t_A$ | ns |
| Unlatched \overline{CS} low to Valid Data In | t _{39u} SR | — | $23 + t_C + 2t_A$ | — | $4TCL - 17 + t_C + 2t_A$ | ns |
| Latched \overline{CS} hold after \overline{RD} , \overline{WR} | t ₄₀ CC | $20 + t_F$ | — | $3TCL - 10 + t_F$ | — | ns |
| Unlatched \overline{CS} hold after \overline{RD} , \overline{WR} | t _{40u} CC | $10 + t_F$ | — | $2TCL - 10 + t_F$ | — | ns |
| ALE fall. edge to \overline{RdCS} , \overline{WrCS} (with RW delay) | t ₄₂ CC | $7 + t_A$ | — | $TCL - 3 + t_A$ | — | ns |
| ALE fall. edge to \overline{RdCS} , \overline{WrCS} (no RW delay) | t ₄₃ CC | $-3 + t_A$ | — | $-3 + t_A$ | — | ns |
| Address float after \overline{RdCS} (with RW delay) ¹ | t ₄₄ CC | — | 3^1 | — | 3^1 | ns |
| Address float after \overline{RdCS} (no RW delay) ¹ | t ₄₅ CC | — | 13^1 | — | $TCL + 3^1$ | ns |

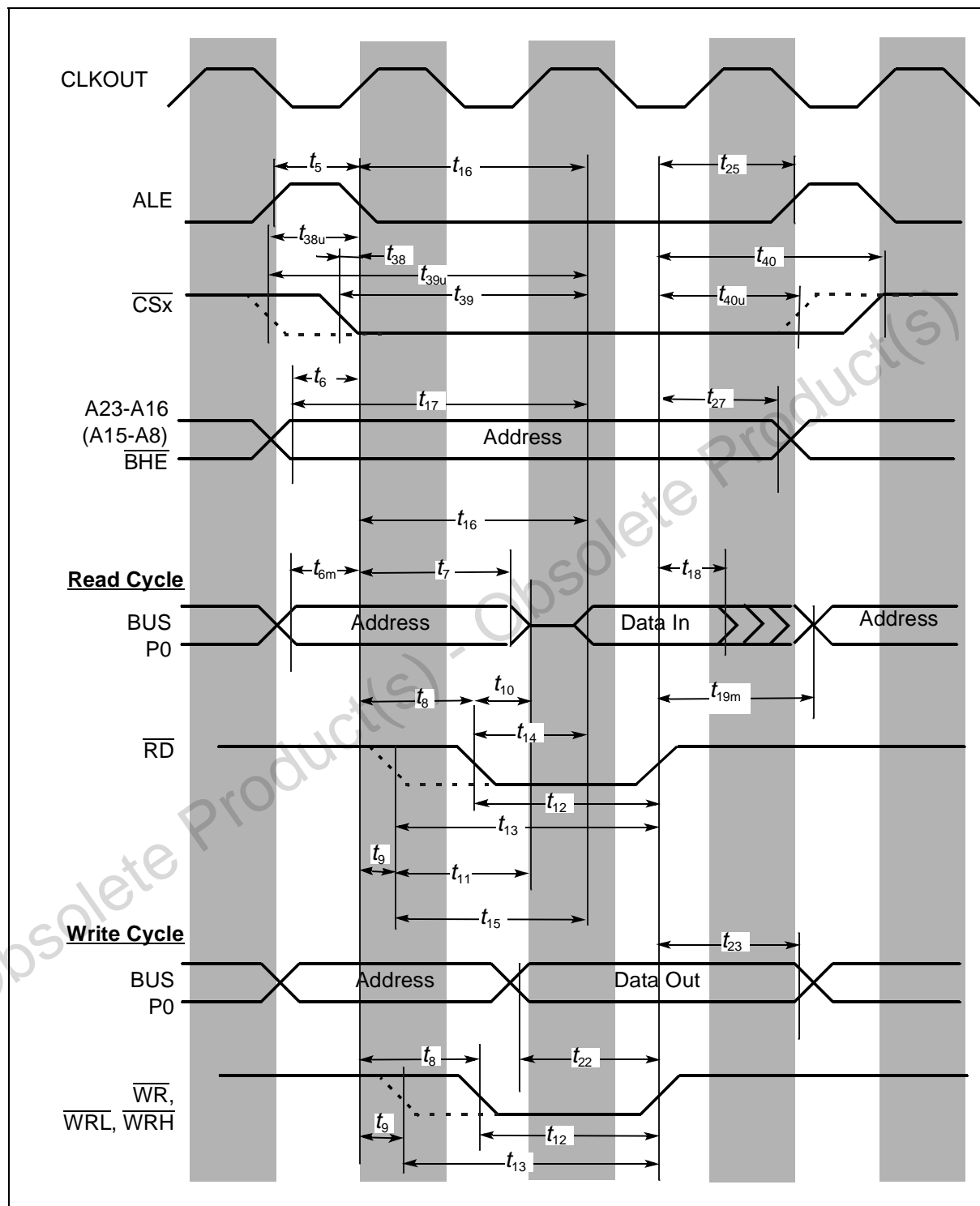
Table 14 Multiplexed bus

ST10R172L - ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Max. CPU Clock = 50 MHz | | Variable CPU Clock 1/2TCL = 1 to 50 MHz | | Unit |
|--|--------------------|----------------------------|----------------------------------|--|--|------|
| | | min. | max. | min. | max. | |
| RdCS to Valid Data In (with RW delay) | t ₄₆ SR | – | 3 + t _C | – | 2TCL - 17 + t _C | ns |
| RdCS to Valid Data In (no RW delay) | t ₄₇ SR | – | 13 + t _C | – | 3TCL - 17 + t _C | ns |
| RdCS, WrCS Low Time (with RW delay) | t ₄₈ CC | 13 + t _C | – | 2TCL - 7 + t _C | – | ns |
| RdCS, WrCS Low Time (no RW delay) | t ₄₉ CC | 23 + t _C | – | 3TCL - 7 + t _C | – | ns |
| Data valid to WrCS | t ₅₀ CC | 10 + t _C | – | 2TCL - 10 + t _C | – | ns |
| Data hold after RdCS | t ₅₁ SR | 0 | – | 0 | – | ns |
| Data float after RdCS ^{1 2} | t ₅₂ SR | – | 13 + t _F ² | – | 2TCL - 7 + t _F ² | ns |
| Address hold after RdCS, WrCS | t ₅₄ CC | 10 + t _F | – | 2TCL - 10 + t _F | – | ns |
| Data hold after WrCS | t ₅₆ CC | 10 + t _F | – | 2TCL - 10 + t _F | – | ns |

Table 14 Multiplexed bus

- 1) Output loading is specified using Figure 10 (CL = 5 pF).
- 2) This delay assumes that the following bus cycle is a multiplexed bus cycle. If next bus cycle is demultiplexed, refer to demultiplexed equivalent AC timing.



**Figure 13 External memory cycle:
multiplexed bus, with/without read/write delay, normal ALE**

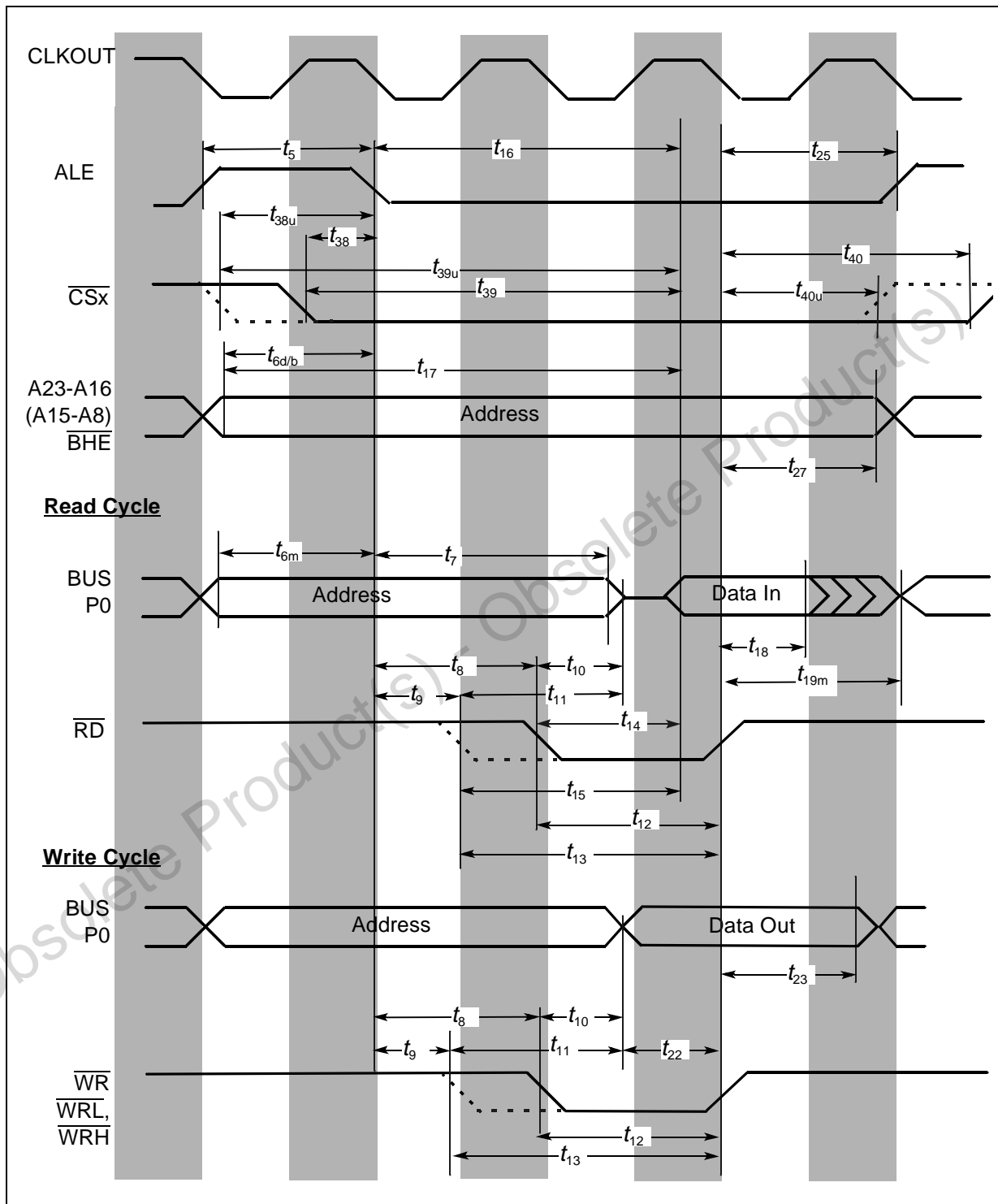


Figure 14 External memory cycle:
multiplexed bus, with/without read/write delay, extended ALE

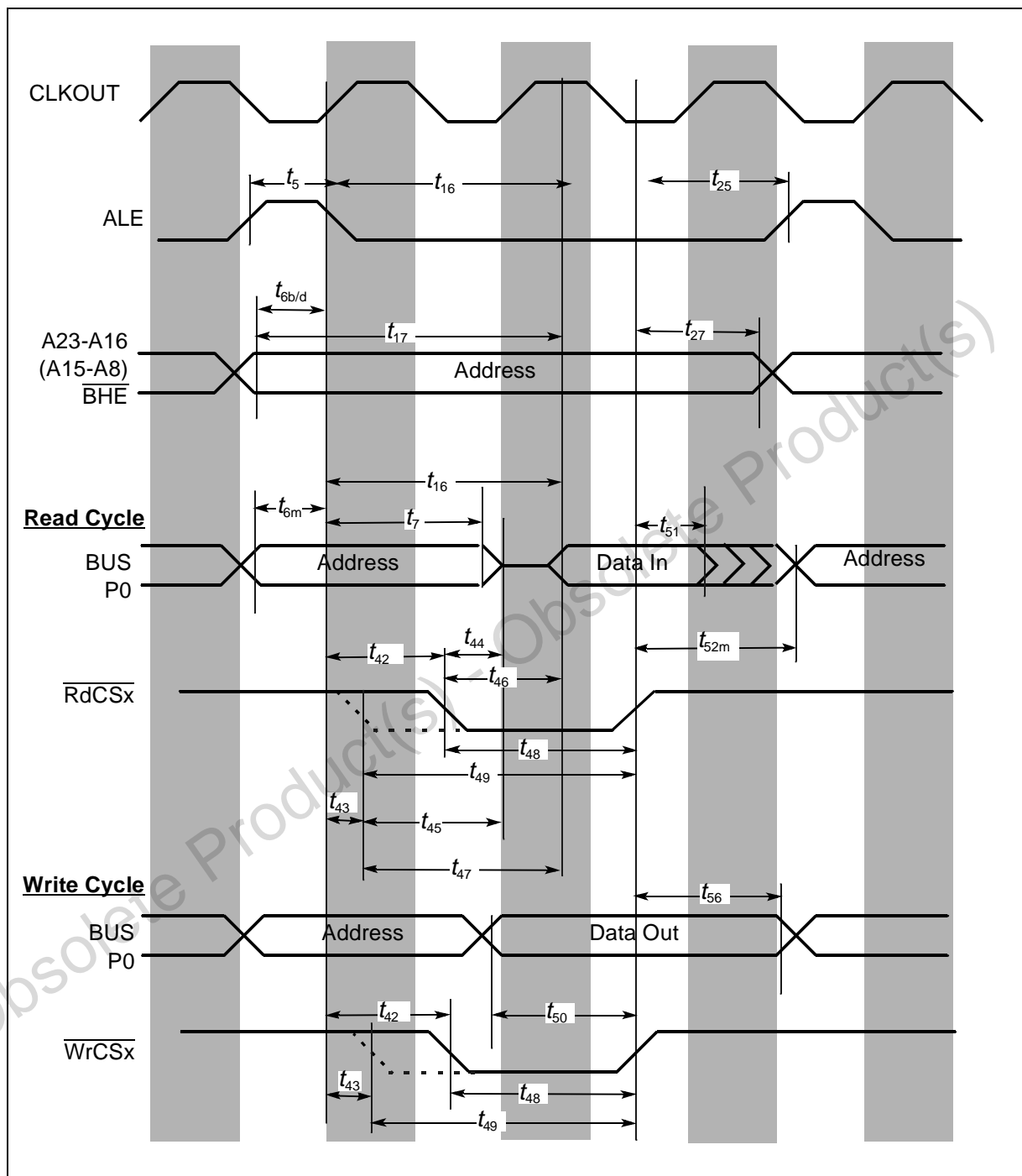


Figure 15 External memory cycle:
multiplexed bus, with/without read/write delay, normal ALE, read/write chip select

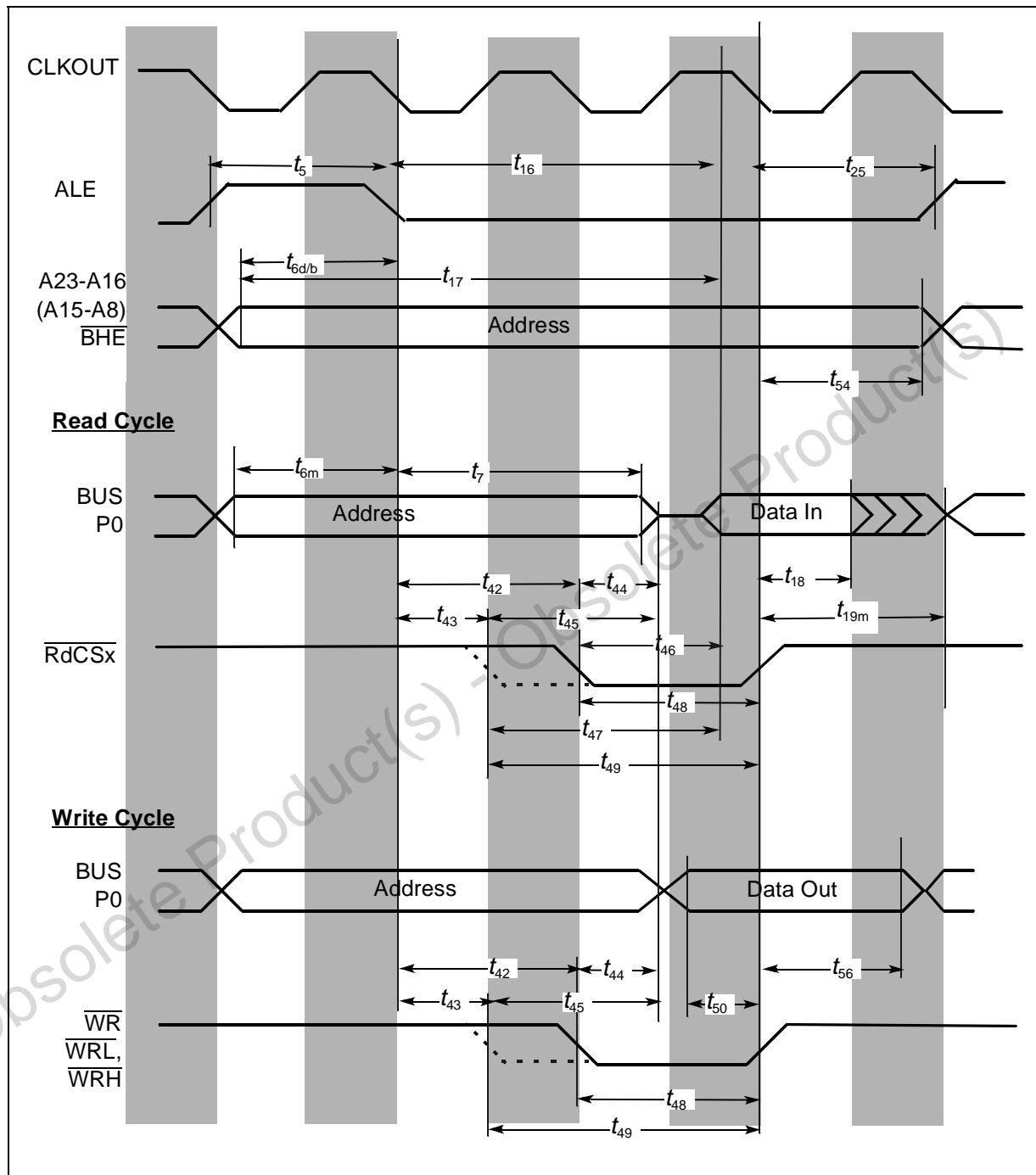


Figure 16 External memory cycle:
multiplexed bus, with/without read/write delay, extended ale, read/write chip select

15.3.4 Demultiplexed Bus
 $V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$ $V_{SS} = 0\text{ V}$ $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $C_L = 50\text{ pF}$

ALE cycle time = $4\text{ TCL} + 2t_A + t_C + t_F$ (40 ns at 50 MHz CPU clock without waitstates)

| Parameter | Symbol | Max CPU Clock 50MHz | | Variable CPU Clock 1/2TCL = 1 to 50 MHz | | Unit |
|--|-------------|---------------------|---------------------|--|----------------------------------|------|
| | | min. | max. | min. | max. | |
| ALE high time | t_5 CC | $7 + t_A$ | — | $\text{TCL} - 3 + t_A$ | — | ns |
| Address (P1, P4), $\overline{\text{BHE}}$ setup to ALE | t_6 CC | $3 + t_A$ | — | $\text{TCL} - 7 + t_A$ | — | ns |
| Address setup to $\overline{\text{RD}}$, $\overline{\text{WR}}$ (with RW-delay) | t_{80} CC | $13 + 2t_A$ | — | $2\text{TCL} - 7 + 2t_A$ | — | ns |
| Address setup to $\overline{\text{RD}}$, $\overline{\text{WR}}$ (no RW-delay) | t_{81} CC | $3 + 2t_A$ | — | $\text{TCL} - 7 + 2t_A$ | — | ns |
| $\overline{\text{RD}}$, $\overline{\text{WR}}$ low time (with RW-delay) | t_{12} CC | $13 + t_C$ | — | $2\text{TCL} - 7 + t_C$ | — | ns |
| $\overline{\text{RD}}$, $\overline{\text{WR}}$ low time (no RW-delay) | t_{13} CC | $23 + t_C$ | — | $3\text{TCL} - 7 + t_C$ | — | ns |
| $\overline{\text{RD}}$ to valid data in (with RW-delay) | t_{14} SR | — | $5 + t_C$ | — | $2\text{TCL} - 15 + t_C$ | ns |
| $\overline{\text{RD}}$ to valid data in (no RW-delay) | t_{15} SR | — | $15 + t_C$ | — | $3\text{TCL} - 15 + t_C$ | ns |
| ALE low to valid data in | t_{16} SR | — | $15 + t_A + t_C$ | — | $3\text{TCL} - 15 + t_A + t_C$ | ns |
| Address to valid data in | t_{17} SR | — | $20 + 2t_A + t_C$ | — | $4\text{TCL} - 20 + 2t_A + t_C$ | ns |
| Data hold after $\overline{\text{RD}}$ rising edge | t_{18} SR | 0 | — | 0 | — | ns |
| Data float after $\overline{\text{RD}}$ rising edge (with RW-delay) ^{1) 2)} | t_{20} SR | — | $15 + t_F + 2t_A^2$ | — | $2\text{TCL} - 5 + t_F + 2t_A^2$ | ns |
| Data float after $\overline{\text{RD}}$ rising edge (no RW-delay) ^{1) 2)} | t_{21} SR | — | $5 + t_F + 2t_A^2$ | — | $\text{TCL} - 5 + t_F + 2t_A^2$ | ns |
| Data valid to $\overline{\text{WR}}$ | t_{22} CC | $13 + t_C$ | — | $2\text{TCL} - 7 + t_C$ | — | ns |

Table 15 Demultiplexed bus

ST10R172L - ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Max CPU Clock 50MHz | | Variable CPU Clock 1/2TCL = 1 to 50 MHz | | Unit |
|---|--------------|--|-------------------|--|--------------------------|------|
| | | min. | max. | min. | max. | |
| Data hold after \overline{WR} | t_{24} CC | $5 + t_F$ | — | $TCL - 5 + t_F$ | — | ns |
| ALE rising edge after \overline{RD} , \overline{WR} | t_{26} CC | $-5 + t_F$ | — | $-5 + t_F$ | — | ns |
| Address hold after \overline{RD} , \overline{WR} | t_{28} CC | 0 (no t_F) $-9 + t_F$ ($t_F > 0$) | — | 0 (no t_F) $-9 + t_F$ ($t_F > 0$) | — | ns |
| Address hold after \overline{WRH} | t_{28h} CC | -1 (no t_F) $-8 + t_F$ ($t_F > 0$) | — | -1 (no t_F) $-8 + t_F$ ($t_F > 0$) | — | ns |
| Latched \overline{CS} setup to ALE | t_{38} CC | $-7 + t_A$ | $3 + t_A$ | $-7 + t_A$ | $3 + t_A$ | ns |
| Unlatched \overline{CS} setup to ALE | t_{38u} CC | $3 + t_A$ | — | $TCL - 7 + t_A$ | — | ns |
| Latched \overline{CS} low to Valid Data In | t_{39} SR | — | $13 + t_C + 2t_A$ | — | $3TCL - 17 + t_C + 2t_A$ | ns |
| Unlatched \overline{CS} low to Valid Data In | t_{39u} SR | — | $23 + t_C + 2t_A$ | — | $4TCL - 17 + t_C + 2t_A$ | ns |
| Latched \overline{CS} hold after \overline{RD} , \overline{WR} | t_{41} CC | $3 + t_F$ | — | $TCL - 7 + t_F$ | — | ns |
| Unlatched \overline{CS} hold after \overline{RD} , \overline{WR} | t_{41u} CC | 0 (no t_F) $-7 + t_F$ ($t_F > 0$) | — | 0 (no t_F) $-7 + t_F$ ($t_F > 0$) | — | ns |
| Address setup to \overline{RdCs} , \overline{WrCs} (with RW-delay) | t_{82} CC | $13 + 2t_A$ | — | $2TCL - 7 + 2t_A$ | — | ns |
| Address setup to \overline{RdCs} , \overline{WrCs} (no RW-delay) | t_{83} CC | $3 + 2t_A$ | — | $TCL - 7 + 2t_A$ | — | ns |
| \overline{RdCS} to Valid Data In (with RW-delay) | t_{46} SR | — | $3 + t_C$ | — | $2TCL - 17 + t_C$ | ns |
| \overline{RdCS} to Valid Data In (no RW-delay) | t_{47} SR | — | $13 + t_C$ | — | $3TCL - 17 + t_C$ | ns |
| \overline{RdCS} , \overline{WrCS} Low Time (with RW-delay) | t_{48} CC | $11 + t_C$ | — | $2TCL - 9 + t_C$ | — | ns |
| \overline{RdCS} , \overline{WrCS} Low Time (no RW-delay) | t_{49} CC | $21 + t_C$ | — | $3TCL - 9 + t_C$ | — | ns |
| Data valid to \overline{WrCS} | t_{50} CC | $13 + t_C$ | — | $2TCL - 7 + t_C$ | — | ns |

Table 15 Demultiplexed bus

ST10R172L - ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Max CPU Clock 50MHz | | Variable CPU Clock 1/2TCL = 1 to 50 MHz | | Unit |
|---|--------------------|---------------------|---------------------|--|---------------------------|------|
| | | min. | max. | min. | max. | |
| Data hold after $\overline{\text{RdCS}}$ | t ₅₁ SR | 0 | — | 0 | — | ns |
| Data float after $\overline{\text{RdCS}}$ (with RW-delay) ^{1 2} | t ₅₃ SR | — | $13 + t_F + 2t_A^2$ | — | $2TCL - 7 + t_F + 2t_A^2$ | ns |
| Data float after $\overline{\text{RdCS}}$ (no RW-delay) ^{1 2} | t ₆₈ SR | — | $3 + t_F + 2t_A^2$ | — | $TCL - 7 + t_F + 2t_A^2$ | ns |
| Address hold after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ | t ₅₅ CC | $-5 + t_F$ | — | $-5 + t_F$ | — | ns |
| Data hold after $\overline{\text{WrCS}}$ | t ₅₇ CC | $3 + t_F$ | — | $TCL - 7 + t_F$ | — | ns |

Table 15 Demultiplexed bus

- 1) Output loading is specified using Figure 10 with CL = 5 pF.
- 2) This delay assumes that the following bus cycle is a demultiplexed bus cycle and that the data bus will only be driven externally when the $\overline{\text{RD}}$ or $\overline{\text{RdCS}}$ signal becomes active. RW-delay and t_A refer to the following bus cycle. If the following bus cycle is a multiplexed bus cycle, refer to equivalent multiplexed AC timing (which are still applicable due to automatic insertion an idle state (2TCL) when switching from Demultiplexed to Multiplexed Bus Mode.

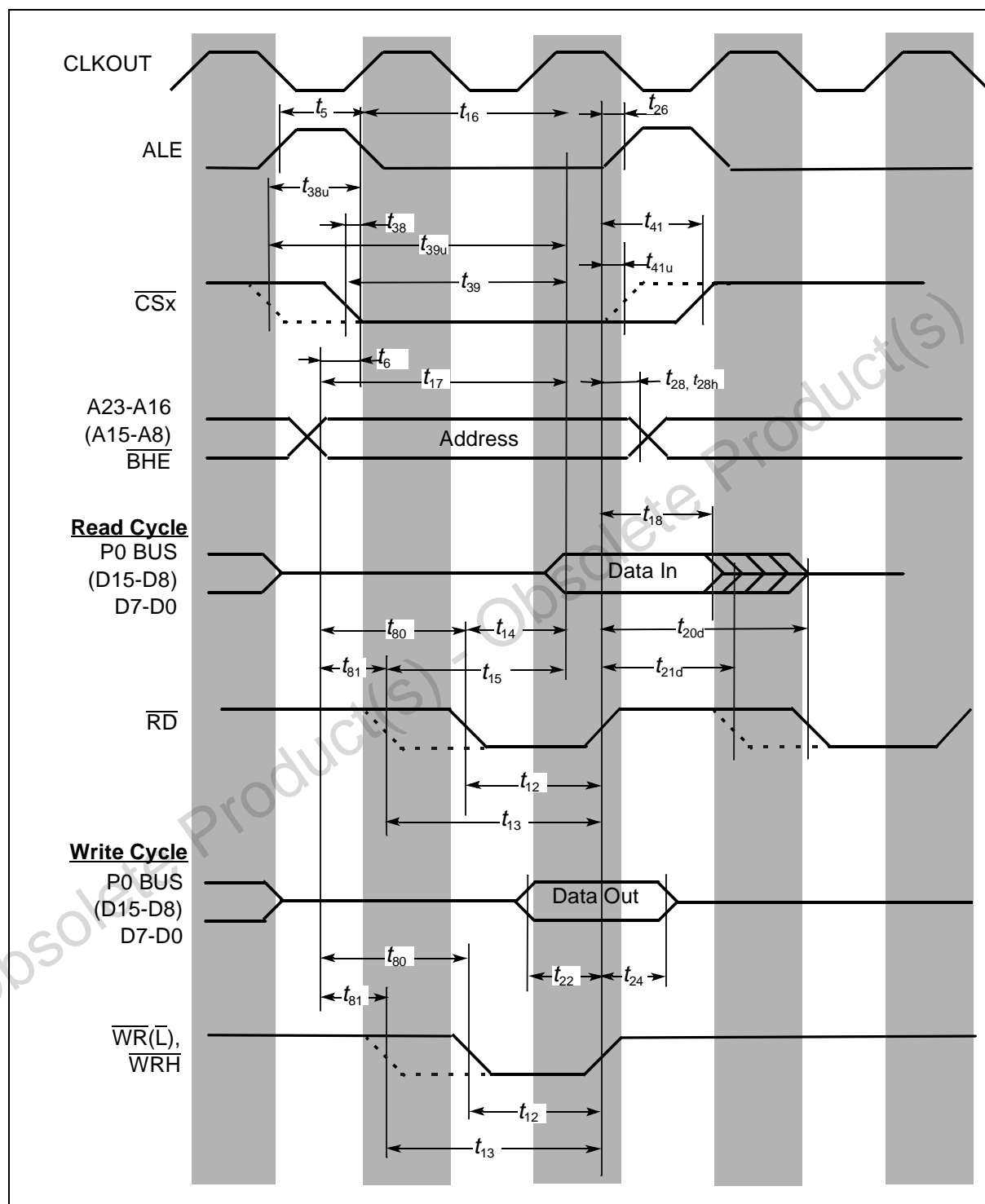
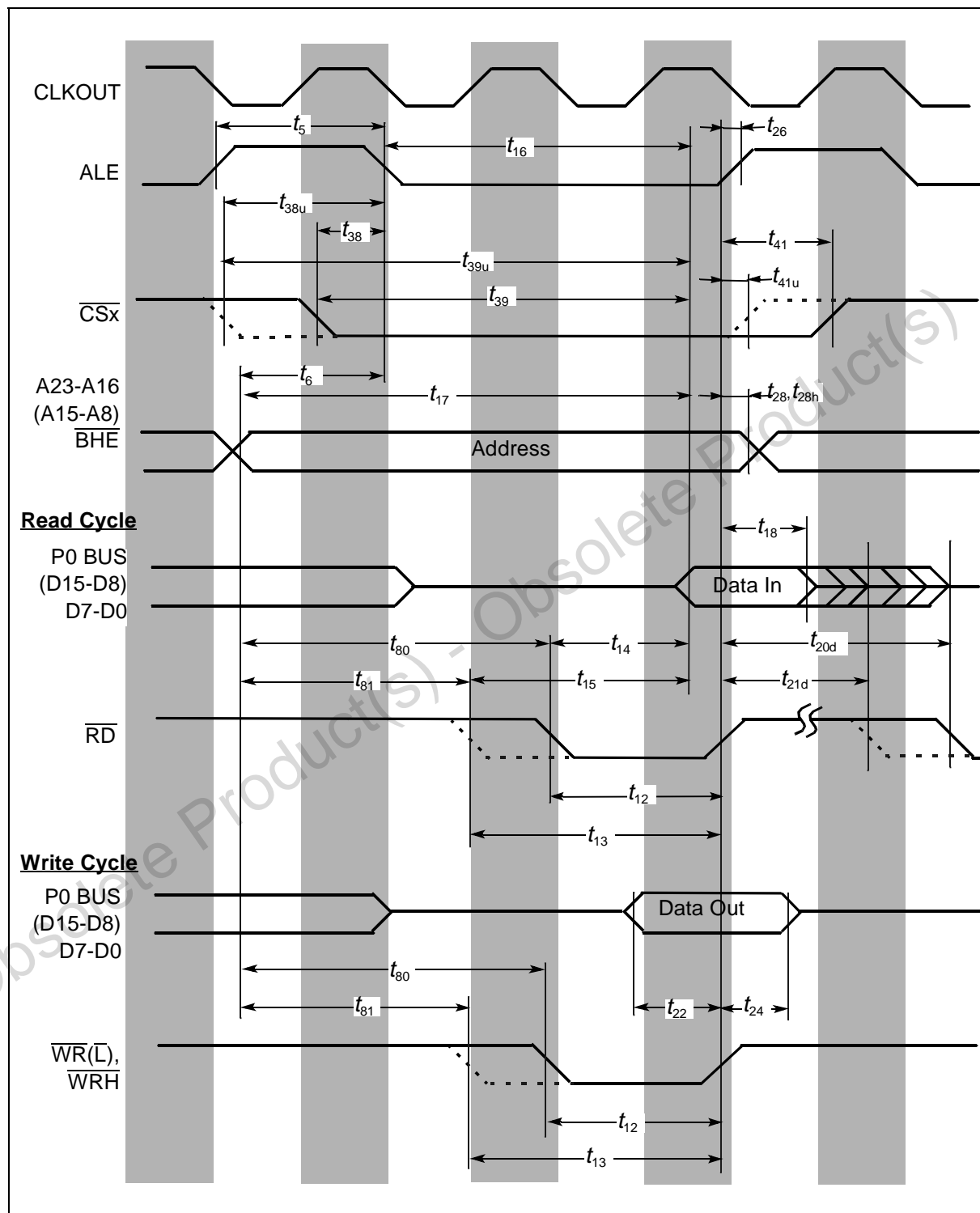


Figure 17 External memory cycle:
demultiplexed bus, with/without read/write delay, normal ALE



**Figure 18 External memory cycle:
demultiplexed bus, with/without read/write delay, extended ALE**

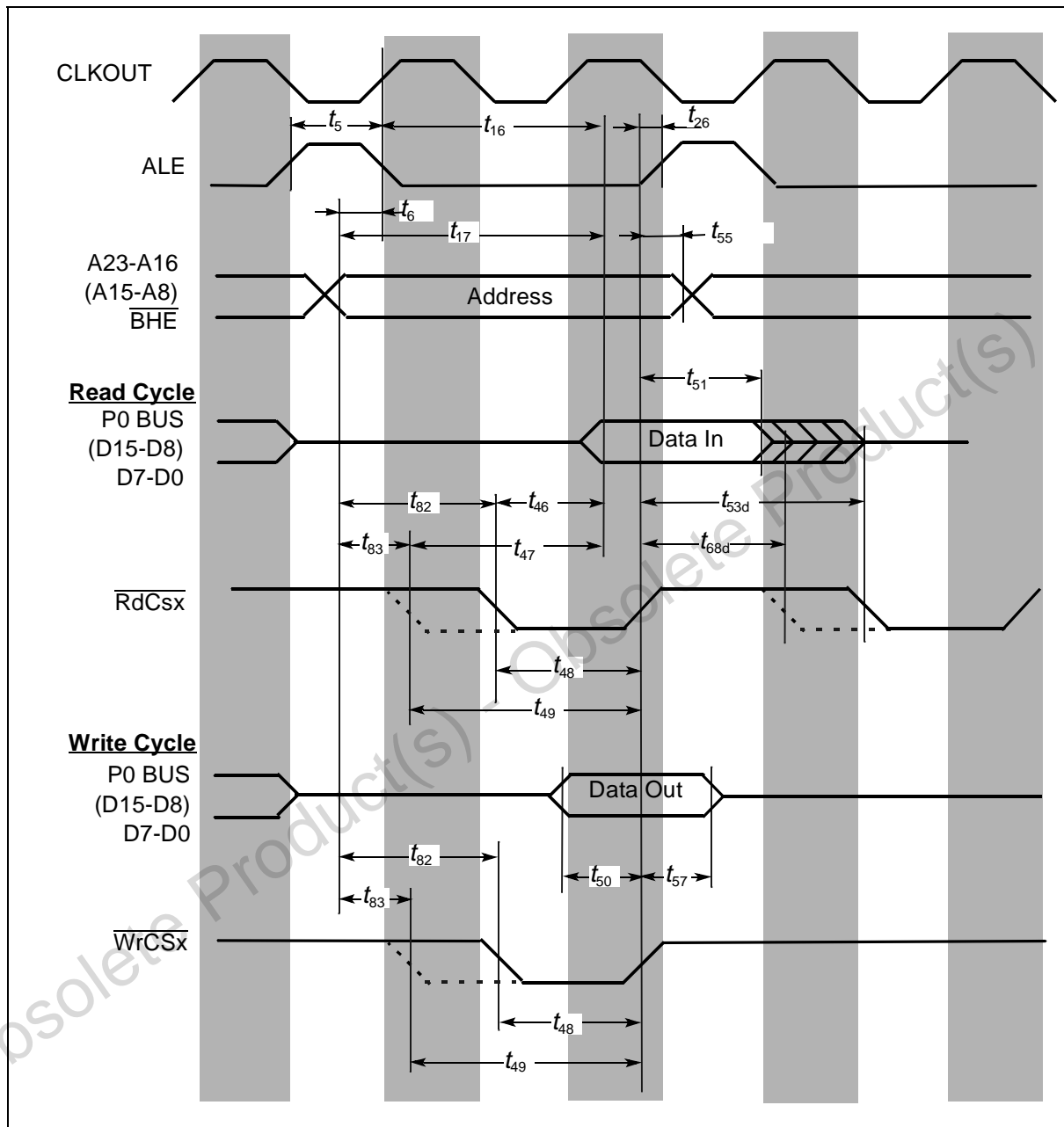


Figure 19 External memory cycle:
demultiplexed bus, with/without read/write delay, normal ALE, read/write chip select

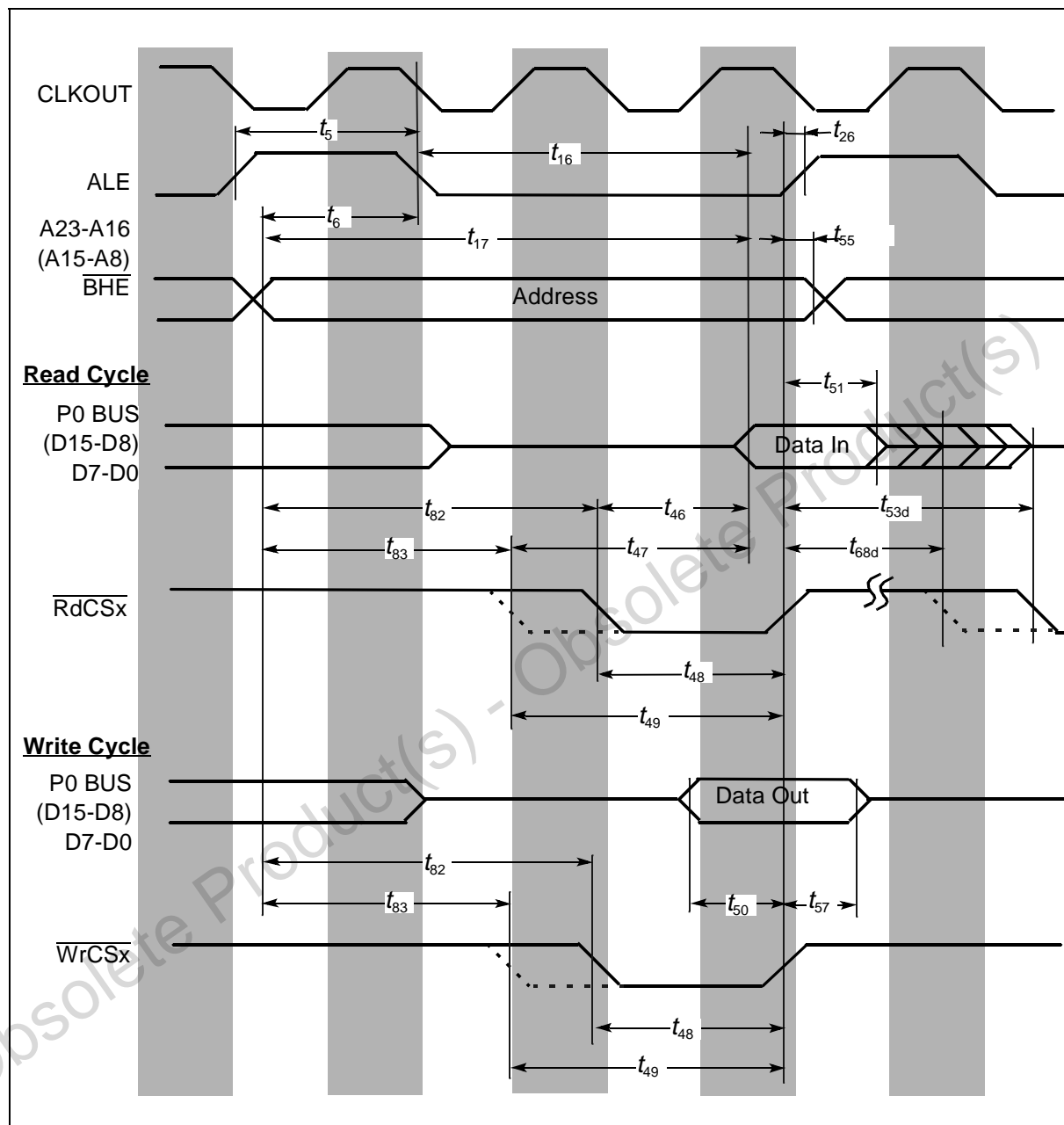


Figure 20 External memory cycle:
demultiplexed bus, no read/write delay, extended ALE, read/write chip select

15.3.5 CLKOUT and $\overline{\text{READY}}$ /READY

$V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$

$V_{SS} = 0 \text{ V}$

$T_A = -40^\circ\text{C to } +85^\circ\text{C}$

$C_L = 50 \text{ pF}$

| Parameter | Symbol | Max. CPU Clock = 50 MHz | | Variable CPU Clock 1/2TCL = 1 to 50 MHz | | Unit |
|---|--------------------|----------------------------|---|--|--|------|
| | | min. | max. | min. | max. | |
| CLKOUT cycle time | t ₂₉ CC | 20 | 20 | 2TCL | 2TCL | ns |
| CLKOUT high time | t ₃₀ CC | 5 | — | TCL – 5 | — | ns |
| CLKOUT low time | t ₃₁ CC | 5 | — | TCL – 5 | — | ns |
| CLKOUT rise time ¹⁾ | t ₃₂ CC | — | 3 ¹ | — | 3 ¹ | ns |
| CLKOUT fall time ¹⁾ | t ₃₃ CC | — | 3 ¹ | — | 3 ¹ | ns |
| CLKOUT rising edge to ALE falling edge | t ₃₄ CC | -3 + t _A | 5 + t _A | -3 + t _A | 5 + t _A | ns |
| Synchronous READY setup time to CLKOUT | t ₃₅ SR | 9 | — | 9 | — | ns |
| Synchronous READY hold time after CLKOUT | t ₃₆ SR | 0 | — | 0 | — | ns |
| Asynchronous READY low time | t ₃₇ SR | 27 | — | 2TCL + 7 | — | ns |
| Asynchronous READY setup time ²⁾ | t ₅₈ SR | 9 | — | 9 | — | ns |
| Asynchronous READY hold time ²⁾ | t ₅₉ SR | 0 | — | 0 | — | ns |
| Async. READY hold time after $\overline{\text{RD}}$, $\overline{\text{WR}}$ high (Demulti- plexed Bus) ³⁾²⁾ | t ₆₀ SR | 0 | 0 + 2t _A + t _C + t _F ³ | 0 | TCL - 10 + 2t _A + t _C + t _F ³ | ns |

Table 16 CLKOUT and $\overline{\text{READY}}$ /READY

- 1) Measured between 0.3 and 2.7 volts
- 2) These timings assure recognition at a specific clock edge for test purposes only.
- 3) Demultiplexed bus is the worst case. For multiplexed bus, 2TCL should be added to the maximum values. This adds even more time for deactivating READY.
2t_A and t_C refer to the following bus cycle, t_F refers to the current bus cycle.

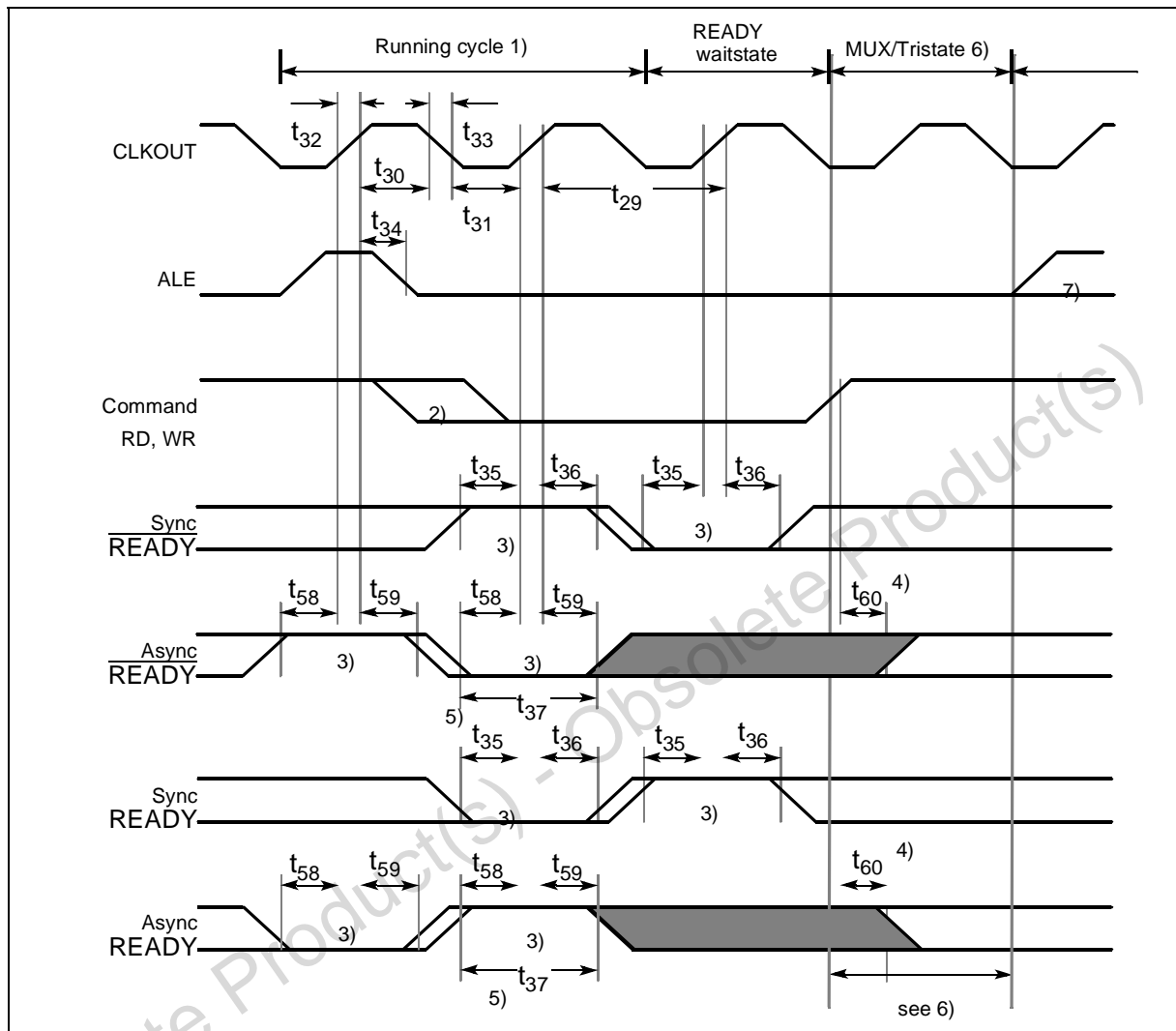


Figure 21 CLKOUT and $\overline{\text{READY}}$ /READY

- 1 Cycle as programmed, including MCTC waitstates (Example shows 0 MCTC WS).
- 2 The leading edge of the respective command depends on RW-delay.
- 3 $\overline{\text{READY}}$ (or READY) sampled HIGH (resp. LOW) at this sampling point generates a READY controlled waitstate, $\overline{\text{READY}}$ (resp. READY) sampled LOW (resp. HIGH) at this sampling point terminates the currently running bus cycle.
- 4 $\overline{\text{READY}}$ (resp. READY) may be deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{\text{RD}}$ or $\overline{\text{WR}}$).
- 5 If the Asynchronous $\overline{\text{READY}}$ (or READY) signal does not fulfill the indicated setup and hold times with respect to CLKOUT (e.g. because CLKOUT is not enabled), it must fulfill t₃₇ in order to be safely synchronized. This is guaranteed, if READY is removed in response to the command (see Note 4)).

- 6 Multiplexed bus modes have a MUX waitstate added after a bus cycle, and an additional MTTC waitstate may be inserted here. For a multiplexed bus with MTTC waitstate this delay is 2 CLKOUT cycles, for a demultiplexed bus without MTTC waitstate this delay is zero.
- 7 The next external bus cycle may start here.

Obsolete Product(s) - Obsolete Product(s)

15.3.6 External Bus Arbitration

$$V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$$

$$V_{SS} = 0\text{ V}$$

$$T_A = -40^\circ\text{C to } +85^\circ\text{C}$$

$$C_L = 50\text{ pF}$$

| Parameter | Symbol | Max. CPU Clock = 50 MHz | | Variable CPU Clock 1/2TCL = 1 to 50 MHz | | Unit |
|--|--------------------|----------------------------|------|--|------|------|
| | | min. | max. | min. | max. | |
| HOLD input setup time to CLKOUT | t ₆₁ SR | 15 | — | 15 | — | ns |
| CLKOUT to HLDA high or BREQ low delay | t ₆₂ CC | — | 10 | — | 10 | ns |
| CLKOUT to HLDA low or BREQ high delay | t ₆₃ CC | — | 10 | — | 10 | ns |
| CSx release | t ₆₄ CC | — | 15 | — | 15 | ns |
| CSx drive | t ₆₅ CC | -3 | 15 | -3 | 15 | ns |
| Other signals release | t ₆₆ CC | — | 15 | — | 15 | ns |
| Other signals drive | t ₆₇ CC | -3 | 15 | -3 | 15 | ns |

Table 17 External bus arbitration

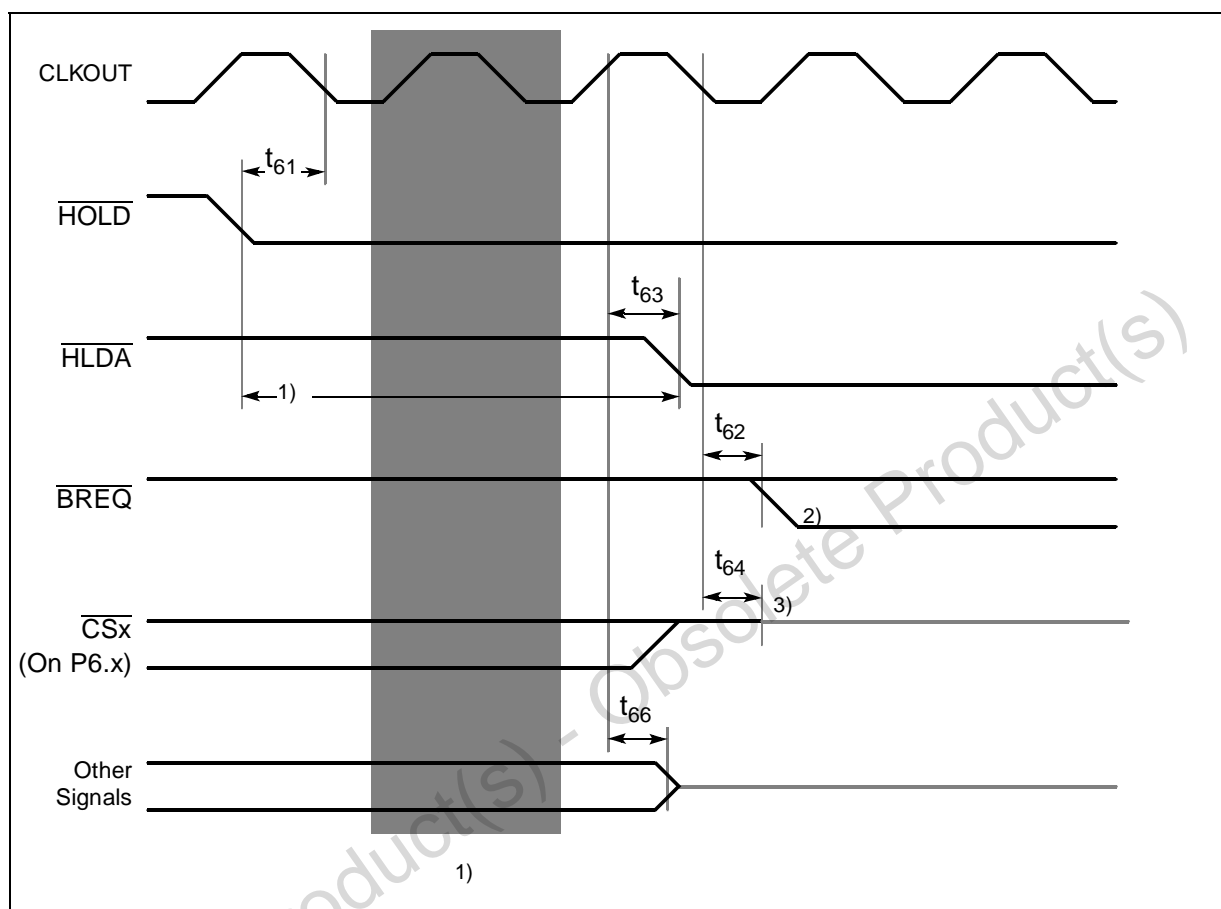


Figure 22 External bus arbitration, releasing the bus

- 1 The ST10R172L will complete the running bus cycle before granting bus access.
- 2 This is the first opportunity for \overline{BREQ} to become active.
- 3 The \overline{CS} outputs will be resistive high (pullup) after t_{64} .

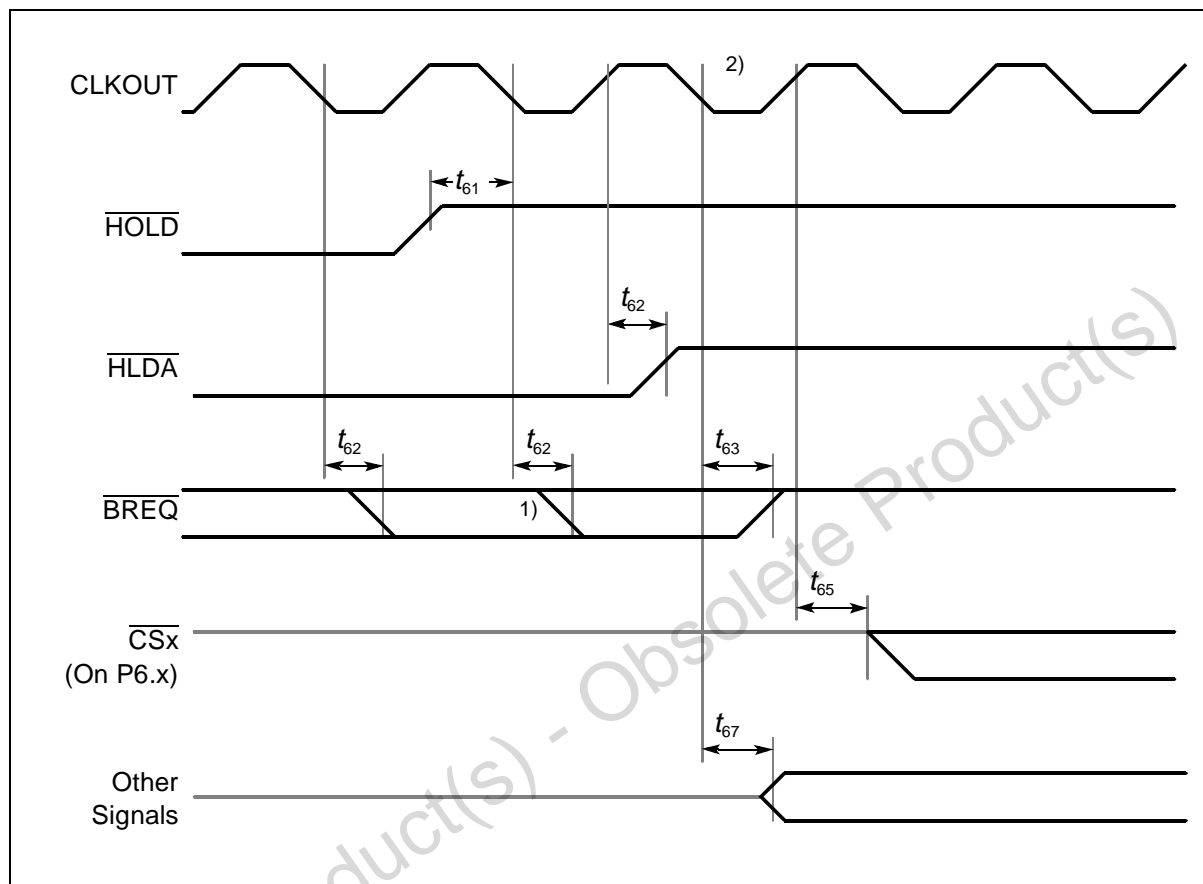


Figure 23 External bus arbitration, (regaining the bus)

- 1 This is the last chance for $\overline{\text{BREQ}}$ to trigger the regain-sequence indicated. Even if $\overline{\text{BREQ}}$ is activated earlier, the regain-sequence is initiated by $\overline{\text{HOLD}}$ going high. Please note that $\overline{\text{HOLD}}$ may also be de-activated without the ST10R172L requesting the bus.
- 2 The next ST10R172L driven bus cycle may start here.

15.3.7 External Hardware Reset

$$V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$$

$$V_{SS} = 0 \text{ V}$$

$$T_A = -40^\circ\text{C to } +85^\circ\text{C} \quad C_L = 50 \text{ pF}$$

| Parameter | Symbol | Max. CPU Clock = 50 MHz | | Variable CPU Clock 1/2TCL = 1 to 50 MHz | | Unit |
|--|--------------------|----------------------------|------|--|------|------|
| | | min. | max. | min. | max. | |
| Sync. $\overline{\text{RSTIN}}$ low time ¹⁾ | t ₇₀ SR | 50 | — | 4 TCL + 10 | — | ns |
| $\overline{\text{RSTIN}}$ low to internal reset sequence start | t ₇₁ CC | 4 | 16 | 4 | 16 | TCL |
| internal reset sequence, ($\overline{\text{RSTIN}}$ internally pulled low) | t ₇₂ CC | 1024 | 1024 | 1024 | 1024 | TCL |
| $\overline{\text{RSTIN}}$ rising edge to internal reset condition end | t ₇₃ CC | 4 | 6 | 4 | 6 | TCL |
| PORT0 system start-up configuration setup to $\overline{\text{RSTIN}}$ rising edge ²⁾ | t ₇₄ SR | 100 | — | 100 | — | ns |
| PORT0 system start-up configuration hold after $\overline{\text{RSTIN}}$ rising edge | t ₇₅ SR | 1 | 6 | 1 | 6 | TCL |
| Bus signals drive from internal reset end | t ₇₆ CC | 0 | 20 | 0 | 20 | ns |
| $\overline{\text{RSTIN}}$ low to signals release | t ₇₇ CC | — | 50 | — | 50 | ns |
| ALE rising edge from internal reset condition end | t ₇₈ CC | 8 | 8 | 8 | 8 | TCL |
| Async. $\overline{\text{RSTIN}}$ low time ¹⁾ | t ₇₉ SR | 1500 | — | 1500 | — | ns |

Table 18 External hardware reset

- 1) On power-up reset, the $\overline{\text{RSTIN}}$ pin must be asserted until a stable clock signal is available (about 10...50 ms to allow the on-chip oscillator to stabilize) and until System Start-up Configuration is correct on PORT0 (about 50 μs for internal pullup devices to load 50 pF from $V_{IL\text{min}}$ to $V_{IH\text{min}}$).
- 2) The value of bits 0 (EMU), 1 (ADAPT), 13 to 15 (Clock Configuration) are loaded during hardware reset as long as internal reset signal is active, and have an immediate effect on the system.

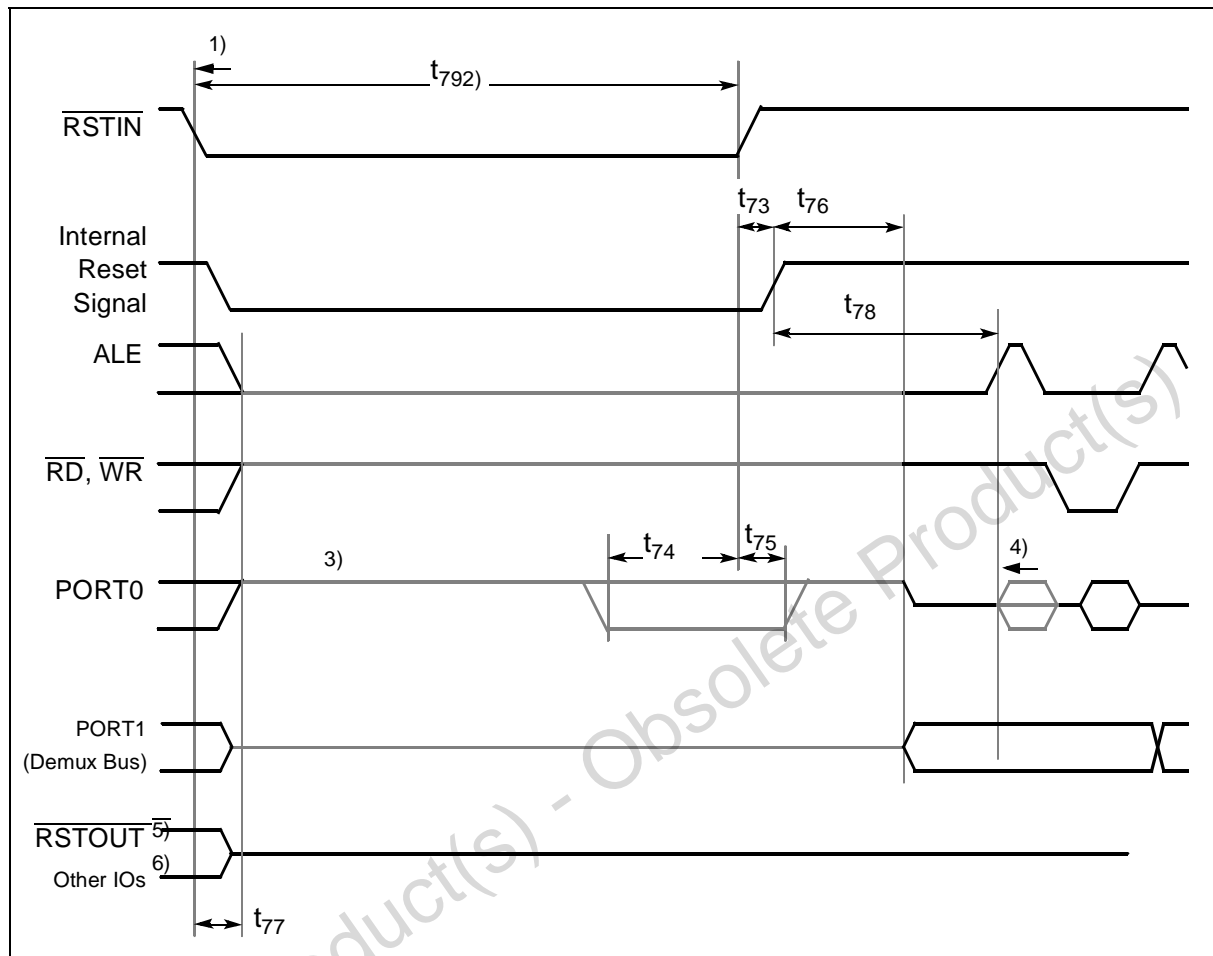


Figure 24 External asynchronous hardware reset (power-up reset): Vpp low

- 1 The ST10R172L is reset in its default state asynchronously with $\overline{\text{RSTIN}}$. The internal RAM content may be altered if an internal write access is in progress.
- 2 On power-up, $\overline{\text{RSTIN}}$ must be asserted t_{79} after a stabilized CPU clock signal is available.
- 3 Internal pullup devices are active on the PORT0 lines, so - input level is high if the respective pin is left open - or is low if the respective pin is connected to an external pulldown device.
- 4 The ST10R172L starts execution here at address 00'0000h.
- 5 $\overline{\text{RSTOUT}}$ stays active until execution of the EINIT (end of initialization) instruction.
- 6 Activation of the IO pins is controlled by software

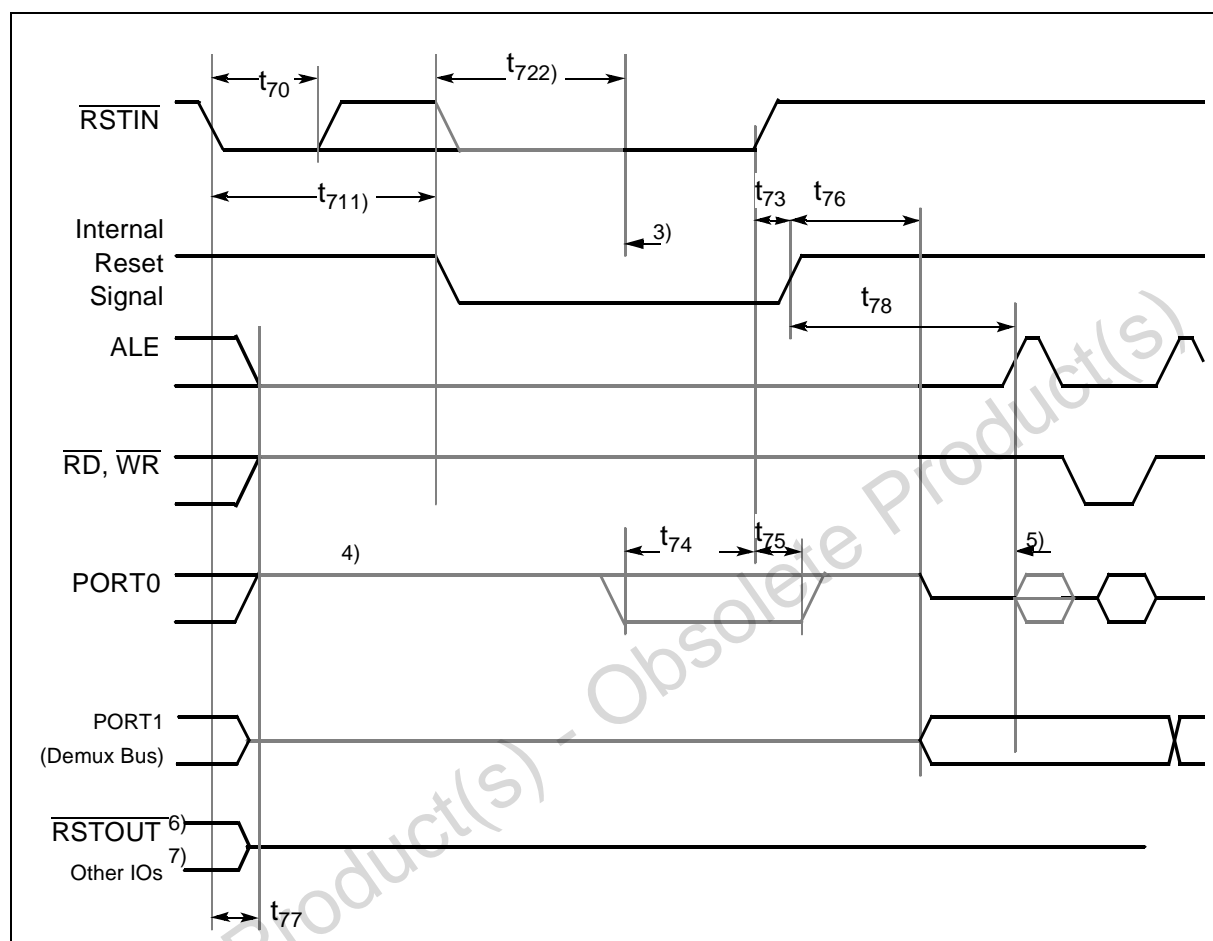


Figure 25 External synchronous hardware reset (warm reset): Vpp high

- 1 The pending internal hold states are cancelled and the current internal access cycle (if any) is completed.
- 2 $\overline{\text{RSTIN}}$ pulled low by internal device during internal reset sequence.
- 3 The reset condition may ends here if $\overline{\text{RSTIN}}$ pin is sampled high after t_{72} .
- 4 Internal pullup devices are active on the PORT0 lines. Their input level is high if the respective pin is left open, or is low if the respective pin is connected to an external pull-down device by resistive high (pullup) after t_{64} .
- 5 The ST10R172L starts execution here at address 00'0000h.
- 6 $\overline{\text{RSTOUT}}$ stays active until execution of the EINIT (End of Initialization) instruction.
- 7 Activation of the IO pins is controlled by software.

15.3.8 Synchronous Serial Port Timing

$$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V} \quad V_{SS} = 0 \text{ V}$$

$$T_A = -40^\circ\text{C to } +85^\circ\text{C} \quad C_L = 50 \text{ pF}$$

| Parameter | Symbol | Max. Baudrate = 25 MBd | | Variable Baudrate = 0.2 to 25 MBd | | Unit |
|--|---------------------|---------------------------|------|--------------------------------------|-------------------------|------|
| | | min. | max. | min. | max. | |
| SSP clock cycle time | t ₂₀₀ CC | 40 | 40 | 4 TCL | 512 TCL | ns |
| SSP clock high time | t ₂₀₁ CC | 13 | – | t ₂₀₀ /2 - 7 | – | ns |
| SSP clock low time | t ₂₀₂ CC | 13 | – | t ₂₀₀ /2 - 7 | – | ns |
| SSP clock rise time | t ₂₀₃ CC | – | 3 | – | 3 | ns |
| SSP clock fall time | t ₂₀₄ CC | – | 3 | – | 3 | ns |
| CE active before shift edge | t ₂₀₅ CC | 13 | – | t ₂₀₀ /2 - 7 | – | ns |
| CE inactive after latch edge | t ₂₀₆ CC | 33 | 47 | t ₂₀₀ - 7 | t ₂₀₀ + 7 | ns |
| Write data valid after shift edge | t ₂₀₇ CC | – | 7 | – | 7 | ns |
| Write data hold after shift edge | t ₂₀₈ CC | 0 | – | 0 | – | ns |
| Write data hold after latch edge | t ₂₀₉ CC | 15 | 25 | t ₂₀₀ /2 - 5 | t ₂₀₀ /2 + 5 | ns |
| Read data active after latch edge | t ₂₁₀ SR | 27 | – | t ₂₀₀ /2 + 7 | – | ns |
| Read data setup time before latch edge | t ₂₁₁ SR | 15 | – | 15 | – | ns |
| Read data hold time after latch edge | t ₂₁₂ SR | 0 | – | 0 | – | ns |

Table 19 Synchronous serial port timing

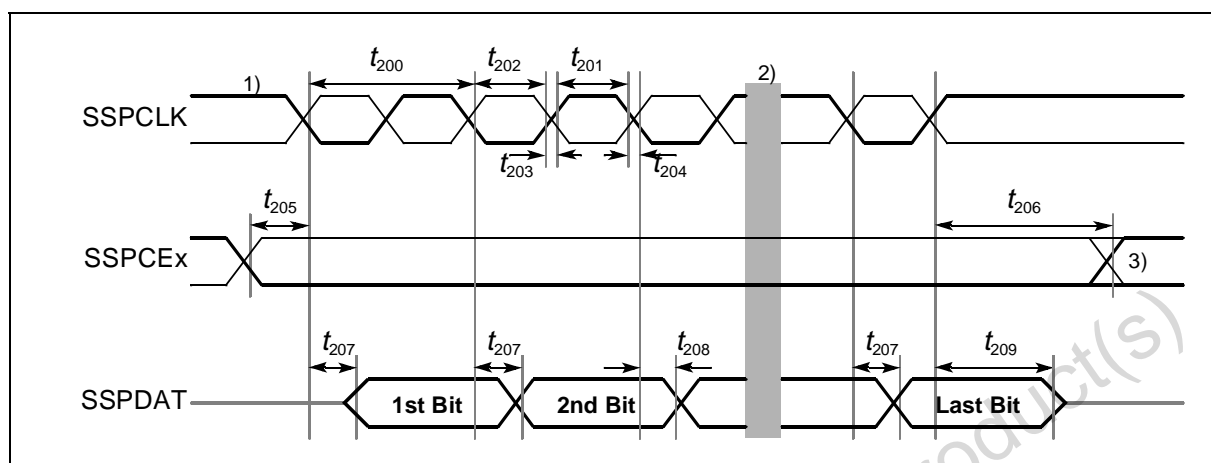


Figure 26 SSP write timing

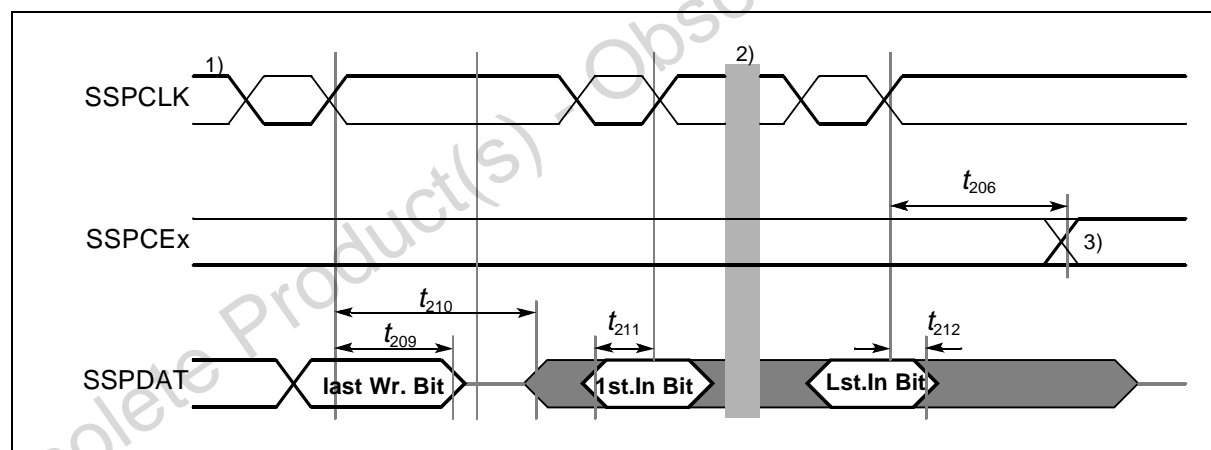


Figure 27 SSP read timing

- 1 The transition of shift and latch edge of SSPCLK is programmable. This figure uses the falling edge as shift edge (drawn bold).
- 2 The bit timing is repeated for all bits to be transmitted or received.
- 3 The active level of the chip enable lines is programmable. This figure uses an active low CE (drawn bold). At the end of a transmission or reception the CE signal is disabled in single transfer mode. In continuous transfer mode it remains active.

16 PACKAGE MECHANICAL DATA

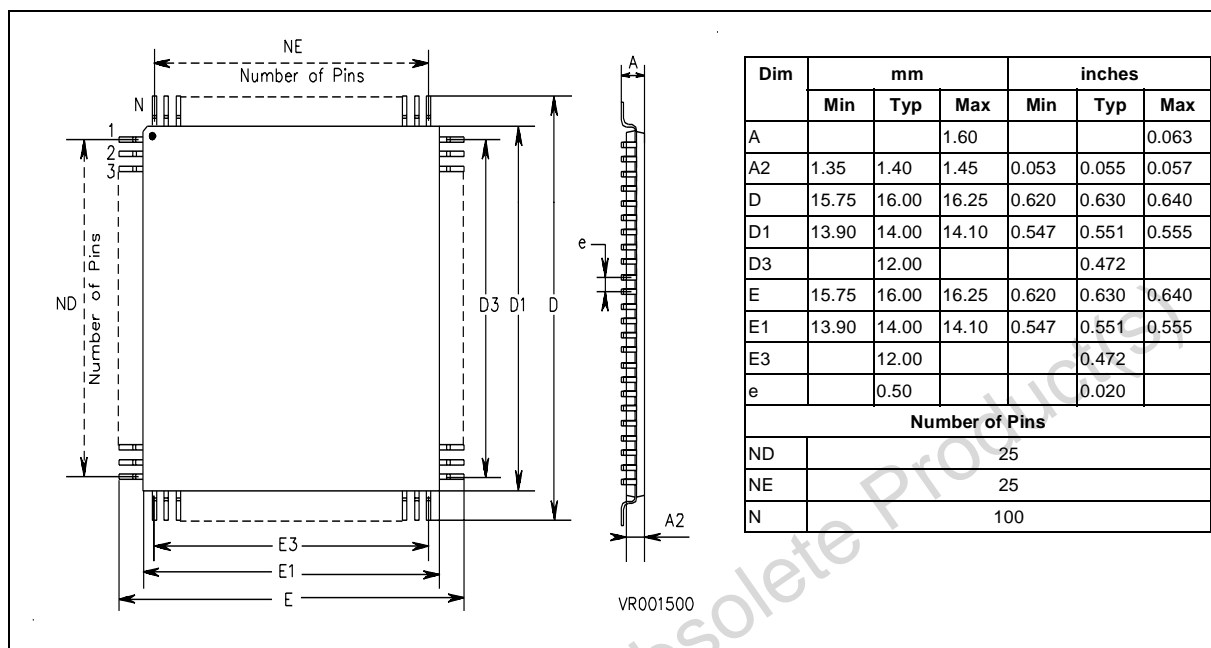


Figure 28 Package outline TQFP100 (14 x 14 mm)

17 ORDERING INFORMATION

| Sales type | Temperature range | Package |
|-------------|-------------------|------------------|
| ST10R172LT1 | 0°C to 70°C | TQFP100 (14x 14) |
| ST10R172LT6 | -40°C to +85 °C | |

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