

## Quad channel high-side driver with CurrentSense analog feedback for automotive applications

Datasheet - production data



### Features

|                                   |            |           |
|-----------------------------------|------------|-----------|
| Max transient supply voltage      | $V_{CC}$   | 40 V      |
| Operating voltage range           | $V_{CC}$   | 4 to 28 V |
| Typ. on-state resistance (per Ch) | $R_{ON}$   | 50 mΩ     |
| Current limitation (typ)          | $I_{LIMH}$ | 27 A      |
| Stand-by current (max)            | $I_{STBY}$ | 0.5 μA    |

- Automotive qualified
- General
  - Quad channel smart high-side driver with CS analog feedback
  - Very low standby current
  - Compatible with 3 V and 5 V CMOS outputs
- CurrentSense diagnostic functions
  - Analog feedback of load current with high precision proportional current mirror
  - Overload and short to ground (power limitation) indication
  - Thermal shutdown indication
  - OFF-state open-load detection
  - Output short to  $V_{CC}$  detection
  - Sense enable/disable
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation

- Self limiting of fast thermal transients
- Configurable latch-off on overtemperature or power limitation with dedicated fault reset pin
- Loss of ground and loss of  $V_{CC}$
- Reverse battery with external components
- Electrostatic discharge protection

### Applications

- All types of Automotive resistive, inductive and capacitive loads
- Specially intended for Automotive Signal Lamps (up to P27W or SAE1156 or LED Rear Combinations)

### Description

The device is a quad channel high-side driver manufactured using ST proprietary VIPower® M0-7 technology and housed in PowerSSO-16 package. The device is designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, providing protection and diagnostics.

The device integrates advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown with configurable latch-off.

A  $\overline{\text{FaultRST}}$  pin unlatches the output in case of fault or disables the latch-off functionality.

A sense enable pin allows OFF-state diagnosis to be disabled during the module low-power mode as well as external sense resistor sharing among similar devices.

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# 1 Block diagram and pin description

Figure 1: Block diagram

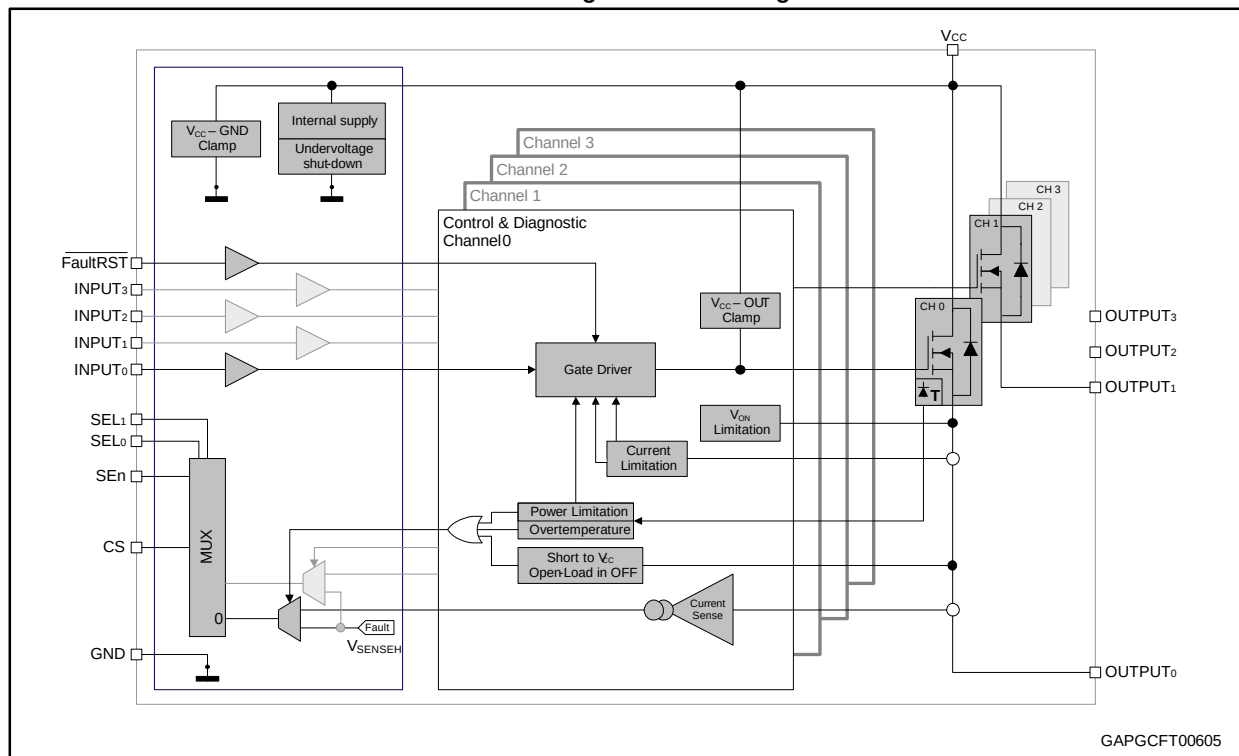


Table 1: Pin functions

| Name                      | Function                                                                                                                                                      |
|---------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| V <sub>CC</sub>           | Battery connection.                                                                                                                                           |
| OUTPUT <sub>0,1,2,3</sub> | Power output.                                                                                                                                                 |
| GND                       | Ground connection. Must be reverse battery protected by an external diode / resistor network.                                                                 |
| INPUT <sub>0,1,2,3</sub>  | Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. They control output switch state.                                     |
| CS                        | Analog current sense output pin delivers a current proportional to the load current.                                                                          |
| SEn                       | Active high, compatible with 3 V and 5 V CMOS outputs input pin; it enables the CS diagnostic pin.                                                            |
| SEL <sub>0,1</sub>        | Active high, compatible with 3 V and 5 V CMOS outputs input pin; They address the CS multiplexer.                                                             |
| FaultRST                  | Active low, compatible with 3 V and 5 V CMOS outputs input pin; it unlatches the output in case of fault; If kept low, sets the outputs in auto-restart mode. |

Figure 2: Configuration diagram (top view)

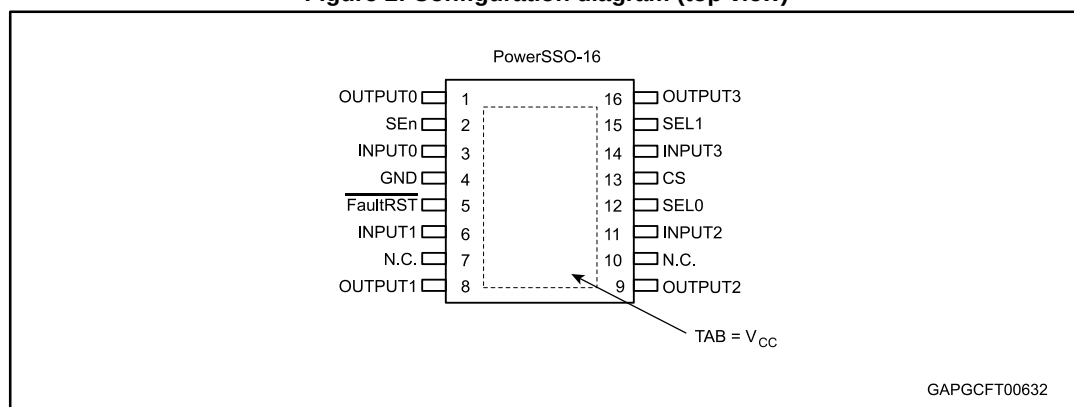


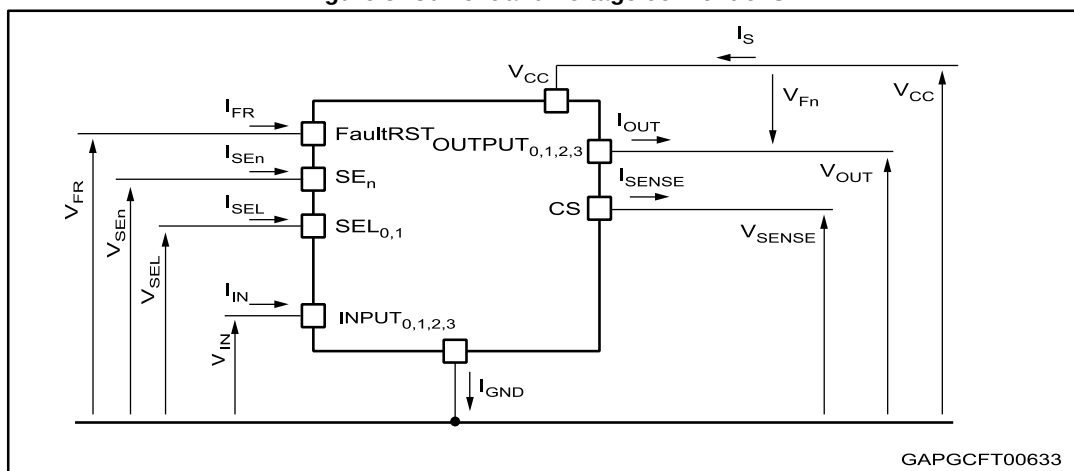
Table 2: Suggested connections for unused and not connected pins

| Connection / pin | CS                    | N.C.             | Output      | Input                  | SEn, SELx,<br>FaultRST |
|------------------|-----------------------|------------------|-------------|------------------------|------------------------|
| Floating         | Not allowed           | X <sup>(1)</sup> | X           | X                      | X                      |
| To ground        | Through 1 kΩ resistor | X                | Not allowed | Through 15 kΩ resistor | Through 15 kΩ resistor |

**Notes:**<sup>(1)</sup>X: do not care.

## 2 Electrical specification

Figure 3: Current and voltage conventions



$V_{Fn} = V_{OUTn} - V_{CC}$  during reverse battery condition.

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in [Table 3: "Absolute maximum ratings"](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Table 3: Absolute maximum ratings

| Symbol     | Parameter                                                                                     | Value              | Unit |
|------------|-----------------------------------------------------------------------------------------------|--------------------|------|
| $V_{CC}$   | DC supply voltage                                                                             | 38                 | V    |
| $-V_{CC}$  | Reverse DC supply voltage                                                                     | 0.3                |      |
| $V_{CCPK}$ | Maximum transient supply voltage (ISO 16750-2:2010 Test B clamped to 40 V; $R_L = 4 \Omega$ ) | 40                 | V    |
| $V_{CCJS}$ | Maximum jump start voltage for single pulse short circuit protection                          | 28                 | V    |
| $-I_{GND}$ | DC reverse ground pin current                                                                 | 200                | mA   |
| $I_{OUT}$  | OUTPUT <sub>0,1,2,3</sub> DC output current                                                   | Internally limited | A    |
| $-I_{OUT}$ | Reverse DC output current                                                                     | 16                 |      |
| $I_{IN}$   | INPUT <sub>0,1,2,3</sub> DC input current                                                     | -1 to 10           | mA   |
| $I_{SEn}$  | SE <sub>n</sub> DC input current                                                              |                    |      |
| $I_{SEL}$  | SEL <sub>0,1</sub> DC input current                                                           |                    |      |
| $I_{FR}$   | FaultRST DC input current                                                                     |                    |      |
| $V_{FR}$   | FaultRST DC input voltage                                                                     | 7.5                | V    |

| Symbol             | Parameter                                                                                                                    | Value      | Unit |
|--------------------|------------------------------------------------------------------------------------------------------------------------------|------------|------|
| I <sub>SENSE</sub> | CS pin DC output current ( $V_{\text{GND}} = V_{\text{CC}}$ and $V_{\text{SENSE}} < 0 \text{ V}$ )                           | 10         | mA   |
|                    | CS pin DC output current in reverse ( $V_{\text{CC}} < 0 \text{ V}$ )                                                        | -20        |      |
| E <sub>MAX</sub>   | Maximum switching energy (single pulse)<br>( $T_{\text{DEMAG}} = 0.4 \text{ ms}$ ; $T_{\text{jstart}} = 150^\circ\text{C}$ ) | 30         | mJ   |
| V <sub>ESD</sub>   | Electrostatic discharge (JEDEC 22A-114F)                                                                                     |            |      |
|                    | • INPUT <sub>0,1,2,3</sub>                                                                                                   | 4000       | V    |
|                    | • CS                                                                                                                         | 2000       | V    |
|                    | • SEn, SEL <sub>0,1</sub> , FaultRST                                                                                         | 4000       | V    |
|                    | • OUTPUT <sub>0,1,2,3</sub>                                                                                                  | 4000       | V    |
|                    | • V <sub>CC</sub>                                                                                                            | 4000       | V    |
| V <sub>ESD</sub>   | Charge device model (CDM-AEC-Q100-011)                                                                                       | 750        | V    |
| T <sub>j</sub>     | Junction operating temperature                                                                                               | -40 to 150 | °C   |
| T <sub>stg</sub>   | Storage temperature                                                                                                          | -55 to 150 |      |

## 2.2 Thermal data

Table 4: Thermal data

| Symbol                 | Parameter                                                                    | Typ. value | Unit |
|------------------------|------------------------------------------------------------------------------|------------|------|
| R <sub>thj-board</sub> | Thermal resistance junction-board (JEDEC JESD 51-5 / 51-8) <sup>(1)(2)</sup> | 6.3        | °C/W |
| R <sub>thj-amb</sub>   | Thermal resistance junction-ambient (JEDEC JESD 51-5) <sup>(1)(3)</sup>      | 57.3       |      |
| R <sub>thj-amb</sub>   | Thermal resistance junction-ambient (JEDEC JESD 51-7) <sup>(1)(2)</sup>      | 23.5       |      |

### Notes:

<sup>(1)</sup>One channel ON.

<sup>(2)</sup>Device mounted on four-layers 2s2p PCB.

<sup>(3)</sup>Device mounted on two-layers 2s0p PCB with 2 cm<sup>2</sup> heatsink copper trace.

## 2.3 Main electrical characteristics

7 V < V<sub>CC</sub> < 28 V; -40°C < T<sub>j</sub> < 150°C, unless otherwise specified.

All typical values refer to V<sub>CC</sub> = 13 V; T<sub>j</sub> = 25°C, unless otherwise specified.

Table 5: Power section

| Symbol                | Parameter                          | Test conditions                                                      | Min. | Typ. | Max. | Unit |
|-----------------------|------------------------------------|----------------------------------------------------------------------|------|------|------|------|
| V <sub>CC</sub>       | Operating supply voltage           |                                                                      | 4    | 13   | 28   | V    |
| V <sub>USD</sub>      | Undervoltage shutdown              |                                                                      |      |      | 4    |      |
| V <sub>USDReset</sub> | Undervoltage shutdown reset        |                                                                      |      |      | 5    |      |
| V <sub>USDhyst</sub>  | Undervoltage shutdown hysteresis   |                                                                      |      | 0.3  |      |      |
| R <sub>ON</sub>       | On-state resistance <sup>(1)</sup> | I <sub>OUT</sub> = 2 A; T <sub>j</sub> = 25°C                        |      | 50   |      | mΩ   |
|                       |                                    | I <sub>OUT</sub> = 2 A; T <sub>j</sub> = 150°C                       |      |      | 100  |      |
|                       |                                    | I <sub>OUT</sub> = 2 A; V <sub>CC</sub> = 4 V; T <sub>j</sub> = 25°C |      |      | 75   |      |

| Symbol               | Parameter                                                                  | Test conditions                                                                                                                                                                                  | Min. | Typ. | Max. | Unit          |
|----------------------|----------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $V_{\text{clamp}}$   | Clamp voltage                                                              | $I_S = 20 \text{ mA}; T_J = -40^\circ\text{C}$                                                                                                                                                   | 38   |      |      | V             |
|                      |                                                                            | $I_S = 20 \text{ mA}; 25^\circ\text{C} < T_J < 150^\circ\text{C}$                                                                                                                                | 41   | 46   | 52   |               |
| $I_{\text{STBY}}$    | Supply current in Standby at $V_{\text{CC}} = 13 \text{ V}$ <sup>(2)</sup> | $V_{\text{CC}} = 13 \text{ V};$<br>$V_{\text{IN}} = V_{\text{OUT}} = V_{\text{FR}} = V_{\text{SEn}} = 0 \text{ V};$<br>$V_{\text{SEL0,1}} = 0 \text{ V}; T_J = 25^\circ\text{C}$                 |      |      | 0.5  | $\mu\text{A}$ |
|                      |                                                                            | $V_{\text{CC}} = 13 \text{ V};$<br>$V_{\text{IN}} = V_{\text{OUT}} = V_{\text{FR}} = V_{\text{SEn}} = 0 \text{ V};$<br>$V_{\text{SEL0,1}} = 0 \text{ V}; T_J = 85^\circ\text{C}$ <sup>(3)</sup>  |      |      | 0.5  | $\mu\text{A}$ |
|                      |                                                                            | $V_{\text{CC}} = 13 \text{ V};$<br>$V_{\text{IN}} = V_{\text{OUT}} = V_{\text{FR}} = V_{\text{SEn}} = 0 \text{ V};$<br>$V_{\text{SEL0,1}} = 0 \text{ V}; T_J = 125^\circ\text{C}$                |      |      | 3    | $\mu\text{A}$ |
| $t_{\text{D\_STBY}}$ | Standby mode blanking time                                                 | $V_{\text{CC}} = 13 \text{ V}$<br>$V_{\text{IN}} = V_{\text{OUT}} = V_{\text{FR}} = V_{\text{SEL0,1}} = 0 \text{ V};$<br>$V_{\text{SEn}} = 5 \text{ V to } 0 \text{ V}$                          | 60   | 300  | 550  | $\mu\text{s}$ |
| $I_{\text{S(ON)}}$   | Supply current                                                             | $V_{\text{CC}} = 13 \text{ V}; V_{\text{SEn}} = V_{\text{FR}} = V_{\text{SEL0,1}} = 0 \text{ V};$<br>$V_{\text{IN0,1,2,3}} = 5 \text{ V}; I_{\text{OUT0,1,2,3}} = 0 \text{ A}$                   |      | 10   | 16   | mA            |
| $I_{\text{GND(ON)}}$ | Control stage current consumption in ON state. All channels active.        | $V_{\text{CC}} = 13 \text{ V}; V_{\text{SEn}} = 5 \text{ V};$<br>$V_{\text{FR}} = V_{\text{SEL0,1}} = 0 \text{ V}; V_{\text{IN0,1,2,3}} = 5 \text{ V};$<br>$I_{\text{OUT0,1,2,3}} = 1 \text{ A}$ |      |      | 20   | mA            |
| $I_{\text{L(off)}}$  | Off-state output current at $V_{\text{CC}} = 13 \text{ V}$ <sup>(1)</sup>  | $V_{\text{IN}} = V_{\text{OUT}} = 0 \text{ V}; V_{\text{CC}} = 13 \text{ V}; T_J = 25^\circ\text{C}$                                                                                             | 0    | 0.01 | 0.5  | $\mu\text{A}$ |
|                      |                                                                            | $V_{\text{IN}} = V_{\text{OUT}} = 0 \text{ V}; V_{\text{CC}} = 13 \text{ V}; T_J = 125^\circ\text{C}$                                                                                            | 0    |      | 3    |               |
| $V_{\text{F}}$       | Output - $V_{\text{CC}}$ diode voltage <sup>(1)</sup>                      | $I_{\text{OUT}} = -2 \text{ A}; T_J = 150^\circ\text{C}$                                                                                                                                         |      |      | 0.7  | V             |

**Notes:**<sup>(1)</sup>For each channel.<sup>(2)</sup>PowerMOS leakage included.<sup>(3)</sup>Parameter specified by design; not subject to production test.**Table 6: Switching ( $V_{\text{CC}} = 13 \text{ V}; -40^\circ\text{C} < T_J < 150^\circ\text{C}$ , unless otherwise specified)**

| Symbol                                    | Parameter                                                        | Test conditions    | Min. | Typ. | Max.                | Unit             |
|-------------------------------------------|------------------------------------------------------------------|--------------------|------|------|---------------------|------------------|
| $t_{\text{d(on)}}^{(1)}$                  | Turn-on delay time at $T_J = 25^\circ\text{C}$                   | $R_L = 6.5 \Omega$ | 10   | 35   | 120                 | $\mu\text{s}$    |
| $t_{\text{d(off)}}^{(1)}$                 | Turn-off delay time at $T_J = 25^\circ\text{C}$                  |                    | 10   | 45   | 100                 |                  |
| $(dV_{\text{OUT}}/dt)_{\text{on}}^{(1)}$  | Turn-on voltage slope at $T_J = 25^\circ\text{C}$                | $R_L = 6.5 \Omega$ | 0.1  | 0.28 | 0.7                 | V/ $\mu\text{s}$ |
| $(dV_{\text{OUT}}/dt)_{\text{off}}^{(1)}$ | Turn-off voltage slope at $T_J = 25^\circ\text{C}$               |                    | 0.1  | 0.31 | 0.7                 |                  |
| $W_{\text{ON}}$                           | Switching energy losses at turn-on ( $t_{\text{won}}$ )          | $R_L = 6.5 \Omega$ | —    | 0.26 | 0.35 <sup>(2)</sup> | mJ               |
| $W_{\text{OFF}}$                          | Switching energy losses at turn-off ( $t_{\text{woff}}$ )        | $R_L = 6.5 \Omega$ | —    | 0.23 | 0.31 <sup>(2)</sup> | mJ               |
| $t_{\text{SKEW}}^{(1)}$                   | Differential Pulse skew<br>( $t_{\text{PHL}} - t_{\text{PLH}}$ ) | $R_L = 6.5 \Omega$ | -40  | 10   | 60                  | $\mu\text{s}$    |

**Notes:**<sup>(1)</sup>See [Figure 4: "Switching times and Pulse skew"](#).<sup>(2)</sup>Parameter guaranteed by design and characterization, not subject to production test

Table 7: Logic Inputs (7 V < V<sub>CC</sub> < 28 V; -40°C < T<sub>j</sub> < 150°C)

| Symbol                                                            | Parameter                | Test conditions         | Min. | Typ. | Max. | Unit |
|-------------------------------------------------------------------|--------------------------|-------------------------|------|------|------|------|
| INPUT <sub>0,1,2,3</sub> characteristics                          |                          |                         |      |      |      |      |
| V <sub>IL</sub>                                                   | Input low level voltage  |                         |      |      | 0.9  | V    |
| I <sub>IL</sub>                                                   | Low level input current  | V <sub>IN</sub> = 0.9 V | 1    |      |      | μA   |
| V <sub>IH</sub>                                                   | Input high level voltage |                         | 2.1  |      |      | V    |
| I <sub>IH</sub>                                                   | High level input current | V <sub>IN</sub> = 2.1 V |      |      | 10   | μA   |
| V <sub>I(hyst)</sub>                                              | Input hysteresis voltage |                         | 0.2  |      |      | V    |
| V <sub>ICL</sub>                                                  | Input clamp voltage      | I <sub>IN</sub> = 1 mA  | 5.3  |      | 7.2  | V    |
|                                                                   |                          | I <sub>IN</sub> = -1 mA |      | -0.7 |      |      |
| FaultRST characteristics                                          |                          |                         |      |      |      |      |
| V <sub>FRL</sub>                                                  | Input low level voltage  |                         |      |      | 0.9  | V    |
| I <sub>FRL</sub>                                                  | Low level input current  | V <sub>IN</sub> = 0.9 V | 1    |      |      | μA   |
| V <sub>FRH</sub>                                                  | Input high level voltage |                         | 2.1  |      |      | V    |
| I <sub>FRH</sub>                                                  | High level input current | V <sub>IN</sub> = 2.1 V |      |      | 10   | μA   |
| V <sub>FR(hyst)</sub>                                             | Input hysteresis voltage |                         | 0.2  |      |      | V    |
| V <sub>FRCL</sub>                                                 | Input clamp voltage      | I <sub>IN</sub> = 1 mA  | 5.3  |      | 7.5  | V    |
|                                                                   |                          | I <sub>IN</sub> = -1 mA |      | -0.7 |      |      |
| SEL <sub>0,1</sub> characteristics (7 V < V <sub>CC</sub> < 18 V) |                          |                         |      |      |      |      |
| V <sub>SELL</sub>                                                 | Input low level voltage  |                         |      |      | 0.9  | V    |
| I <sub>SELL</sub>                                                 | Low level input current  | V <sub>IN</sub> = 0.9 V | 1    |      |      | μA   |
| V <sub>SELH</sub>                                                 | Input high level voltage |                         | 2.1  |      |      | V    |
| I <sub>SELH</sub>                                                 | High level input current | V <sub>IN</sub> = 2.1 V |      |      | 10   | μA   |
| V <sub>SEL(hyst)</sub>                                            | Input hysteresis voltage |                         | 0.2  |      |      | V    |
| V <sub>SELCL</sub>                                                | Input clamp voltage      | I <sub>IN</sub> = 1 mA  | 5.3  |      | 7.2  | V    |
|                                                                   |                          | I <sub>IN</sub> = -1 mA |      | -0.7 |      |      |
| SEn characteristics (7 V < V <sub>CC</sub> < 18 V)                |                          |                         |      |      |      |      |
| V <sub>SEnL</sub>                                                 | Input low level voltage  |                         |      |      | 0.9  | V    |
| I <sub>SEnL</sub>                                                 | Low level input current  | V <sub>IN</sub> = 0.9 V | 1    |      |      | μA   |
| V <sub>SEnH</sub>                                                 | Input high level voltage |                         | 2.1  |      |      | V    |
| I <sub>SEnH</sub>                                                 | High level input current | V <sub>IN</sub> = 2.1 V |      |      | 10   | μA   |
| V <sub>SEn(hyst)</sub>                                            | Input hysteresis voltage |                         | 0.2  |      |      | V    |
| V <sub>SEnCL</sub>                                                | Input clamp voltage      | I <sub>IN</sub> = 1 mA  | 5.3  |      | 7.2  | V    |
|                                                                   |                          | I <sub>IN</sub> = -1 mA |      | -0.7 |      |      |

Table 8: Protections (7 V < V<sub>CC</sub> < 18 V; -40°C < T<sub>j</sub> < 150°C)

| Symbol            | Parameter                                    | Test conditions                                                               | Min. | Typ. | Max. | Unit |
|-------------------|----------------------------------------------|-------------------------------------------------------------------------------|------|------|------|------|
| I <sub>LIMH</sub> | DC short circuit current                     | V <sub>CC</sub> = 13 V                                                        | 21   | 27   | 38   | A    |
|                   |                                              | 4 V < V <sub>CC</sub> < 18 V <sup>(1)</sup>                                   |      |      | 38   |      |
| I <sub>LIML</sub> | Short circuit current during thermal cycling | V <sub>CC</sub> = 13 V;<br>T <sub>R</sub> < T <sub>j</sub> < T <sub>TSD</sub> |      | 9    |      |      |

| Symbol             | Parameter                                             | Test conditions                                                                                                                           | Min.          | Typ.          | Max.          | Unit          |
|--------------------|-------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------------|---------------|---------------|
| $T_{TSD}$          | Shutdown temperature                                  |                                                                                                                                           | 150           | 175           | 200           | °C            |
| $T_R$              | Reset temperature <sup>(1)</sup>                      |                                                                                                                                           | $T_{RS} + 1$  | $T_{RS} + 7$  |               |               |
| $T_{RS}$           | Thermal reset of fault diagnostic indication          | $V_{FR} = 0\text{ V}$ ; $V_{SEn} = 5\text{ V}$ ;                                                                                          | 135           |               |               |               |
| $T_{HYST}$         | Thermal hysteresis ( $T_{TSD} - T_R$ ) <sup>(1)</sup> |                                                                                                                                           |               | 7             |               |               |
| $\Delta T_{J\_SD}$ | Dynamic temperature                                   | $T_j = -40^\circ\text{C}$ ; $V_{CC} = 13\text{ V}$                                                                                        |               | 60            |               | K             |
| $t_{LATCH\_RST}$   | Fault reset time for output unlatch <sup>(1)</sup>    | $V_{FR} = 5\text{ V to }0\text{ V}$ ;<br>$V_{SEn} = 5\text{ V}$<br>• E.g. $Ch_0$<br>$V_{IN0} = 5\text{ V}$ ;<br>$V_{SELO,1} = 0\text{ V}$ | 3             | 10            | 20            | $\mu\text{s}$ |
| $V_{DEMAC}$        | Turn-off output voltage clamp                         | $I_{OUT} = 2\text{ A}$ ; $L = 6\text{ mH}$ ;<br>$T_j = -40^\circ\text{C}$                                                                 | $V_{CC} - 38$ |               |               | V             |
|                    |                                                       | $I_{OUT} = 2\text{ A}$ ; $L = 6\text{ mH}$ ;<br>$T_j = 25^\circ\text{C to }150^\circ\text{C}$                                             | $V_{CC} - 41$ | $V_{CC} - 46$ | $V_{CC} - 52$ | V             |
| $V_{ON}$           | Output voltage drop limitation                        | $I_{OUT} = 0.2\text{ A}$                                                                                                                  |               | 20            |               | mV            |

**Notes:**

(1)Parameter guaranteed by design and characterization; not subject to production test.

**Table 9: CurrentSense (7 V < VCC < 18 V;  $-40^\circ\text{C} < T_j < 150^\circ\text{C}$ )**

| Symbol                                                | Parameter                                      | Test conditions                                                                                                  | Min. | Typ. | Max. | Unit |
|-------------------------------------------------------|------------------------------------------------|------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| V <sub>SENSE_CL</sub>                                 | Current sense clamp voltage                    | V <sub>SEn</sub> = 0 V; I <sub>SENSE</sub> = 1 mA                                                                | -17  |      | -12  | V    |
|                                                       |                                                | V <sub>SEn</sub> = 0 V; I <sub>SENSE</sub> = -1 mA                                                               |      | 7    |      |      |
| Current Sense characteristics                         |                                                |                                                                                                                  |      |      |      |      |
| K <sub>OL</sub>                                       | I <sub>OUT</sub> /I <sub>SENSE</sub>           | I <sub>OUT</sub> = 0.01 A; V <sub>SENSE</sub> = 0.5 V; V <sub>SEn</sub> = 5 V                                    | 425  |      |      |      |
| dK <sub>cal</sub> /K <sub>cal</sub> <sup>(1)(2)</sup> | Current sense ratio drift at calibration point | I <sub>OUT</sub> = 0.01 A to 0.05 A; I <sub>cal</sub> = 30 A; V <sub>SENSE</sub> = 0.5 V; V <sub>SEn</sub> = 5 V | -30  |      | 30   | %    |
| K <sub>LED</sub>                                      | I <sub>OUT</sub> /I <sub>SENSE</sub>           | I <sub>OUT</sub> = 0.05 A; V <sub>SENSE</sub> = 0.5 V; V <sub>SEn</sub> = 5 V                                    | 530  | 1390 | 2120 |      |
| dK <sub>LED</sub> /K <sub>LED</sub> <sup>(1)(2)</sup> | Current sense ratio drift                      | I <sub>OUT</sub> = 0.05 A; V <sub>SENSE</sub> = 0.5 V; V <sub>SEn</sub> = 5 V                                    | -30  |      | 30   | %    |
| K <sub>0</sub>                                        | I <sub>OUT</sub> /I <sub>SENSE</sub>           | I <sub>OUT</sub> = 0.2 A; V <sub>SENSE</sub> = 0.5 V; V <sub>SEn</sub> = 5 V                                     | 730  | 1280 | 1700 |      |
| dK <sub>0</sub> /K <sub>0</sub> <sup>(1)(2)</sup>     | Current sense ratio drift                      | I <sub>OUT</sub> = 0.2 A; V <sub>SENSE</sub> = 0.5 V; V <sub>SEn</sub> = 5 V                                     | -25  |      | 25   | %    |
| K <sub>1</sub>                                        | I <sub>OUT</sub> /I <sub>SENSE</sub>           | I <sub>OUT</sub> = 0.4 A; V <sub>SENSE</sub> = 4 V; V <sub>SEn</sub> = 5 V                                       | 830  | 1180 | 1545 |      |
| dK <sub>1</sub> /K <sub>1</sub> <sup>(1)(2)</sup>     | Current sense ratio drift                      | I <sub>OUT</sub> = 0.4 A; V <sub>SENSE</sub> = 4 V; V <sub>SEn</sub> = 5 V                                       | -20  |      | 20   | %    |
| K <sub>2</sub>                                        | I <sub>OUT</sub> /I <sub>SENSE</sub>           | I <sub>OUT</sub> = 1.5 A; V <sub>SENSE</sub> = 4 V; V <sub>SEn</sub> = 5 V                                       | 885  | 1120 | 1335 |      |

| Symbol                      | Parameter                                       | Test conditions                                                                                                                                                                                                                                                                                                             | Min. | Typ. | Max. | Unit          |
|-----------------------------|-------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $dK_2/K_2^{(1)(2)}$         | Current sense ratio drift                       | $I_{OUT} = 1.5 \text{ A}$ ; $V_{SENSE} = 4 \text{ V}$ ;<br>$V_{SEn} = 5 \text{ V}$                                                                                                                                                                                                                                          | -15  |      | 15   | %             |
| $K_3$                       | $I_{OUT}/I_{SENSE}$                             | $I_{OUT} = 4.5 \text{ A}$ ; $V_{SENSE} = 4 \text{ V}$ ;<br>$V_{SEn} = 5 \text{ V}$                                                                                                                                                                                                                                          | 990  | 1110 | 1210 |               |
| $dK_3/K_3^{(1)(2)}$         | Current sense ratio drift                       | $I_{OUT} = 4.5 \text{ A}$ ; $V_{SENSE} = 4 \text{ V}$ ;<br>$V_{SEn} = 5 \text{ V}$                                                                                                                                                                                                                                          | -10  |      | 10   | %             |
| $I_{SENSE0}$                | Current sense leakage current                   | Current sense disabled:<br>$V_{SEn} = 0 \text{ V}$ ;                                                                                                                                                                                                                                                                        | 0    |      | 0.5  | $\mu\text{A}$ |
|                             |                                                 | Current sense disabled:<br>$-1 \text{ V} < V_{SENSE} < 5 \text{ V}^{(1)}$                                                                                                                                                                                                                                                   | -0.5 |      | 0.5  |               |
|                             |                                                 | Current sense enabled:<br>$V_{SEn} = 5 \text{ V}$ All channels ON;<br>$I_{OUTX} = 0 \text{ A}$ ;<br>Ch <sub>x</sub> diagnostic selected:<br>• E.g. Ch <sub>0</sub> :<br>$V_{IN0,1,2,3} = 5 \text{ V}$ ; $V_{SEL0} = 0 \text{ V}$ ;<br>$V_{SEL1} = 0 \text{ V}$ ; $I_{OUT0} = 0 \text{ A}$ ;<br>$I_{OUT1,2,3} = 2 \text{ A}$ | 0    |      | 2    |               |
|                             |                                                 | Current sense enabled:<br>$V_{SEn} = 5 \text{ V}$ ; Ch <sub>x</sub> OFF;<br>Ch <sub>x</sub> diagnostic selected:<br>• E.g. Ch <sub>0</sub> :<br>$V_{IN0} = 0 \text{ V}$ ; $V_{IN1,2,3} = 0 \text{ V}$ ;<br>$V_{SEL0} = 5 \text{ V}$ ; $V_{SEL1} = 0 \text{ V}$ ;<br>$I_{OUT1,2,3} = 2 \text{ A}$                            | 0    |      | 2    |               |
| $V_{OUT\_MSD}^{(1)}$        | Output Voltage for Current sense shutdown       | $V_{SEn} = 5 \text{ V}$ ; $R_{SENSE} = 2.7 \text{ k}\Omega$<br>• E.g. Ch <sub>0</sub> :<br>$V_{IN0} = 5 \text{ V}$ ; $V_{SEL0} = 0 \text{ V}$ ;<br>$V_{SEL1} = 0 \text{ V}$ ; $I_{OUT0} = 2 \text{ A}$                                                                                                                      |      | 5    |      | V             |
| $V_{SENSE\_SAT}$            | CS saturation voltage                           | $V_{CC} = 7 \text{ V}$ ; $R_{SENSE} = 2.7 \text{ k}\Omega$ ;<br>$V_{SEn} = 5 \text{ V}$ ; $V_{IN0} = 5 \text{ V}$ ;<br>$V_{SEL0,1} = 0 \text{ V}$ ; $I_{OUT0} = 4.5 \text{ A}$ ;<br>$T_j = 150^\circ\text{C}$                                                                                                               | 5    |      |      | V             |
| $I_{SENSE\_SAT}^{(1)}$      | CS saturation current                           | $V_{CC} = 7 \text{ V}$ ; $V_{SENSE} = 4 \text{ V}$ ;<br>$V_{IN0} = 5 \text{ V}$ ; $V_{SEn} = 5 \text{ V}$ ;<br>$V_{SEL0,1} = 0 \text{ V}$ ; $T_j = 150^\circ\text{C}$                                                                                                                                                       | 4    |      |      | mA            |
| $I_{OUT\_SAT}^{(1)}$        | Output saturation current                       | $V_{CC} = 7 \text{ V}$ ; $V_{SENSE} = 4 \text{ V}$ ;<br>$V_{IN0} = 5 \text{ V}$ ; $V_{SEn} = 5 \text{ V}$ ;<br>$V_{SEL0,1} = 0 \text{ V}$ ; $T_j = 150^\circ\text{C}$                                                                                                                                                       | 4.8  |      |      | A             |
| <b>OFF-state diagnostic</b> |                                                 |                                                                                                                                                                                                                                                                                                                             |      |      |      |               |
| $V_{OL}$                    | OFF-state open-load voltage detection threshold | $V_{SEn} = 5 \text{ V}$ ; Ch <sub>x</sub> OFF; Ch <sub>x</sub> diagnostic selected<br>• E.g. Ch <sub>0</sub><br>$V_{IN0} = 0 \text{ V}$ ; $V_{SEL0,1} = 0 \text{ V}$                                                                                                                                                        | 2    | 3    | 4    | V             |
| $I_{L(off2)}$               | OFF-state output sink current                   | $V_{IN} = 0 \text{ V}$ ; $V_{OUT} = V_{OL}$ ;<br>$T_j = -40^\circ\text{C}$ to $125^\circ\text{C}$                                                                                                                                                                                                                           | -100 |      | -15  | $\mu\text{A}$ |

| Symbol                                                                                                                         | Parameter                                                                                                   | Test conditions                                                                                                                                                                                                                                                                                                                                            | Min. | Typ. | Max. | Unit          |
|--------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $t_{DSTKON}$                                                                                                                   | OFF-state diagnostic delay time from falling edge of INPUT (see <a href="#">Figure 6: "TDSKON"</a> )        | $V_{SEN} = 5\text{ V}$ ; $Ch_X$ ON to OFF transition;<br>$Ch_X$ diagnostic selected:<br><ul style="list-style-type: none"> <li>E.g: <math>Ch_0</math><br/> <math>V_{IN0} = 5\text{ V}</math> to <math>0\text{ V}</math>;<br/> <math>V_{SEL0,1} = 0\text{ V}</math>; <math>V_{OUT0} = 4\text{ V}</math>;<br/> <math>I_{OUT0} = 0\text{ A}</math></li> </ul> | 100  | 350  | 700  | $\mu\text{s}$ |
| $t_{D\_OL\_V}$                                                                                                                 | Settling time for valid OFF-state open-load diagnostic indication from rising edge of $SEn$                 | $V_{IN0,1,2,3} = 0\text{ V}$ ; $V_{FR} = 0\text{ V}$ ;<br>$V_{SEL0,1} = 0\text{ V}$ ; $V_{OUT0} = 4\text{ V}$ ;<br>$V_{SEN} = 0\text{ V}$ to $5\text{ V}$                                                                                                                                                                                                  |      |      | 60   | $\mu\text{s}$ |
| $t_{D\_VOL}$                                                                                                                   | OFF-state diagnostic delay time from rising edge of $V_{OUT}$                                               | $V_{SEN} = 5\text{ V}$ ; $Ch_X$ OFF;<br>$Ch_X$ diagnostic selected:<br><ul style="list-style-type: none"> <li>E.g: <math>Ch_0</math><br/> <math>V_{IN0} = 0\text{ V}</math>; <math>V_{SEL0,1} = 0\text{ V}</math>;<br/> <math>V_{OUT0} = 0\text{ V}</math> to <math>4\text{ V}</math></li> </ul>                                                           |      | 5    | 30   | $\mu\text{s}$ |
| <b>Fault diagnostic feedback (see <a href="#">Table 10: "Truth table"</a>)</b>                                                 |                                                                                                             |                                                                                                                                                                                                                                                                                                                                                            |      |      |      |               |
| $V_{SENSEH}$                                                                                                                   | Current sense output voltage in fault condition                                                             | $V_{CC} = 13\text{ V}$ ; $R_{SENSE} = 1\text{ k}\Omega$<br><ul style="list-style-type: none"> <li>E.g: <math>Ch_0</math> in open load<br/> <math>V_{IN0} = 0\text{ V}</math>; <math>V_{SEN} = 5\text{ V}</math>;<br/> <math>V_{SEL0,1} = 0\text{ V}</math>; <math>I_{OUT0} = 0\text{ A}</math>;<br/> <math>V_{OUT0} = 4\text{ V}</math></li> </ul>         | 5    |      | 6.6  | V             |
| $I_{SENSEH}$                                                                                                                   | Current sense output current in fault condition                                                             | $V_{CC} = 13\text{ V}$ ; $V_{SENSE} = 5\text{ V}$                                                                                                                                                                                                                                                                                                          | 7    | 20   | 30   | mA            |
| <b>Current sense timings (current sense mode - see <a href="#">Figure 5: "Current sense timings (current sense mode)"</a>)</b> |                                                                                                             |                                                                                                                                                                                                                                                                                                                                                            |      |      |      |               |
| $t_{DSENSE1H}$                                                                                                                 | Current sense settling time from rising edge of $SEn$                                                       | $V_{IN} = 5\text{ V}$ ; $V_{SEN} = 0\text{ V}$ to $5\text{ V}$ ;<br>$R_{SENSE} = 1\text{ k}\Omega$ ; $R_L = 6.5\text{ }\Omega$                                                                                                                                                                                                                             |      |      | 60   | $\mu\text{s}$ |
| $t_{DSENSE1L}$                                                                                                                 | Current sense disable delay time from falling edge of $SEn$                                                 | $V_{SEN} = 5\text{ V}$ to $0\text{ V}$ ;<br>$R_{SENSE} = 1\text{ k}\Omega$ ; $R_L = 6.5\text{ }\Omega$                                                                                                                                                                                                                                                     |      | 5    | 20   | $\mu\text{s}$ |
| $t_{DSENSE2H}$                                                                                                                 | Current sense settling time from rising edge of INPUT                                                       | $V_{IN} = 0\text{ V}$ to $5\text{ V}$ ; $V_{SEN} = 5\text{ V}$ ;<br>$R_{SENSE} = 1\text{ k}\Omega$ ; $R_L = 6.5\text{ }\Omega$                                                                                                                                                                                                                             |      | 100  | 250  | $\mu\text{s}$ |
| $\Delta t_{DSENSE2H}$                                                                                                          | Current sense settling time from rising edge of $I_{OUT}$ (dynamic response to a step change of $I_{OUT}$ ) | $V_{IN} = 5\text{ V}$ ; $V_{SEN} = 5\text{ V}$ ;<br>$R_{SENSE} = 1\text{ k}\Omega$ ;<br>$I_{SENSE} = 90\text{ \%}$ of $I_{SENSEMAX}$ ;<br>$R_L = 6.5\text{ }\Omega$                                                                                                                                                                                        |      |      | 100  | $\mu\text{s}$ |
| $t_{DSENSE2L}$                                                                                                                 | Current sense turn-off delay time from falling edge of INPUT                                                | $V_{IN} = 5\text{ V}$ to $0\text{ V}$ ; $V_{SEN} = 5\text{ V}$ ;<br>$R_{SENSE} = 1\text{ k}\Omega$ ; $R_L = 6.5\text{ }\Omega$                                                                                                                                                                                                                             |      | 50   | 250  | $\mu\text{s}$ |

**Notes:**

(1)Parameter defined by design. Not subject to production test.

(2)All values refer to  $V_{CC} = 13\text{ V}$ ;  $T_j = 25^\circ\text{C}$ , unless otherwise specified.

Figure 4: Switching times and Pulse skew

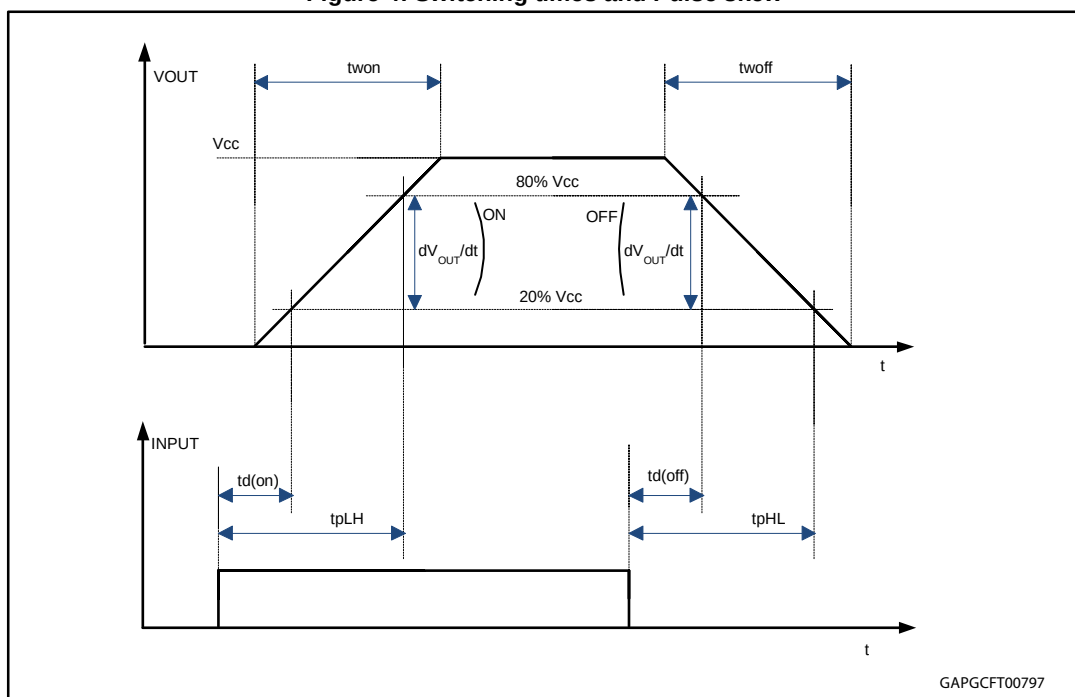


Figure 5: Current sense timings (current sense mode)

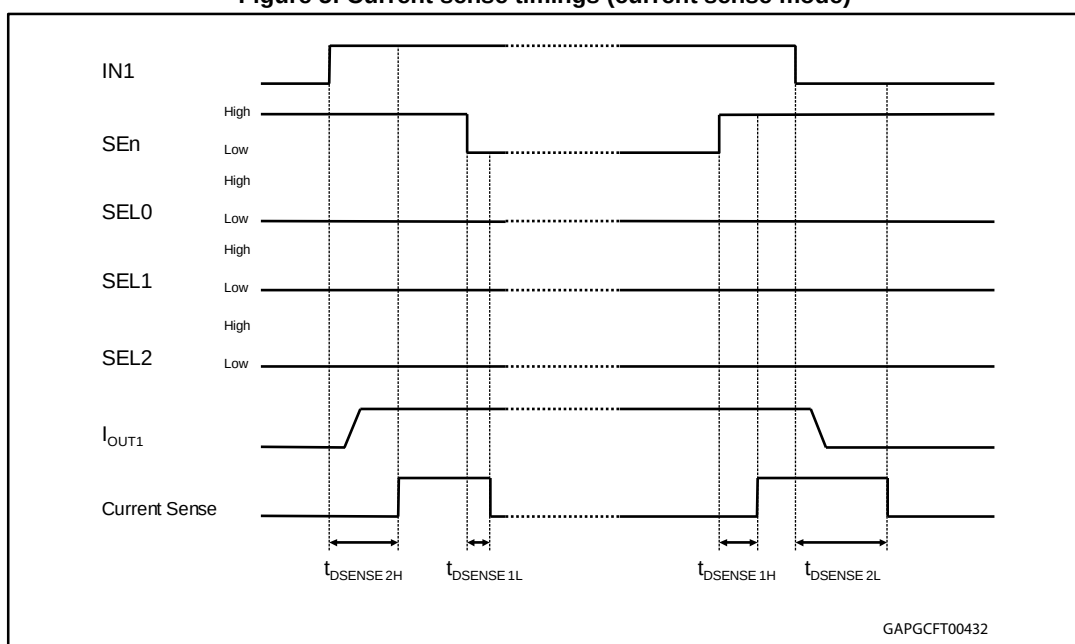


Figure 6: TDSKON

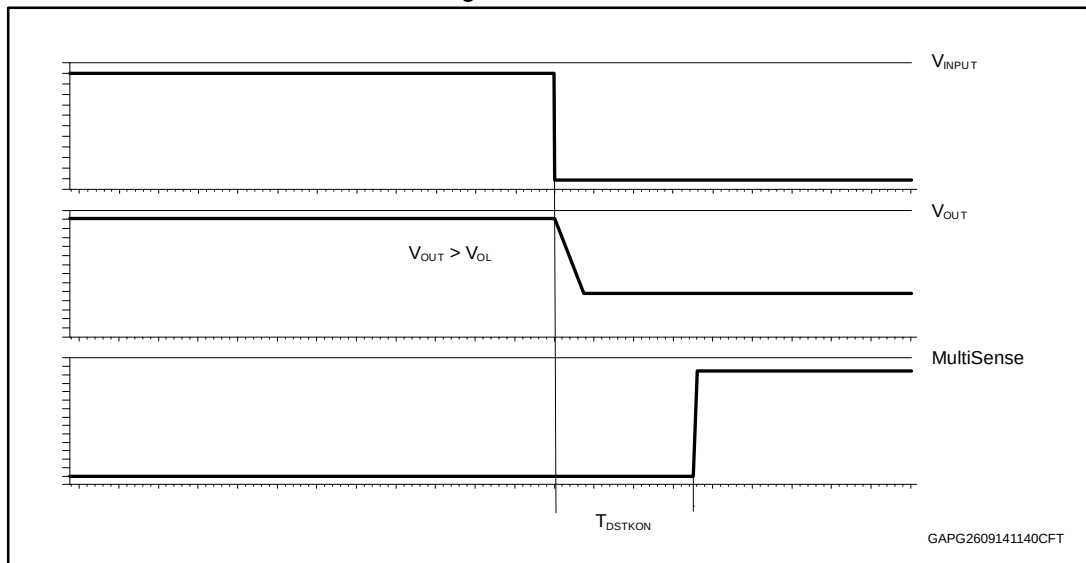


Table 10: Truth table

| Mode                    | Conditions                                                                               | IN <sub>x</sub> | FR | SEn     | SEL <sub>x</sub> | OUT <sub>x</sub> | Current sense | Comments                                                   |
|-------------------------|------------------------------------------------------------------------------------------|-----------------|----|---------|------------------|------------------|---------------|------------------------------------------------------------|
| Standby                 | All logic inputs low                                                                     | L               | L  | L       | L                | L                | Hi-Z          | Low quiescent current consumption                          |
| Normal                  | Nominal load connected;<br>$T_j < 150^\circ\text{C}$                                     | L               | X  | See (1) |                  | L                | See (1)       |                                                            |
|                         |                                                                                          | H               | L  |         |                  | H                | See (1)       | Outputs configured for auto-restart                        |
|                         |                                                                                          | H               | H  |         |                  | H                | See (1)       | Outputs configured for Latch-off                           |
| Overload                | Overload or short to GND causing:<br>$T_j > T_{TSD}$ or<br>$\Delta T_j > \Delta T_{LSD}$ | L               | X  | See (1) |                  | L                | See (1)       |                                                            |
|                         |                                                                                          | H               | L  |         |                  | H                | See (1)       | Output cycles with temperature hysteresis                  |
|                         |                                                                                          | H               | H  |         |                  | L                | See (1)       | Output latches-off                                         |
| Under-voltage           | $V_{CC} < V_{USD}$ (falling)                                                             | X               | X  | X       | X                | L<br>L           | Hi-Z<br>Hi-Z  | Re-start when<br>$V_{CC} > V_{USD} + V_{USDhyst}$ (rising) |
| OFF-state diagnostics   | Short to $V_{CC}$                                                                        | L               | X  | See (1) |                  | H                | See (1)       |                                                            |
|                         | Open-load                                                                                | L               | X  |         |                  | H                | See (1)       | External pull-up                                           |
| Negative output voltage | Inductive loads turn-off                                                                 | L               | X  | See (1) |                  | < 0 V            | See (1)       |                                                            |

**Notes:**(1) Refer to [Table 11: "Current sense multiplexer addressing"](#)

Table 11: Current sense multiplexer addressing

| SEn | SEL <sub>1</sub> | SEL <sub>0</sub> | MUX channel          | Current sense output         |                          |                              |                 |
|-----|------------------|------------------|----------------------|------------------------------|--------------------------|------------------------------|-----------------|
|     |                  |                  |                      | Nomal mode                   | Overload                 | OFF-state diag.<br>(1)(2)(3) | Negative output |
| L   | X                | X                |                      | Hi-Z                         |                          |                              |                 |
| H   | L                | L                | Channel 0 diagnostic | $I_{SENSE} = 1/K * I_{OUT0}$ | $V_{SENSE} = V_{SENSEH}$ | $V_{SENSE} = V_{SENSEH}$     | Hi-Z            |
| H   | L                | H                | Channel 1 diagnostic | $I_{SENSE} = 1/K * I_{OUT1}$ | $V_{SENSE} = V_{SENSEH}$ | $V_{SENSE} = V_{SENSEH}$     | Hi-Z            |
| H   | H                | L                | Channel 2 diagnostic | $I_{SENSE} = 1/K * I_{OUT2}$ | $V_{SENSE} = V_{SENSEH}$ | $V_{SENSE} = V_{SENSEH}$     | Hi-Z            |
| H   | H                | H                | Channel 3 diagnostic | $I_{SENSE} = 1/K * I_{OUT3}$ | $V_{SENSE} = V_{SENSEH}$ | $V_{SENSE} = V_{SENSEH}$     | Hi-Z            |

**Notes:**

(1) In case the output channel corresponding to the selected MUX channel is latched off while the relevant input is low, CS pin delivers feedback according to OFF-State diagnostic.

(2) Example 1: FR = 1; IN<sub>0</sub> = 0; OUT<sub>0</sub> = L (latched); MUX channel = channel 0 diagnostic; CS = 0

(3) Example 2: FR = 1; IN<sub>0</sub> = 0; OUT<sub>0</sub> = latched, V<sub>OUT0</sub> > V<sub>OL</sub>; MUX channel = channel 0 diagnostic; CS = V<sub>SENSEH</sub>

## 2.4 Waveforms

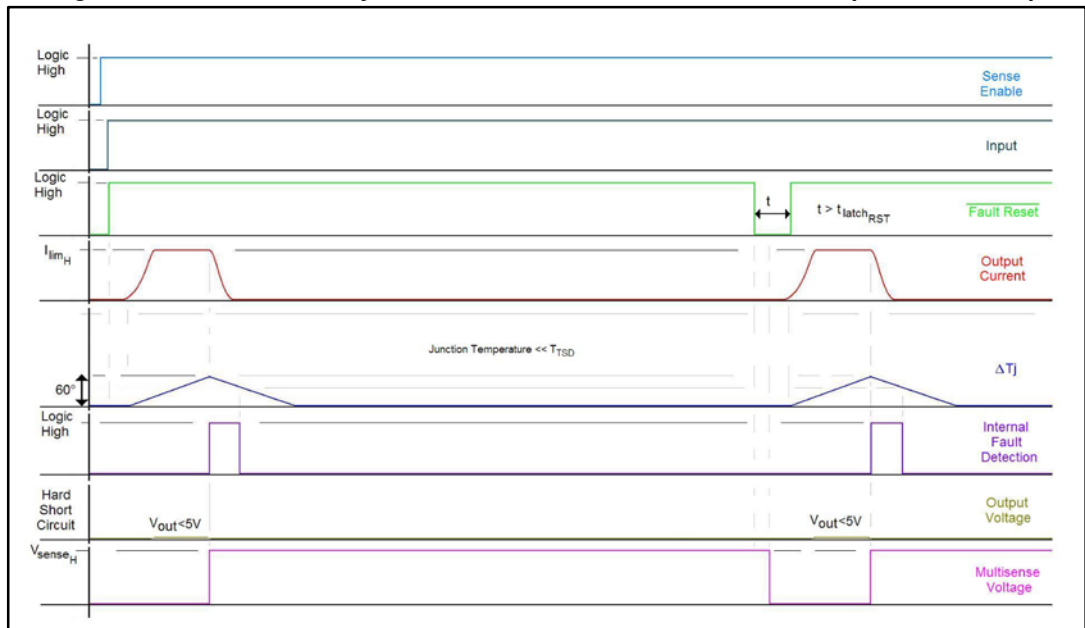
Figure 7: Latch functionality - behavior in hard short circuit condition (T<sub>AMB</sub> << T<sub>TSD</sub>)

Figure 8: Latch functionality - behavior in hard short circuit condition

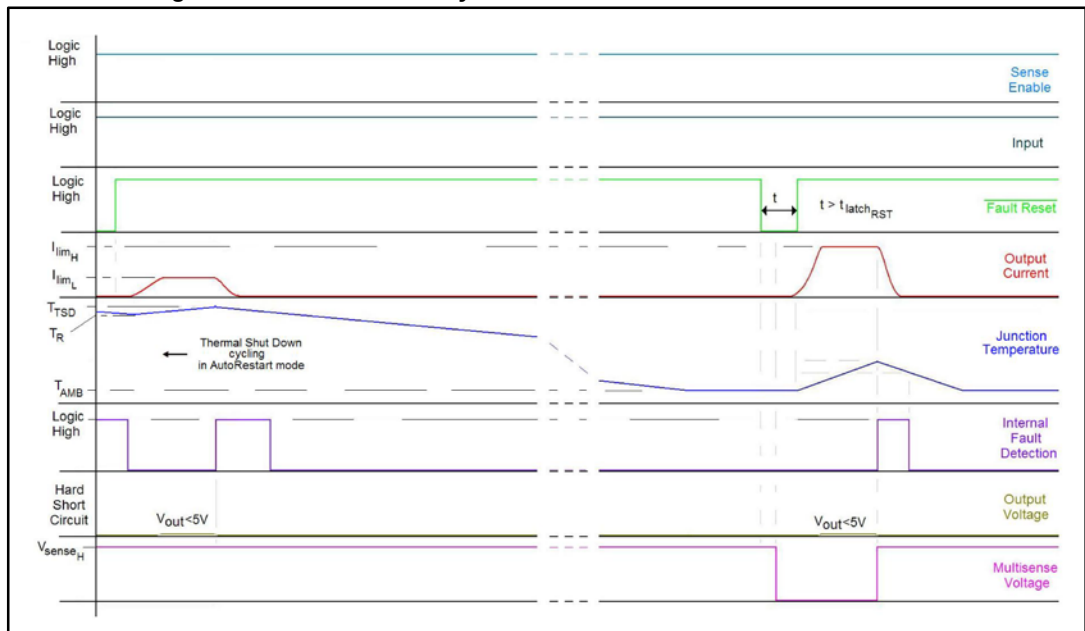


Figure 9: Latch functionality - behavior in hard short circuit condition (autorestart mode + latch off)

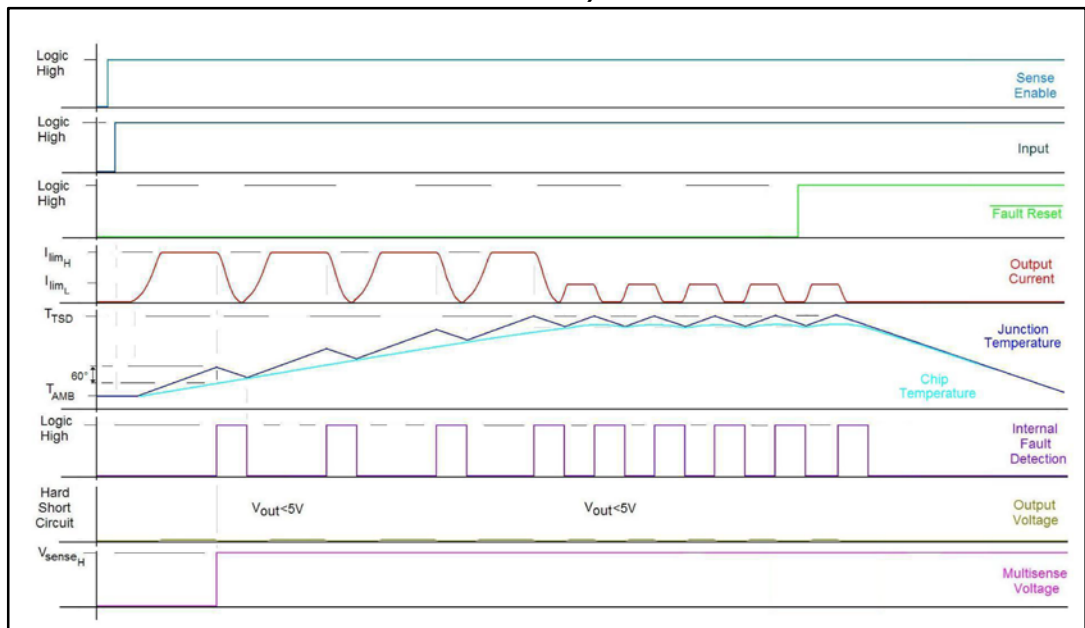


Figure 10: Standby mode activation

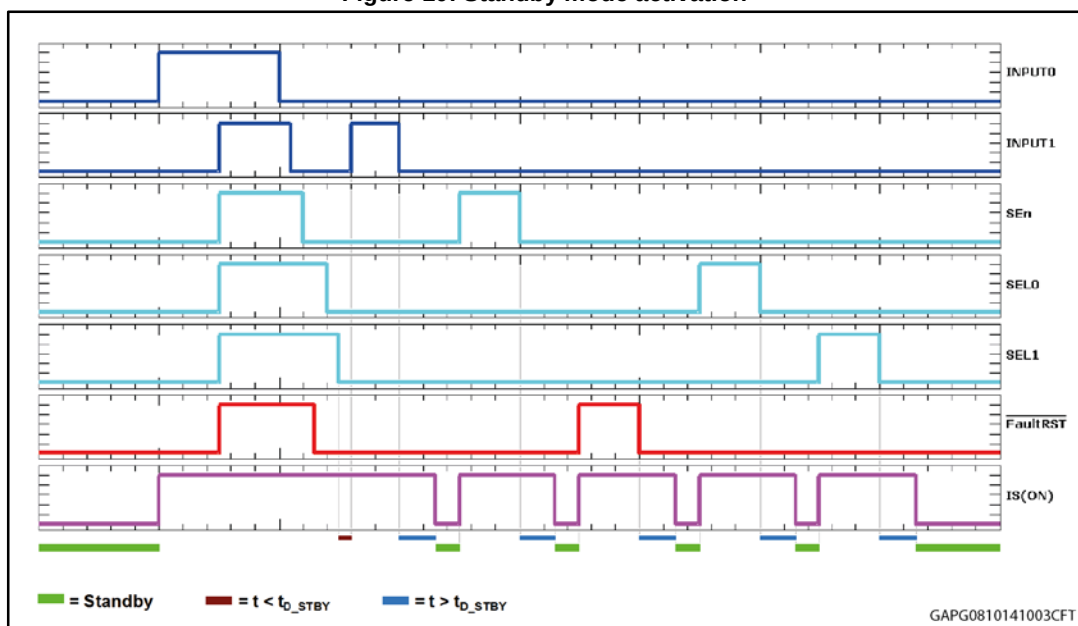
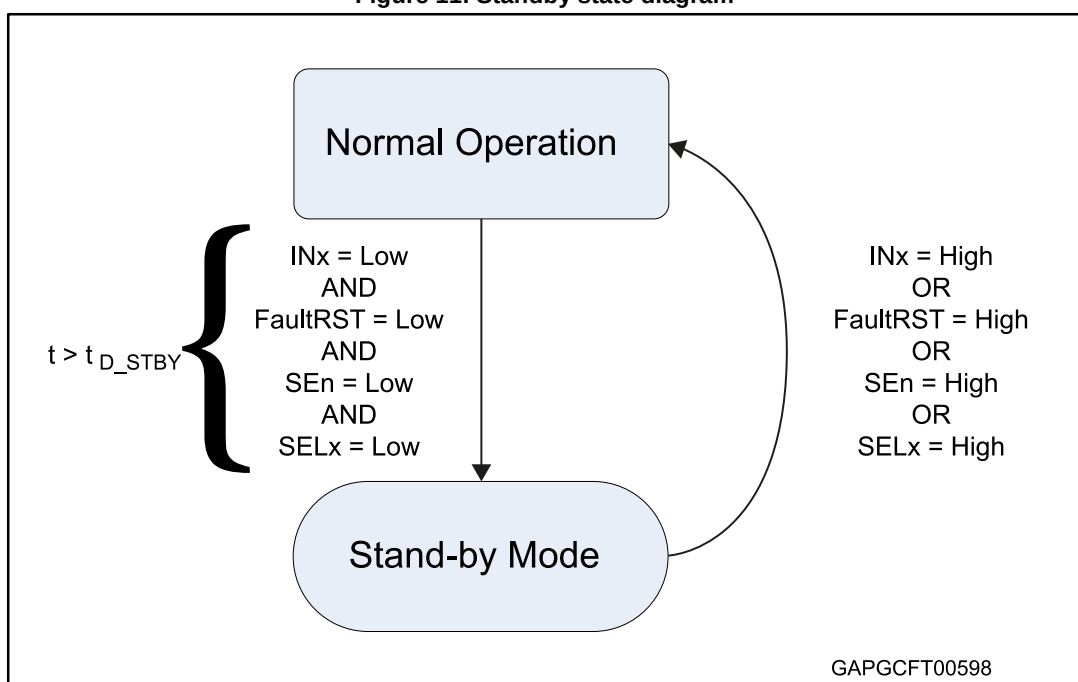


Figure 11: Standby state diagram



## 2.5 Electrical characteristics curves

Figure 12: OFF-state output current

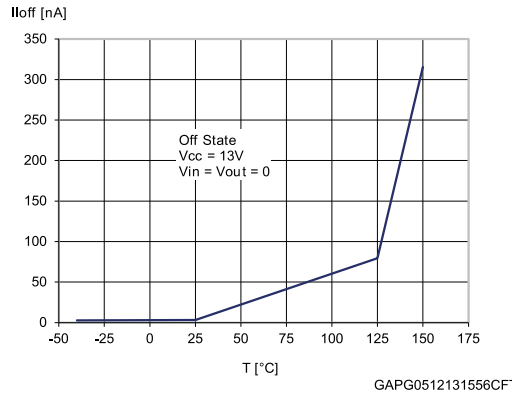


Figure 13: Standby current

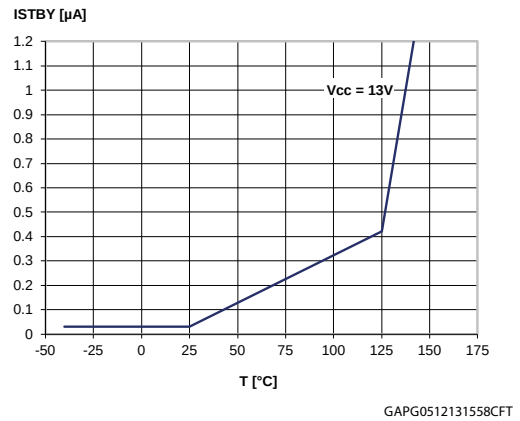


Figure 14: IGND(ON) vs Tcase

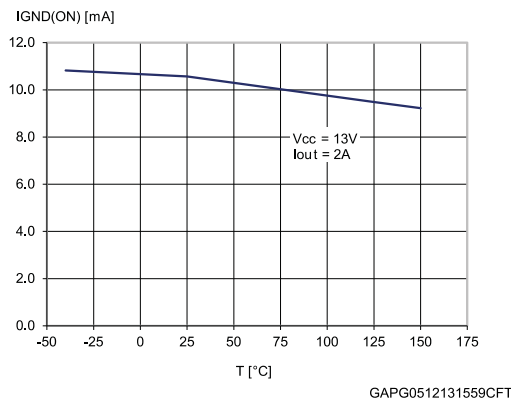


Figure 15: Logic Input high level voltage

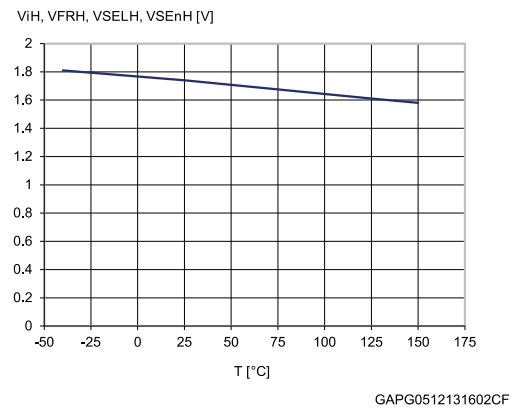


Figure 16: Logic Input low level voltage

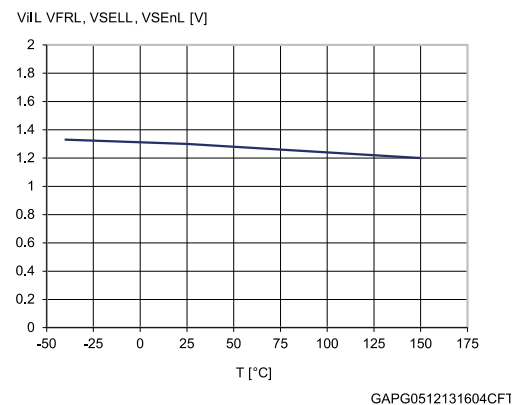


Figure 17: High level logic input current

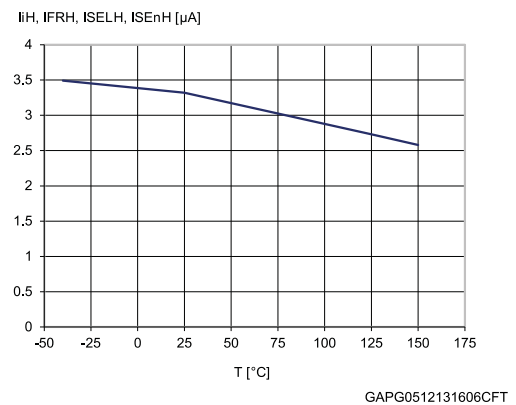


Figure 18: Low level logic input current

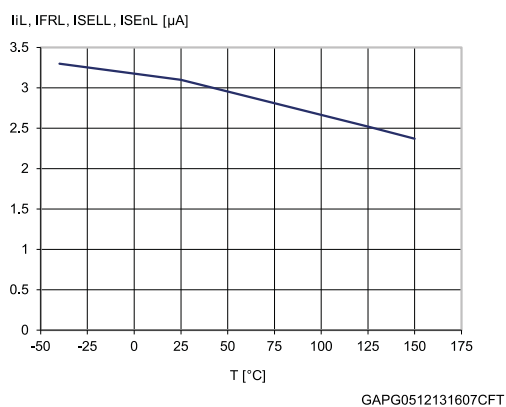


Figure 19: Logic Input hysteresis voltage

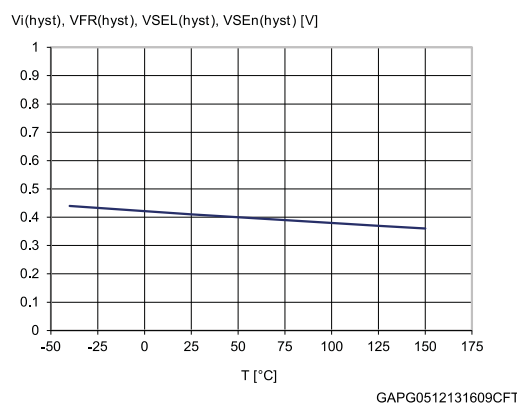


Figure 20: FaultRST Input clamp voltage

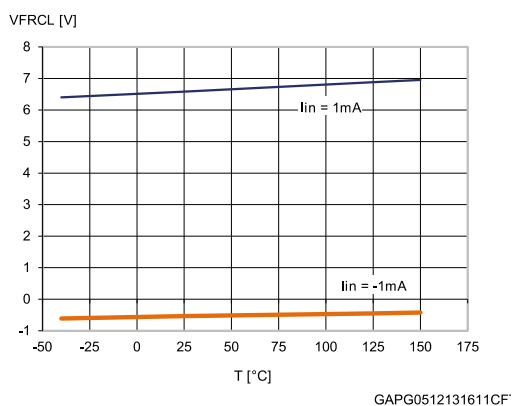


Figure 21: Undervoltage shutdown

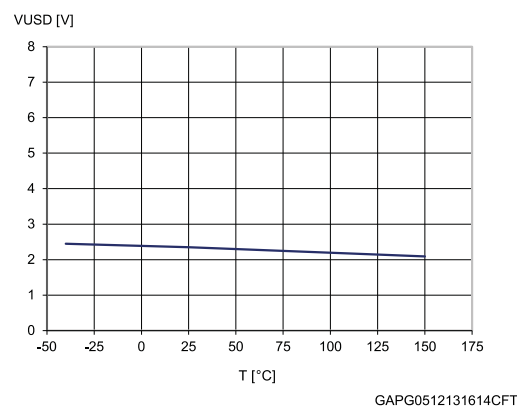


Figure 22: On-state resistance vs Tcase

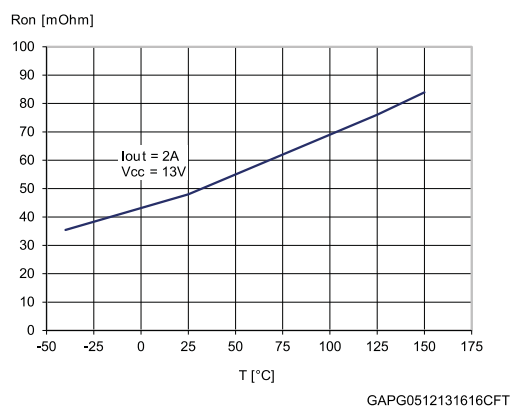


Figure 23: On-state resistance vs VCC

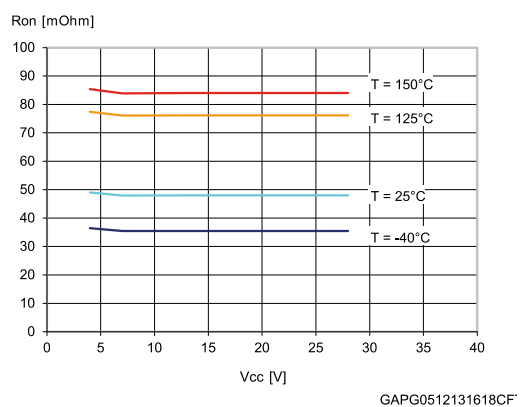


Figure 24: Turn-on voltage slope

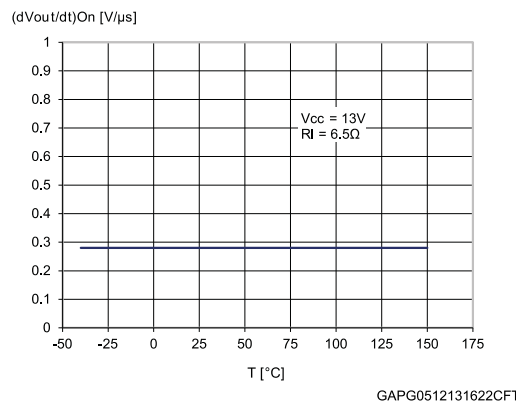


Figure 25: Turn-off voltage slope

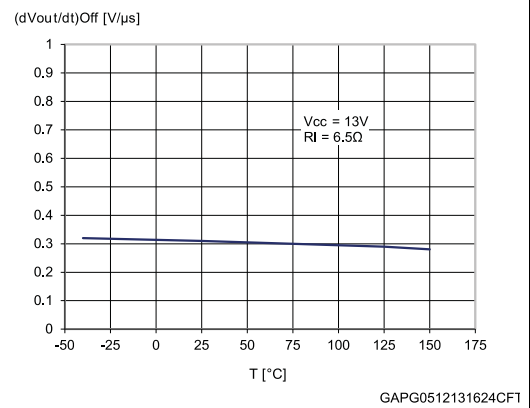


Figure 26: Won vs Tcase

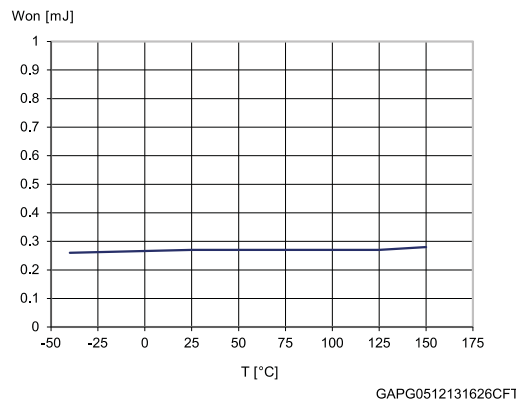


Figure 27: Woff vs Tcase

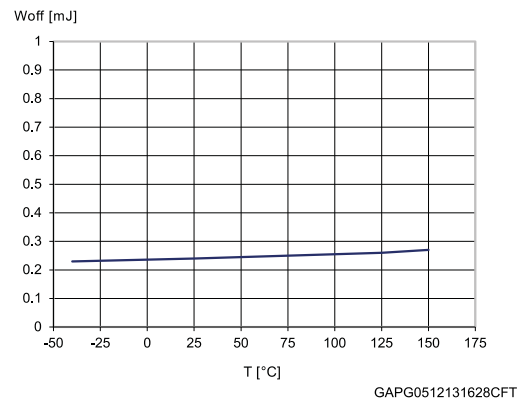


Figure 28: ILIMH vs. Tcase

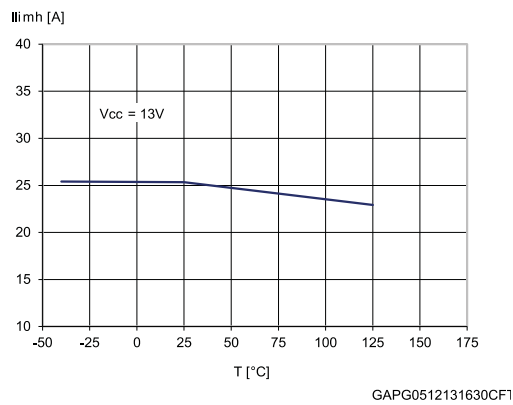


Figure 29: OFF-state open-load voltage detection threshold

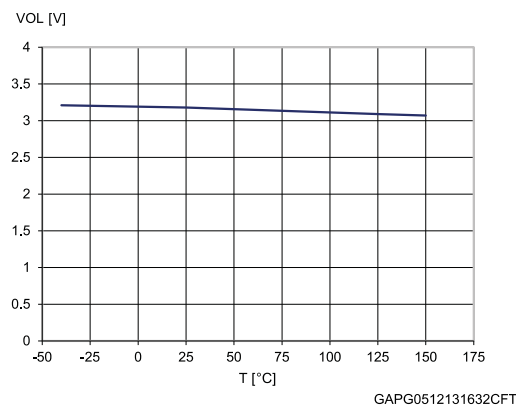


Figure 30: Vsense clamp vs. Tcase

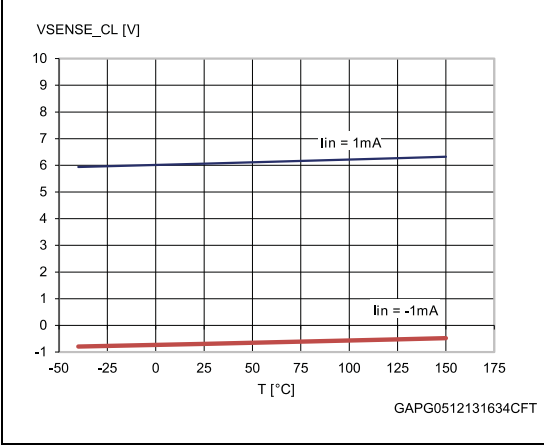
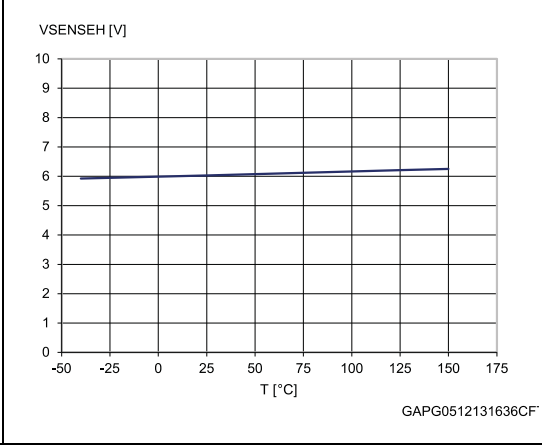


Figure 31: Vsenseh vs. Tcase



## 3 Protections

### 3.1 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing  $\Delta T_j$  through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as  $\Delta T_j$  exceeds the safety level of  $\Delta T_{j\_SD}$ . According to the voltage level on the FaultRST pin, the output MOSFET switches on and cycles with a thermal hysteresis according to the maximum instantaneous power which can be handled (FaultRST = Low) or remains off (FaultRST = High). The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

### 3.2 Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175°C), it automatically switches off and the diagnostic indication is triggered. According to the voltage level on the FaultRST pin, the device switches on again as soon as its junction temperature drops to  $T_R$  (FaultRST = Low) or remains off (FaultRST = High).

### 3.3 Current limitation

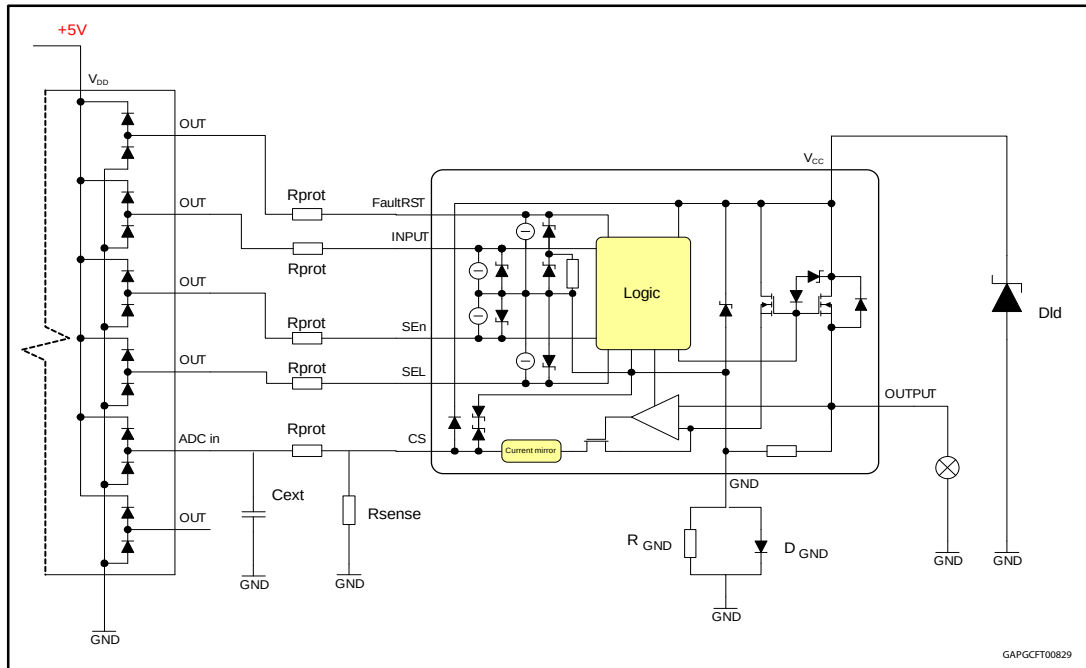
The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short circuit, overload or during load power-up, the output current is clamped to a safety level,  $I_{LIMH}$ , by operating the output power MOSFET in the active region.

### 3.4 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches a negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value,  $V_{DEMG}$ , allowing the inductor energy to be dissipated without damaging the device.

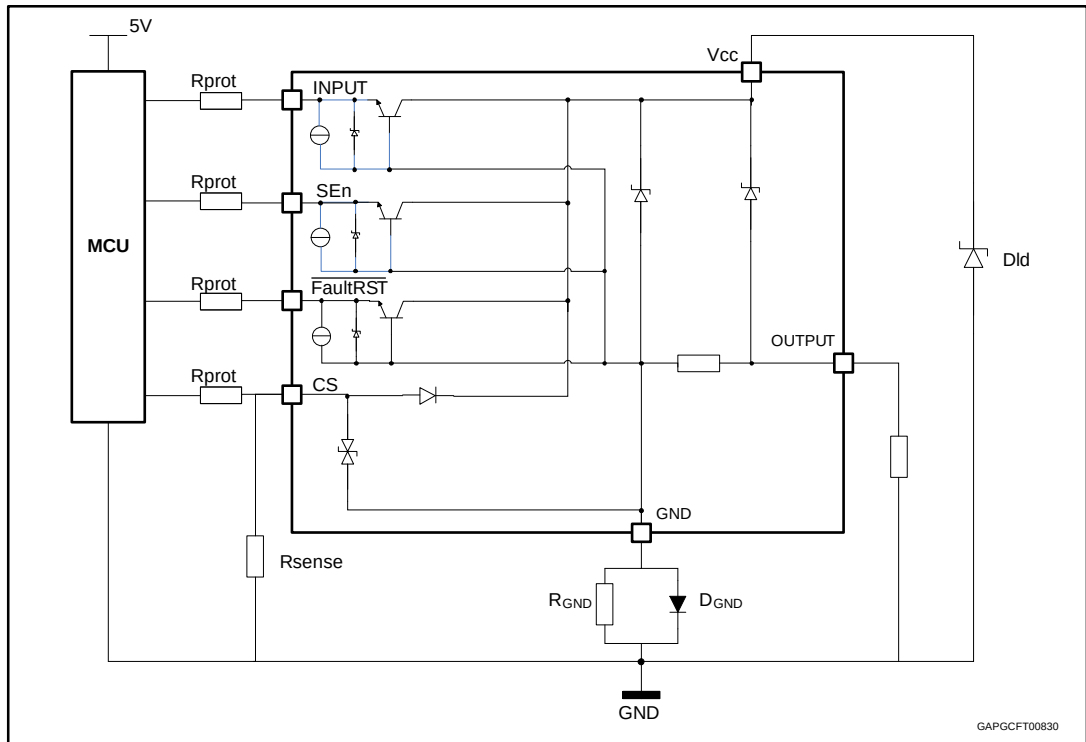
## 4 Application information

Figure 32: Application diagram



### 4.1 GND protection network against reverse battery

Figure 33: Simplified internal structure



### 4.1.1 Diode (DGND) in the ground line

A resistor (typ.  $R_{\text{GND}} = 4.7 \text{ k}\Omega$ ) should be inserted in parallel to  $D_{\text{GND}}$  if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift ( $\approx 600 \text{ mV}$ ) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

## 4.2 Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the  $V_{\text{CC}}$  pin, is tested in accordance with ISO 7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in [Table 12: "ISO 7637-2 - electrical transient conduction along supply line"](#).

Test pulses are applied directly to DUT (Device Under Test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4. The DUT is intended as the present device only, without components and accessed through  $V_{\text{CC}}$  and GND terminals.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: "The function does not perform as designed during the test but returns automatically to normal operation after the test".

**Table 12: ISO 7637-2 - electrical transient conduction along supply line**

| Test Pulse 2011(E)                             | Test pulse severity level with Status II functional performance status |             | Minimum number of pulses or test time | Burst cycle / pulse repetition time |        | Pulse duration and pulse generator internal impedance |
|------------------------------------------------|------------------------------------------------------------------------|-------------|---------------------------------------|-------------------------------------|--------|-------------------------------------------------------|
|                                                | Level                                                                  | $U_s^{(1)}$ |                                       | min                                 | max    |                                                       |
| 1                                              | III                                                                    | -112V       | 500 pulses                            | 0,5 s                               |        | 2ms, 10 $\Omega$                                      |
| 2a                                             | III                                                                    | +55V        | 500 pulses                            | 0,2 s                               | 5 s    | 50 $\mu$ s, 2 $\Omega$                                |
| 3a                                             | IV                                                                     | -220V       | 1h                                    | 90 ms                               | 100 ms | 0.1 $\mu$ s, 50 $\Omega$                              |
| 3b                                             | IV                                                                     | +150V       | 1h                                    | 90 ms                               | 100 ms | 0.1 $\mu$ s, 50 $\Omega$                              |
| 4 <sup>(2)</sup>                               | IV                                                                     | -7V         | 1 pulse                               |                                     |        | 100ms, 0.01 $\Omega$                                  |
| <b>Load dump according to ISO 16750-2:2010</b> |                                                                        |             |                                       |                                     |        |                                                       |
| Test B <sup>(3)</sup>                          |                                                                        | 40V         | 5 pulse                               | 1 min                               |        | 400ms, 2 $\Omega$                                     |

**Notes:**

<sup>(1)</sup> $U_s$  is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.

<sup>(2)</sup>Test pulse from ISO 7637-2:2004(E).

<sup>(3)</sup>With 40 V external suppressor referred to ground ( $-40^\circ\text{C} < T_j < 150^\circ\text{C}$ ).

## 4.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the  $V_{\text{CC}}$  line, the control pins will be pulled negative. ST suggests to insert a resistor ( $R_{\text{prot}}$ ) in line both to prevent the microcontroller I/O pins to latch-up and to protect the HSD inputs.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

### Equation

$$V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For  $V_{CCpeak} = -150 \text{ V}$ ;  $I_{latchup} \geq 20 \text{ mA}$ ;  $V_{OH\mu C} \geq 4.5 \text{ V}$

$$7.5 \text{ k}\Omega \leq R_{prot} \leq 140 \text{ k}\Omega.$$

Recommended values:  $R_{prot} = 15 \text{ k}\Omega$

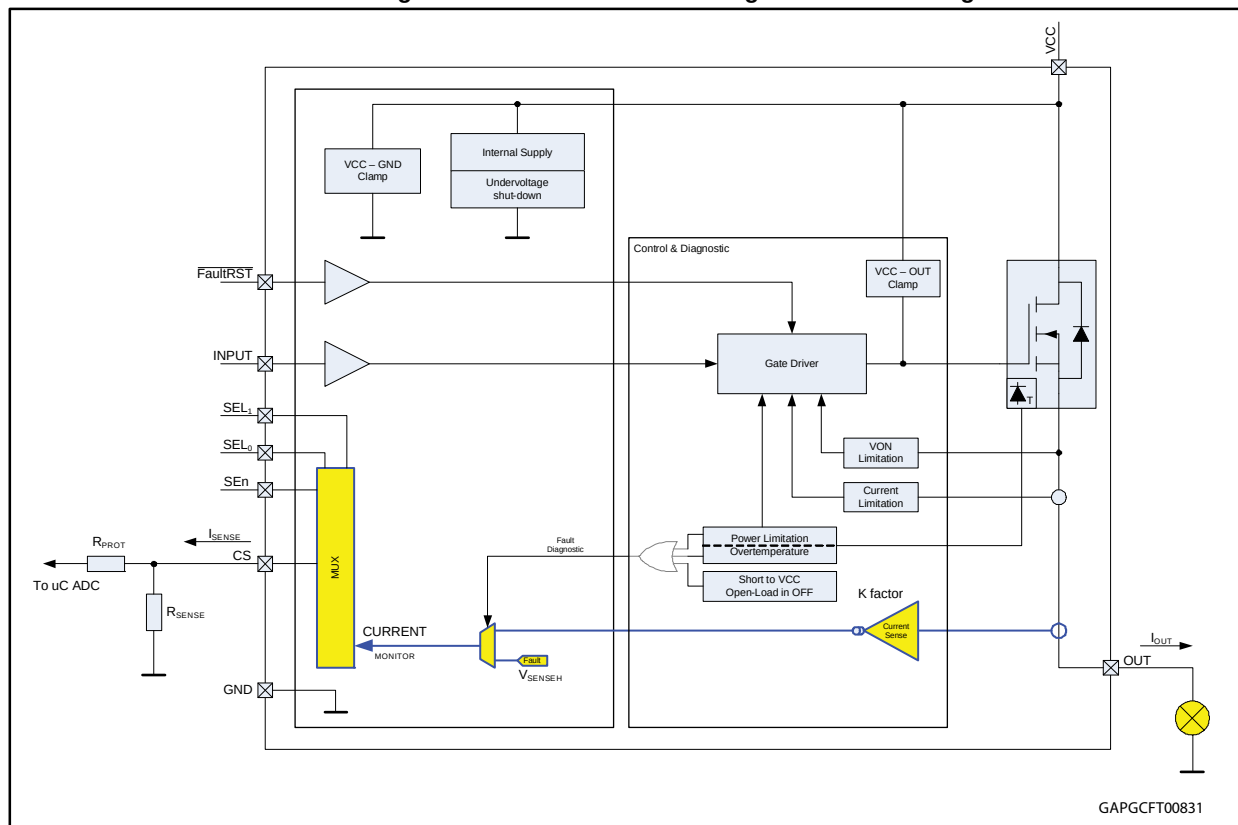
## 4.4 CS - analog current sense

Diagnostic information on device and load status are provided by an analog output pin (CS) delivering the following signals:

- Current monitor: current mirror of channel output current

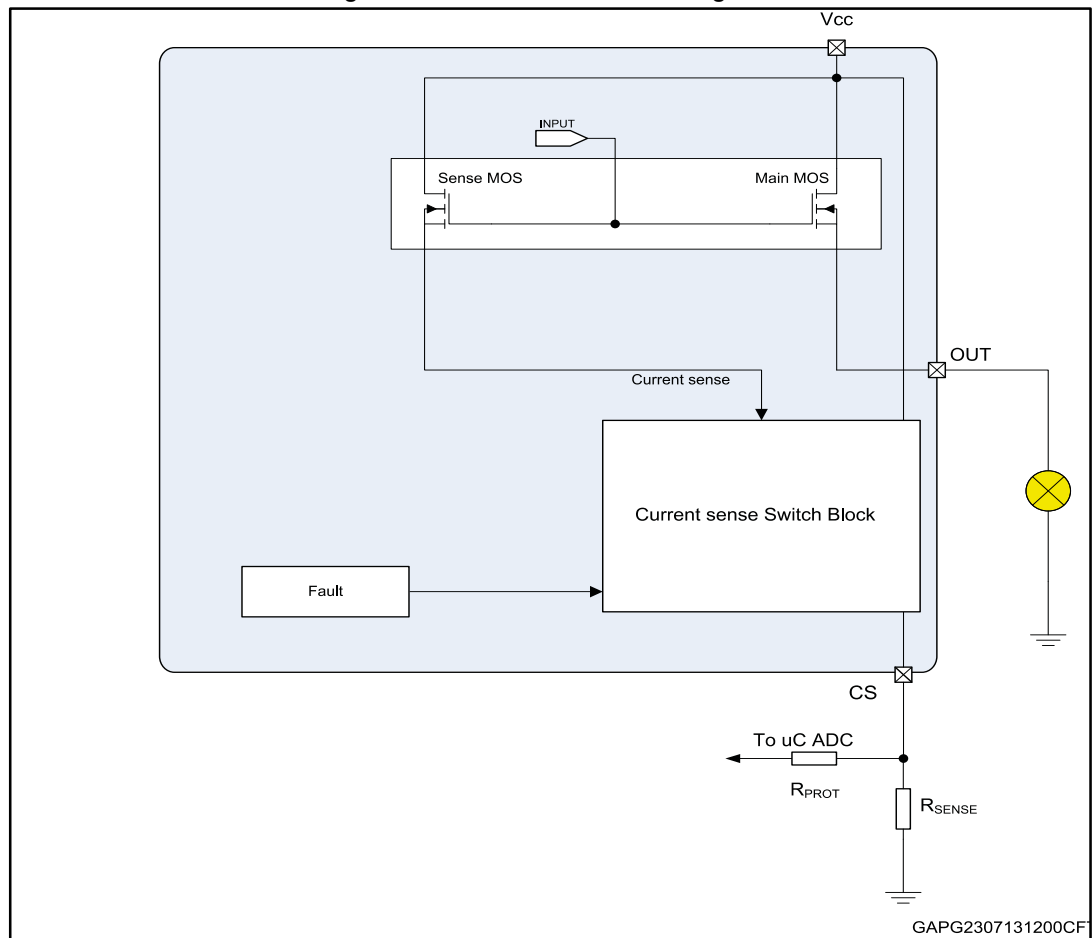
Those signals are routed through an analog multiplexer which is configured and controlled by means of SELx and SEn pins, according to the address map in *MultiSense multiplexer addressing Table*.

Figure 34: CurrentSense and diagnostic – block diagram



#### 4.4.1 Principle of CurrentSense signal generation

Figure 35: CurrentSense block diagram



##### Current sense

This current mode is selected in the MultiSense, this output is capable to provide:

- Current mirror proportional to the load current in normal operation, delivering current proportional to the load according to known ratio named **K**
- Diagnostics flag in fault conditions delivering fixed voltage  $V_{SENSEH}$

The current delivered by the current sense circuit,  $I_{SENSE}$ , can be easily converted to a voltage  $V_{SENSE}$  by using an external sense resistor,  $R_{SENSE}$ , allowing continuous load monitoring and abnormal condition detection.

##### Normal operation (channel ON, no fault, SEn active)

While device is operating in normal conditions (no fault intervention),  $V_{SENSE}$  calculation can be done using simple equations

Current provided by CS output:  $I_{SENSE} = I_{OUT}/K$

Voltage on  $R_{SENSE}$ :  $V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \cdot I_{OUT}/K$

Where:

- $V_{SENSE}$  is voltage measurable on  $R_{SENSE}$  resistor
- $I_{SENSE}$  is current provided from CS pin in current output mode

- $I_{OUT}$  is current flowing through output
- K factor represents the ratio between PowerMOS cells and SenseMOS cells; its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of the overall circuitry the specifying ratio between  $I_{OUT}$  and  $I_{SENSE}$ .

### Failure flag indication

In case of power limitation/overtemperature, the fault is indicated by the CS pin which is switched to a “current limited” voltage source,  $V_{SENSEH}$ .

In any case, the current sourced by the CS in this condition is limited to  $I_{SENSEH}$ .

The typical behavior in case of overload or hard short circuit is shown in *Waveforms* section.

Figure 36: Analogue HSD – open-load detection in off-state

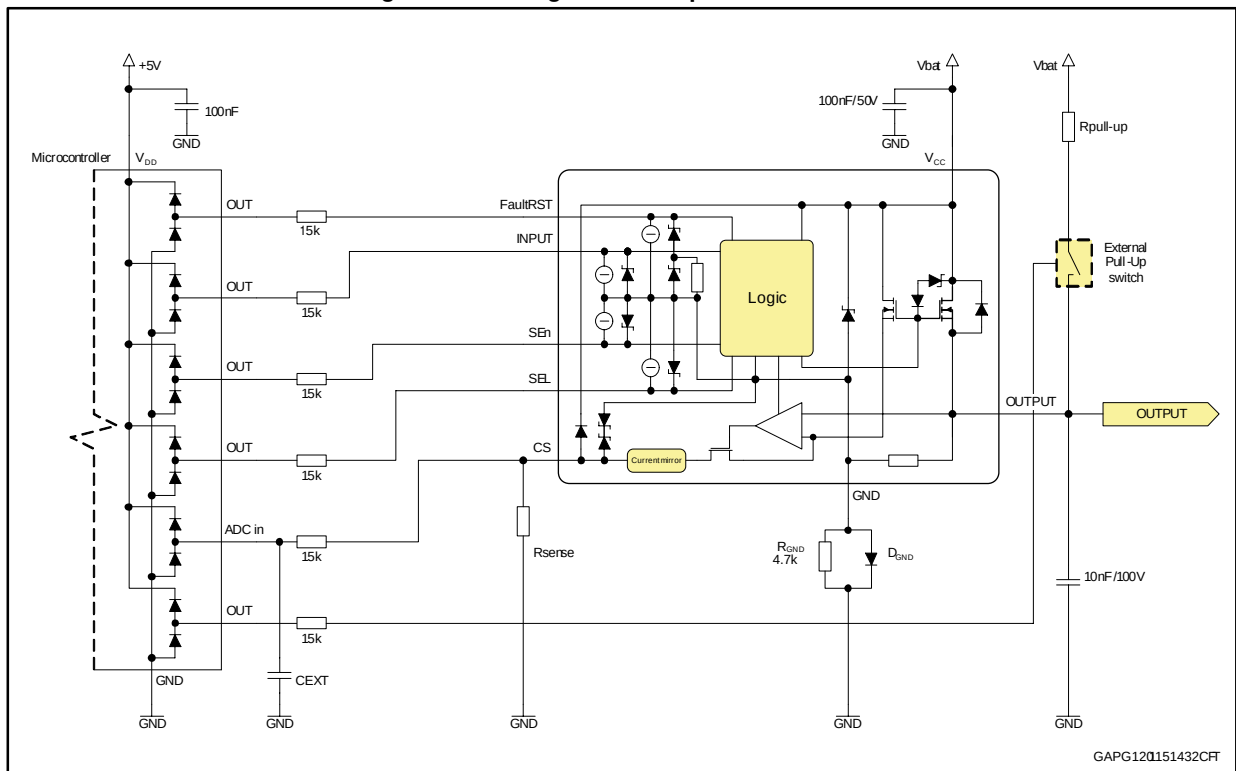


Figure 37: Open-load / short to VCC condition

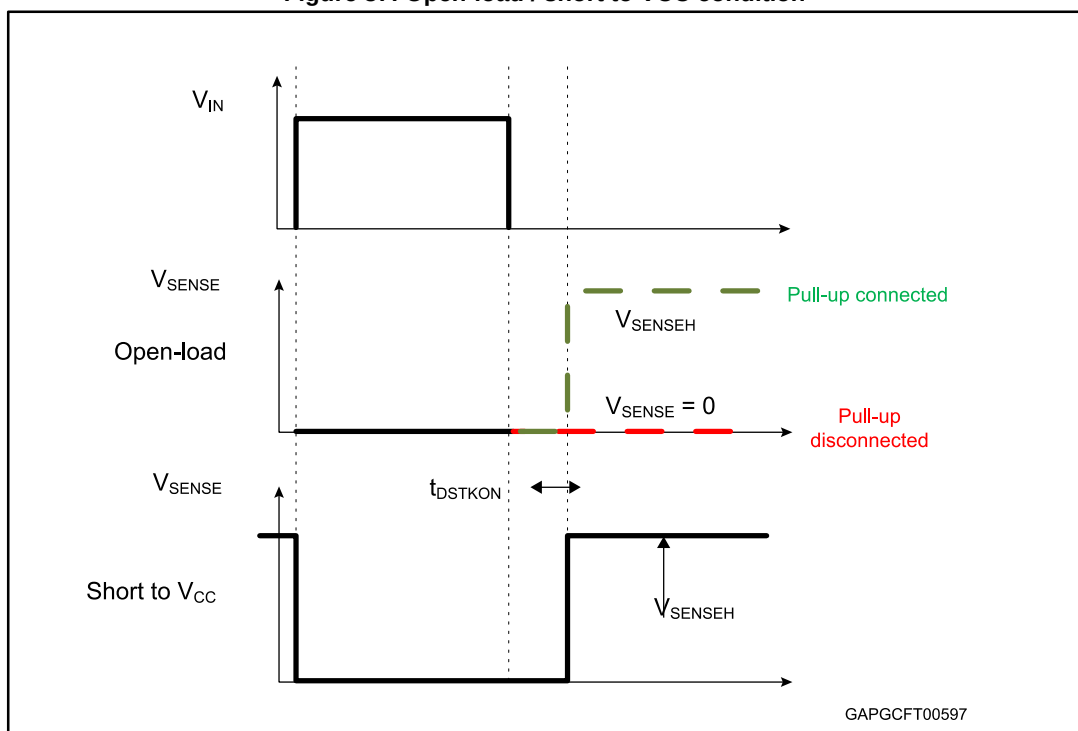


Table 13: CurrentSense pin levels in off-state

| Condition         | Output             | CS           | SEn |
|-------------------|--------------------|--------------|-----|
| Open-load         | $V_{OUT} > V_{OL}$ | Hi-Z         | L   |
|                   |                    | $V_{SENSEH}$ | H   |
|                   | $V_{OUT} < V_{OL}$ | Hi-Z         | L   |
|                   |                    | 0            | H   |
| Short to $V_{CC}$ | $V_{OUT} > V_{OL}$ | Hi-Z         | L   |
|                   |                    | $V_{SENSEH}$ | H   |
| Nominal           | $V_{OUT} < V_{OL}$ | Hi-Z         | L   |
|                   |                    | 0            | H   |

#### 4.4.2 Short to VCC and OFF-state open-load detection

##### Short to $V_{CC}$

A short circuit between  $V_{CC}$  and output is indicated by the relevant current sense pin set to  $V_{SENSEH}$  during the device off-state. Small or no current is delivered by the current sense during the on-state depending on the nature of the short circuit.

##### OFF-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor  $R_{PU}$  connecting the output to a positive supply voltage  $V_{PU}$ .

It is preferable  $V_{PU}$  to be switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

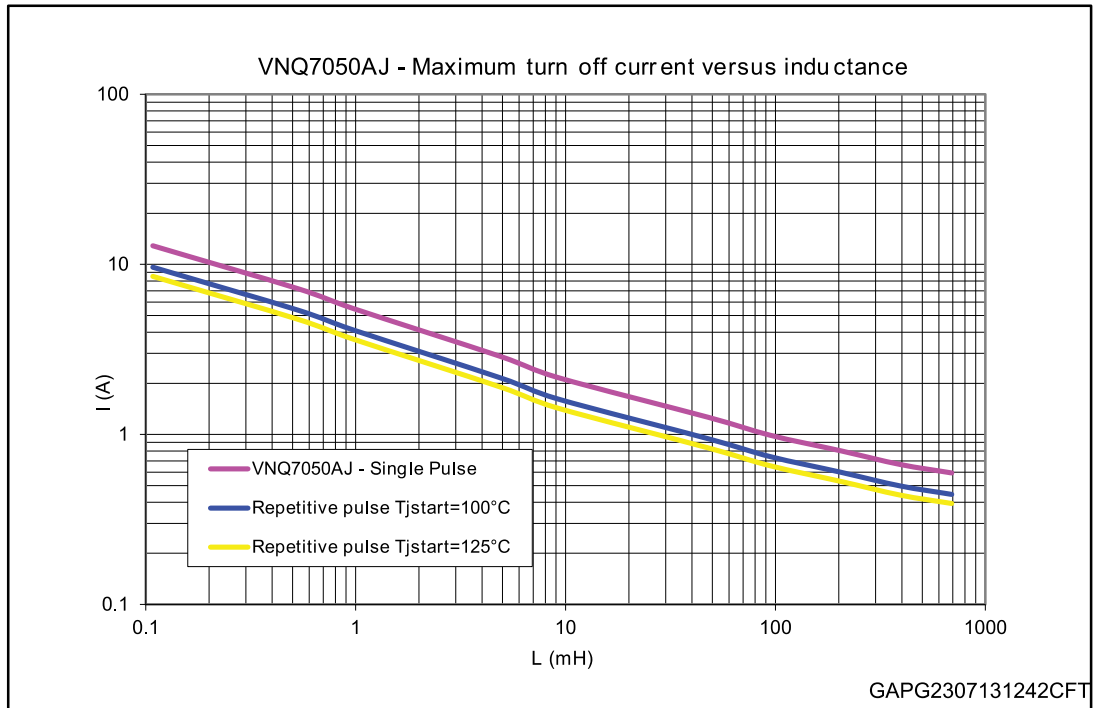
$R_{PU}$  must be selected in order to ensure  $V_{OUT} > V_{OLmax}$  in accordance with the following equation:

**Equation**

$$R_{PU} < \frac{V_{PU} - 4}{I_{L(off2)min @ 4V}}$$

## 5 Maximum demagnetization energy (VCC = 16 V)

Figure 38: Maximum turn off current versus inductance



Values are generated with  $R_L = 0 \Omega$ .

In case of repetitive pulses,  $T_{jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

## 6 Package and PCB thermal data

### 6.1 PowerSSO-16 thermal data

Figure 39: PowerSSO-16 on two-layers PCB (2s0p to JEDEC JESD 51-5)

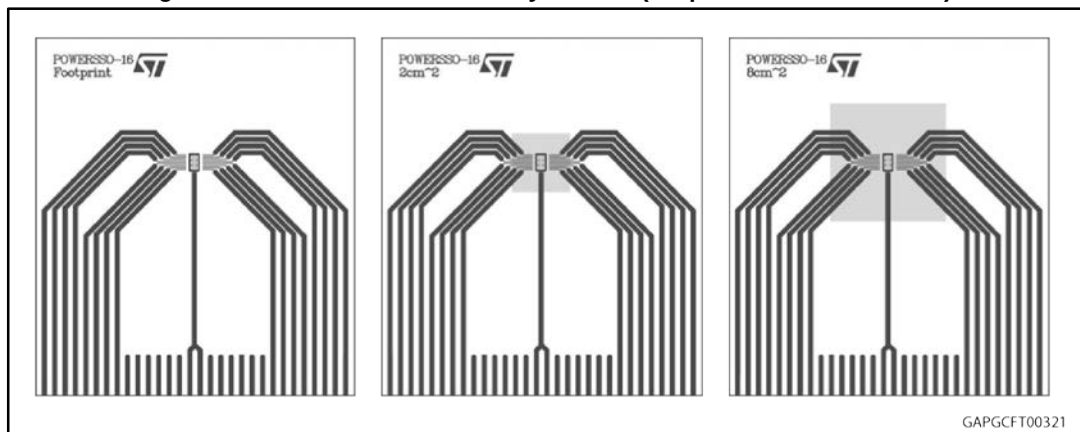


Figure 40: PowerSSO-16 on four-layers PCB (2s2p to JEDEC JESD 51-7)

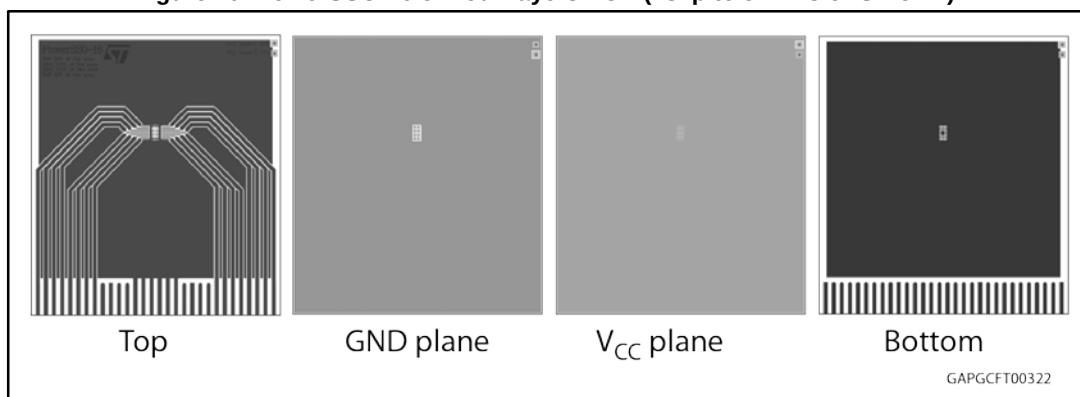


Table 14: PCB properties

| Dimension                                     | Value                                             |
|-----------------------------------------------|---------------------------------------------------|
| Board finish thickness                        | 1.6 mm +/- 10%                                    |
| Board dimension                               | 77 mm x 86 mm                                     |
| Board Material                                | FR4                                               |
| Copper thickness (top and bottom layers)      | 0.070 mm                                          |
| Copper thickness (inner layers)               | 0.035 mm                                          |
| Thermal vias separation                       | 1.2 mm                                            |
| Thermal via diameter                          | 0.3 mm +/- 0.08 mm                                |
| Copper thickness on vias                      | 0.025 mm                                          |
| Footprint dimension (top layer)               | 2.2 mm x 3.9 mm                                   |
| Heatsink copper area dimension (bottom layer) | Footprint, 2 cm <sup>2</sup> or 8 cm <sup>2</sup> |

Figure 41: Rthj-amb vs PCB copper area in open box free air condition (one channel on)

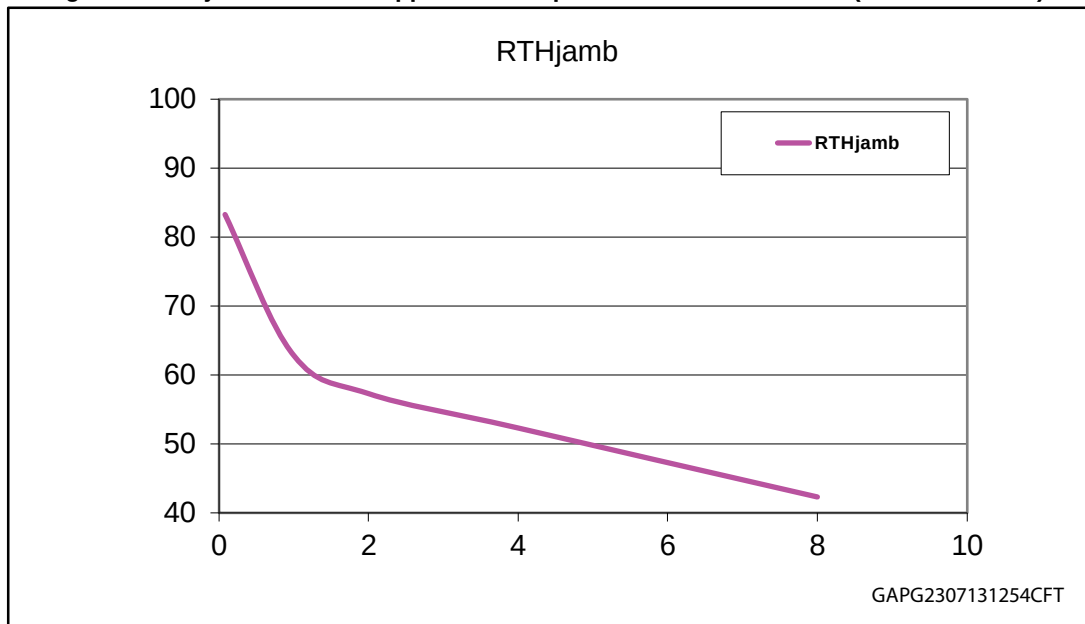
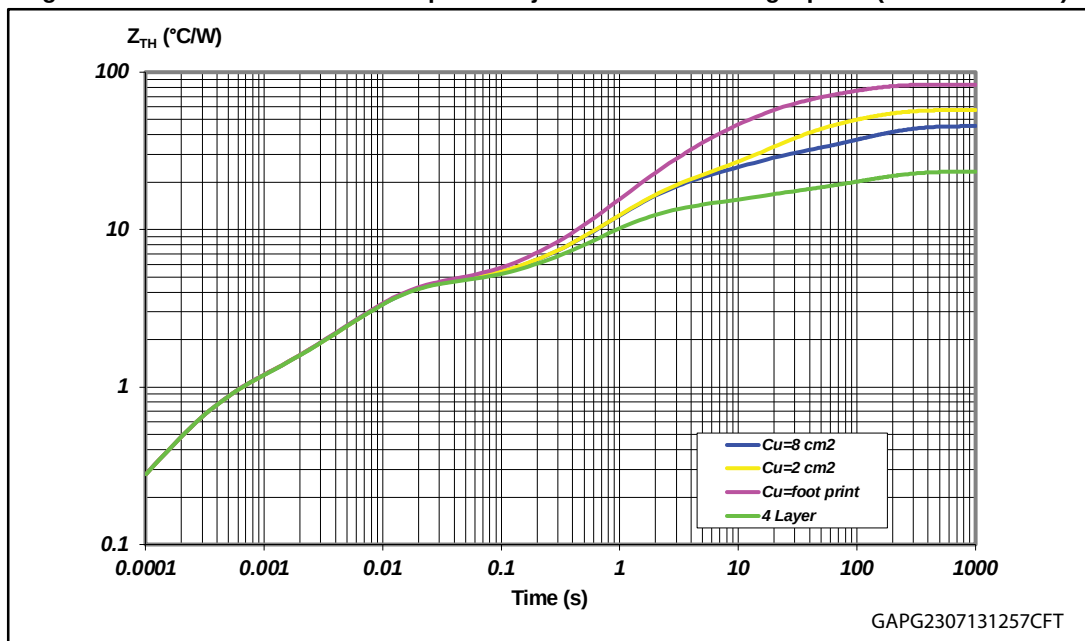


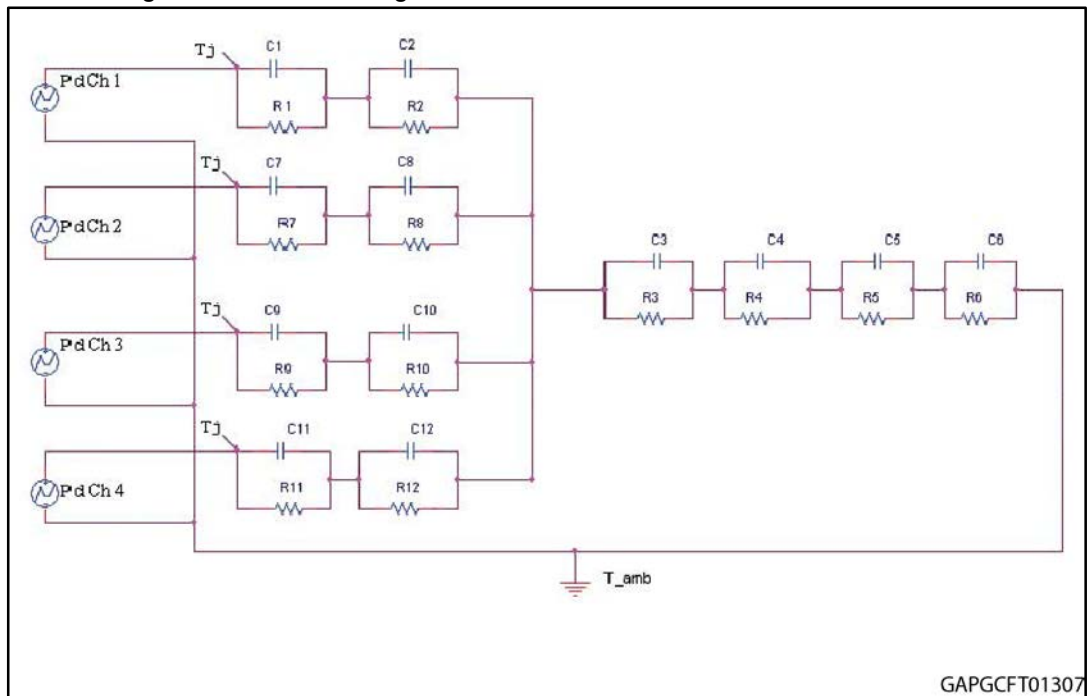
Figure 42: PowerSSO-16 thermal impedance junction ambient single pulse (one channel on)

**Equation: pulse calculation formula**

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp} (1 - \delta)$$

where  $\delta = t_p/T$

Figure 43: Thermal fitting model of a double-channel HSD in PowerSSO-16



The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 15: Thermal parameters

| Area/island (cm <sup>2</sup> ) | Footprint | 2   | 8   |     |
|--------------------------------|-----------|-----|-----|-----|
| R1 = R7 = R9 = R11 (°C/W)      | 0.8       |     |     |     |
| R2 = R8 = R10 = R12 (°C/W)     | 3.5       |     |     |     |
| R3 (°C/W)                      | 7         | 7   | 7   | 7   |
| R4 (°C/W)                      | 16        | 6   | 6   | 4   |
| R5 (°C/W)                      | 30        | 20  | 10  | 3   |
| R6 (°C/W)                      | 26        | 20  | 18  | 7   |
| C1 = C7 = C9 = C11 (W.s/°C)    | 0.00035   |     |     |     |
| C2 = C8 = C10 = C12 (W.s/°C)   | 0.0023    |     |     |     |
| C3 (W.s/°C)                    | 0.14      |     |     |     |
| C4 (W.s/°C)                    | 0.2       | 0.3 | 0.3 | 0.4 |
| C5 (W.s/°C)                    | 0.4       | 1   | 1   | 4   |
| C6 (W.s/°C)                    | 3         | 5   | 7   | 18  |

## 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 7.1 PowerSSO-16 package information

Figure 44: PowerSSO-16 package dimensions

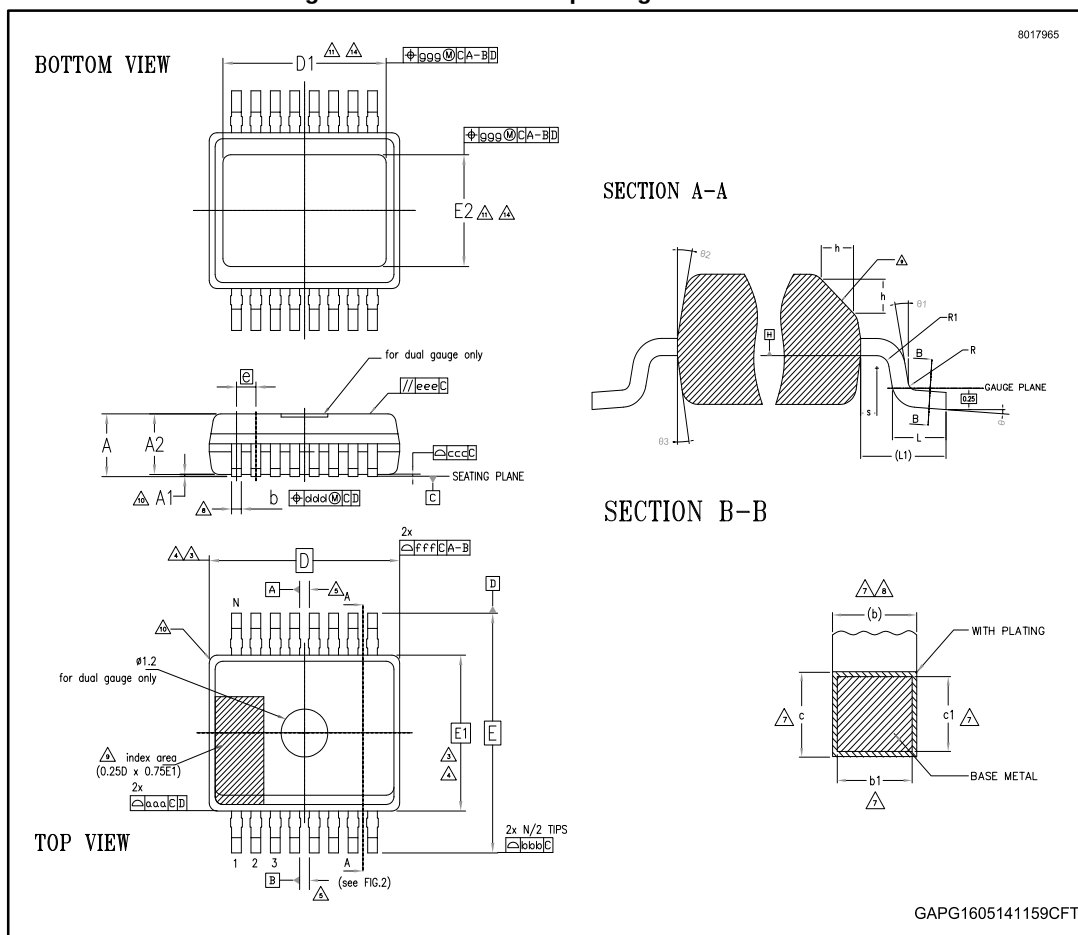


Table 16: PowerSSO-16 mechanical data

| Symbol     | Millimeters |      |      |
|------------|-------------|------|------|
|            | Min.        | Typ. | Max. |
| $\Theta$   | 0°          |      | 8°   |
| $\Theta 1$ | 0°          |      |      |
| $\Theta 2$ | 5°          |      | 15°  |
| $\Theta 3$ | 5°          |      | 15°  |
| A          |             |      | 1.70 |
| A1         | 0.00        |      | 0.10 |
| A2         | 1.10        |      | 1.60 |

| Symbol                         | Millimeters |      |      |
|--------------------------------|-------------|------|------|
|                                | Min.        | Typ. | Max. |
| b                              | 0.20        |      | 0.30 |
| b1                             | 0.20        | 0.25 | 0.28 |
| c                              | 0.19        |      | 0.25 |
| c1                             | 0.19        | 0.20 | 0.23 |
| D                              | 4.9 BSC     |      |      |
| D1                             | 3.60        |      | 4.20 |
| e                              | 0.50 BSC    |      |      |
| E                              | 6.00 BSC    |      |      |
| E1                             | 3.90 BSC    |      |      |
| E2                             | 1.90        |      | 2.50 |
| h                              | 0.25        |      | 0.50 |
| L                              | 0.40        | 0.60 | 0.85 |
| L1                             | 1.00 REF    |      |      |
| N                              | 16          |      |      |
| R                              | 0.07        |      |      |
| R1                             | 0.07        |      |      |
| S                              | 0.20        |      |      |
| Tolerance of form and position |             |      |      |
| aaa                            | 0.10        |      |      |
| bbb                            | 0.10        |      |      |
| ccc                            | 0.08        |      |      |
| ddd                            | 0.08        |      |      |
| eee                            | 0.10        |      |      |
| fff                            | 0.10        |      |      |
| ggg                            | 0.15        |      |      |

## 7.2 PowerSSO-16 packing information

Figure 45: PowerSSO-16 reel 13"

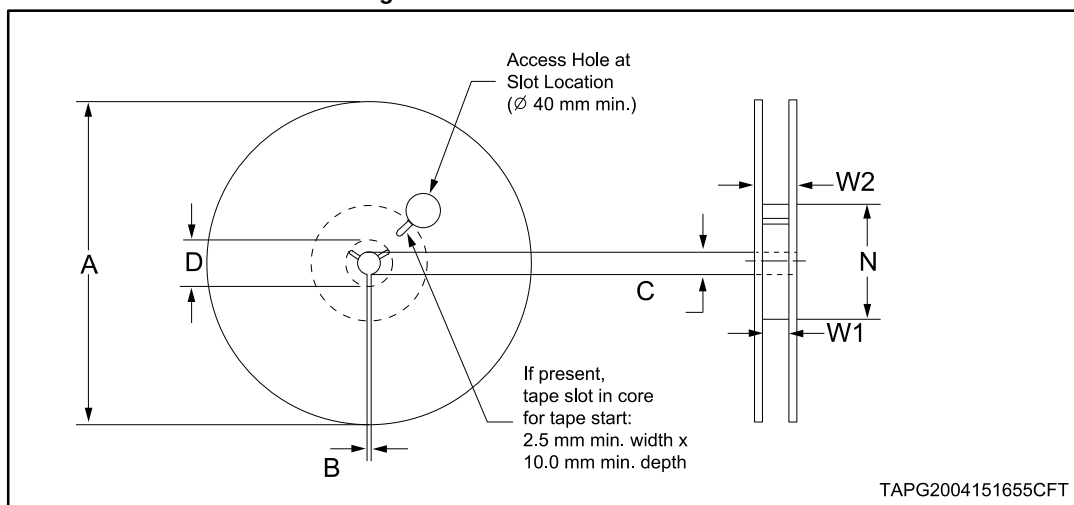


Table 17: Reel dimensions

| Description    | Value <sup>(1)</sup> |
|----------------|----------------------|
| Base quantity  | 2500                 |
| Bulk quantity  | 2500                 |
| A (max)        | 330                  |
| B (min)        | 1.5                  |
| C (+0.5, -0.2) | 13                   |
| D (min)        | 20.2                 |
| N              | 100                  |
| W1 (+2 /-0)    | 12.4                 |
| W2 (max)       | 18.4                 |

**Notes:**

<sup>(1)</sup>All dimensions are in mm.

Figure 46: PowerSSO-16 carrier tape

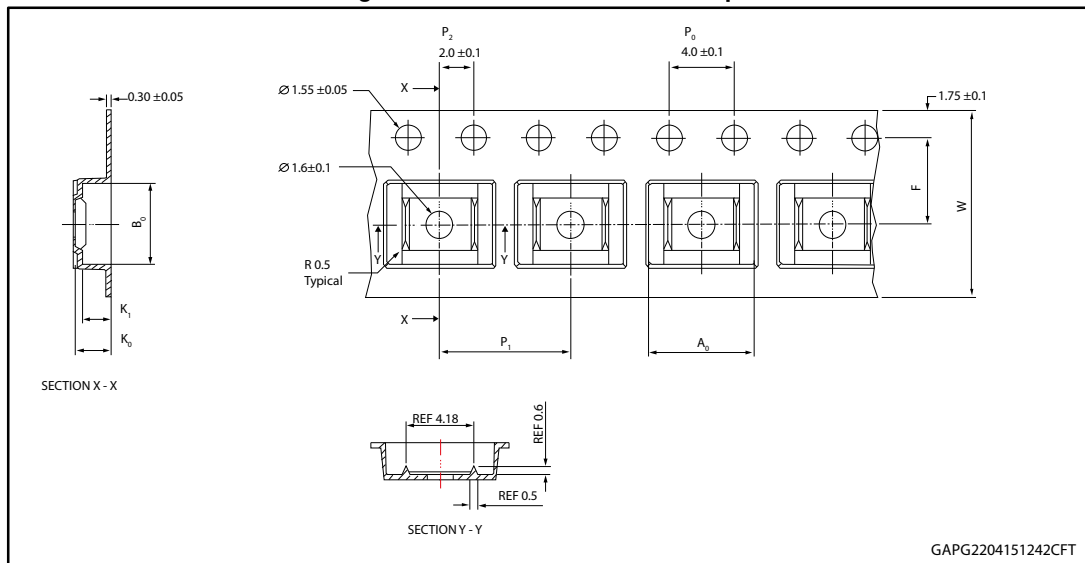


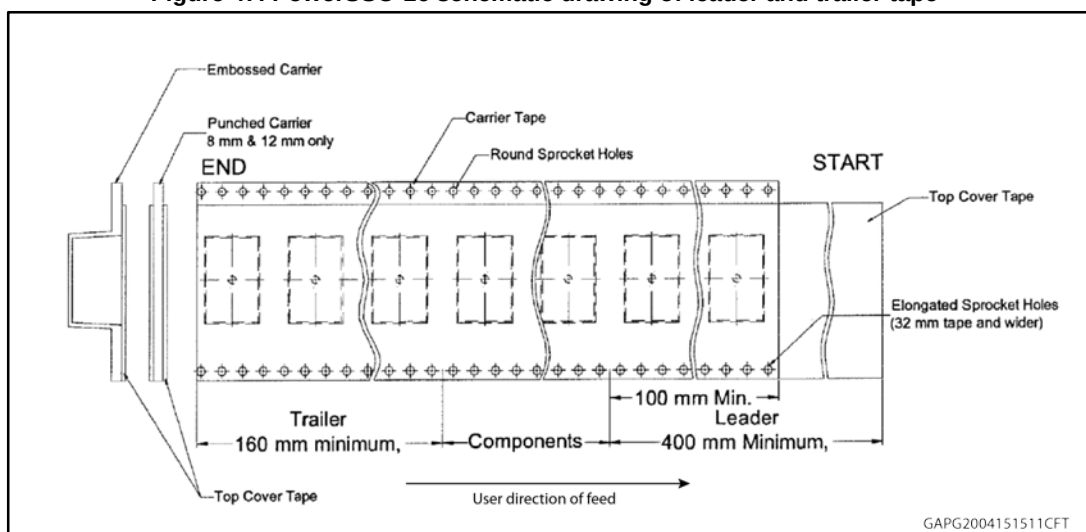
Table 18: PowerSSO-16 carrier tape dimensions

| Description    | Value <sup>(1)</sup> |
|----------------|----------------------|
| A <sub>0</sub> | 6.50 ± 0.1           |
| B <sub>0</sub> | 5.25 ± 0.1           |
| K <sub>0</sub> | 2.10 ± 0.1           |
| K <sub>1</sub> | 1.80 ± 0.1           |
| F              | 5.50 ± 0.1           |
| P <sub>1</sub> | 8.00 ± 0.1           |
| W              | 12.00 ± 0.3          |

**Notes:**

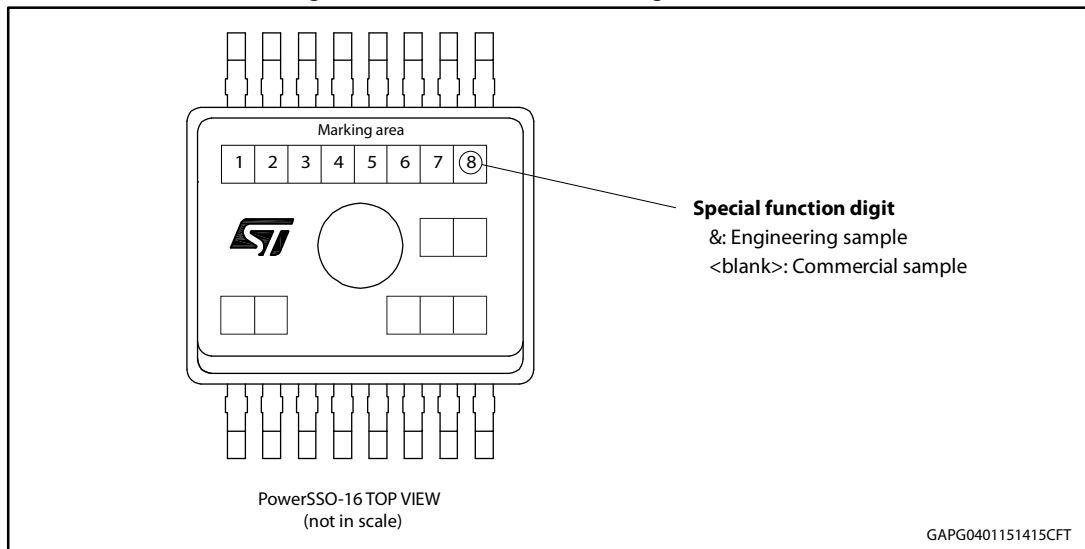
<sup>(1)</sup>All dimensions are in mm.

Figure 47: PowerSSO-16 schematic drawing of leader and trailer tape



### 7.3 PowerSSO-16 marking information

Figure 48: PowerSSO-16 marking information



**Engineering Samples:** these samples can be clearly identified by a dedicated special symbol in the marking of each unit. These samples are intended to be used for electrical compatibility evaluation only; usage for any other purpose may be agreed only upon written authorization by ST. ST is not liable for any customer usage in production and/or in reliability qualification trials.

**Commercial Samples:** fully qualified parts from ST standard production with no usage restrictions.

## 8 Order codes

Table 19: Device summary

| Package     | Order codes   |
|-------------|---------------|
|             | Tape and reel |
| PowerSSO-16 | VNQ7050AJTR   |

## 9 Revision history

Table 20: Document revision history

| Date        | Revision | Changes          |
|-------------|----------|------------------|
| 04-Jun-2015 | 1        | Initial release. |

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