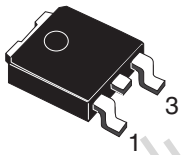
STD35NF3LL

N-channel 30V - 0.014Ω - 35A - DPAK
STripFET™ II Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STD35NF3LL	30V	<0.0195Ω	35A

- Optimal $R_{DS}(on)$ x Q_g trade-off @ 4.5V
- Conduction losses reduced
- Switching losses reduced
- Low threshold drive

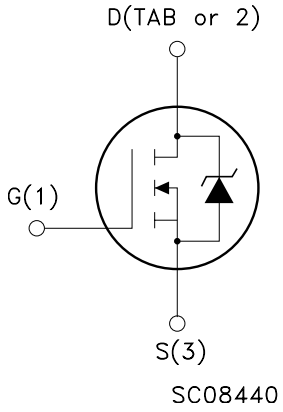


DPAK

Description

This application specific Power MOSFET is the third generation of STMicroelectronics unique "single feature size™" strip-based process. The resulting transistor shows the best trade-off between on-resistance and gate charge. When used as high and low side in buck regulators, it gives the best performance in terms of both conduction and switching losses. This is extremely important for motherboards where fast switching and high efficiency are of paramount importance. remarkable manufacturing reproducibility.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STD35NF3LLT4	D35NF3LL	DPAK	Tape & reel

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	30	V
V_{GS}	Gate- source voltage	± 16	V
I_D	Drain current (continuous) at T_C = 25°C	35	A
I_D	Drain current (continuous) at T_C = 100°C	25	A
I_{DM} (1)	Drain current (pulsed)	140	A
P_{tot}	Total dissipation at T_C = 25°C	50	W
	Derating factor	0.33	W/°C
E_{AS} (2)	Single pulse avalanche energy	300	mJ
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Max. operating junction temperature		

1. Pulse width limited by safe operating area.
2. Starting T_j = 25 °C, I_D = 17.5A, V_{DD} =24V

Table 2. Thermal data

Rthj-case	Thermal resistance junction-case max	3	°C/W
Rthj-amb	Thermal resistance junction-to ambient max	100	°C/W
T_J	Maximum lead temperature for soldering purpose	300	°C

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250µA, V_{GS} =0	30			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0) V_{DS} = Max rating V_{DS} = Max rating @125°C				1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 16V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	1		2.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 17.5A V_{GS} = 4.5V, I_D = 17.5A		0.014 0.016	0.0195 0.0215	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15V, I_D = 17.5A		19		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V, f = 1MHz, V_{GS} = 0		800 250 60		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 15V, I_D = 17.5A R_G = 4.7Ω V_{GS} = 4.5V (see *Figure 12*)		17 100 20 21		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 24V, I_D = 35A, V_{GS} = 5V, R_G = 4.7Ω (see *Figure 13*)		12.5 42 5.2	17	nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%.

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				35 140	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 35A, V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 35A, di/dt = 100A/µs, V_{DD} = 15V, T_j = 150°C (see *Figure 17*)		35 44 2.5		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

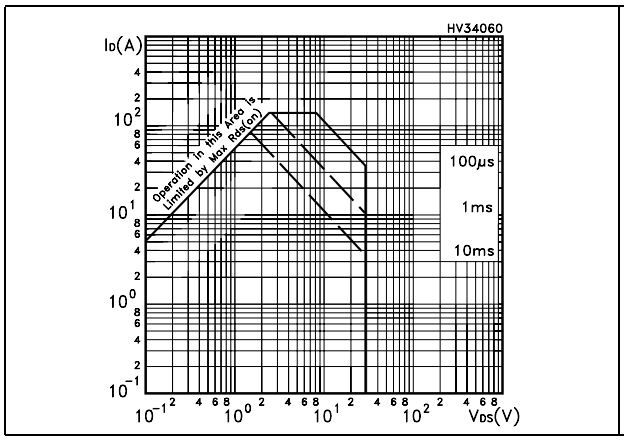


Figure 2. Thermal impedance

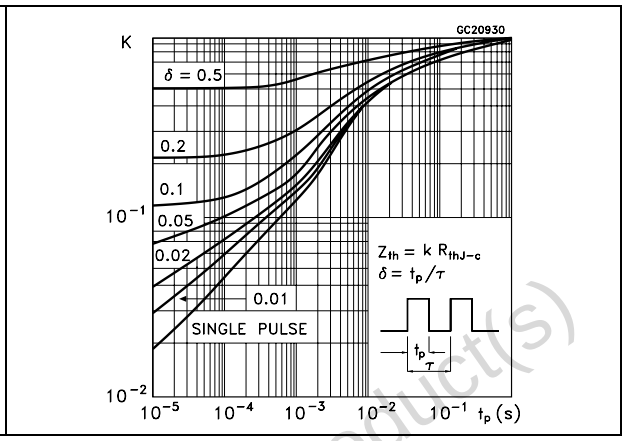


Figure 3. Output characteristics

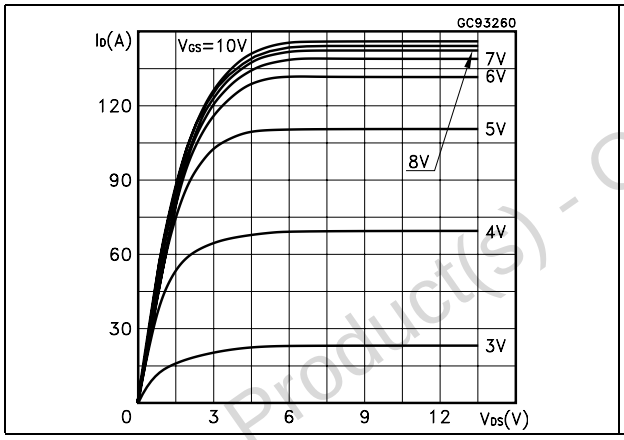


Figure 4. Transfer characteristics

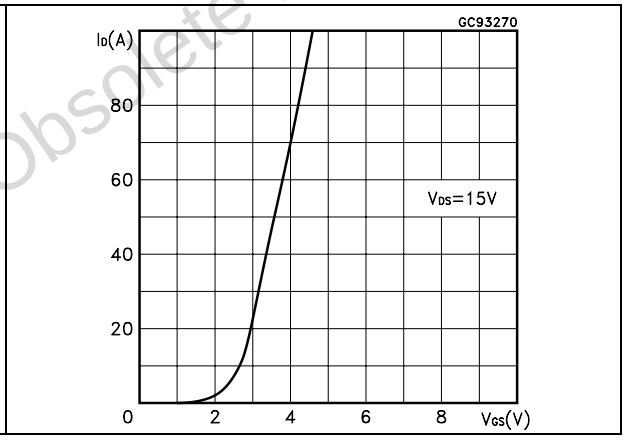


Figure 5. Transconductance

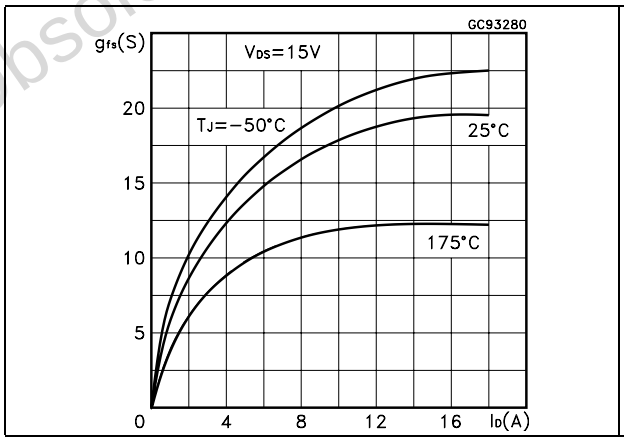


Figure 6. Static drain-source on resistance

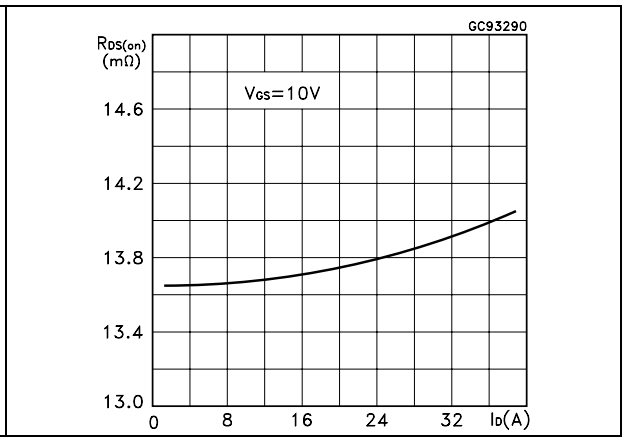


Figure 7. Gate charge vs. gate-source voltage

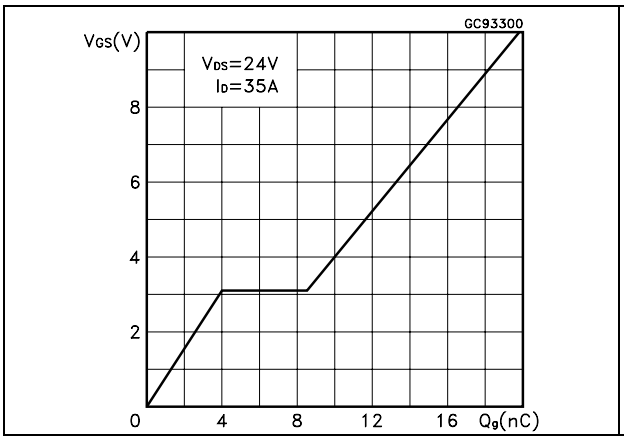


Figure 8. Capacitance variations

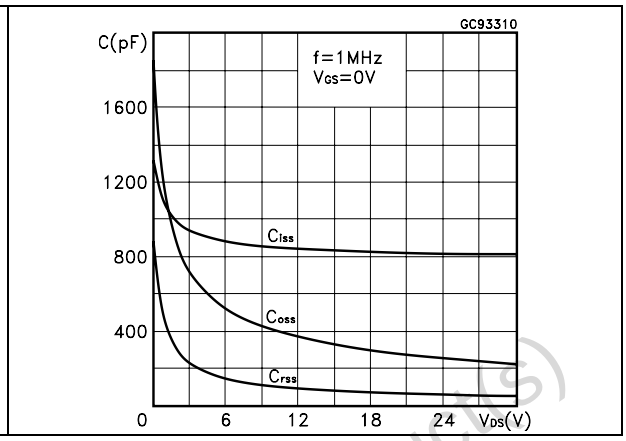


Figure 9. Normalized gate threshold voltage vs. temperature

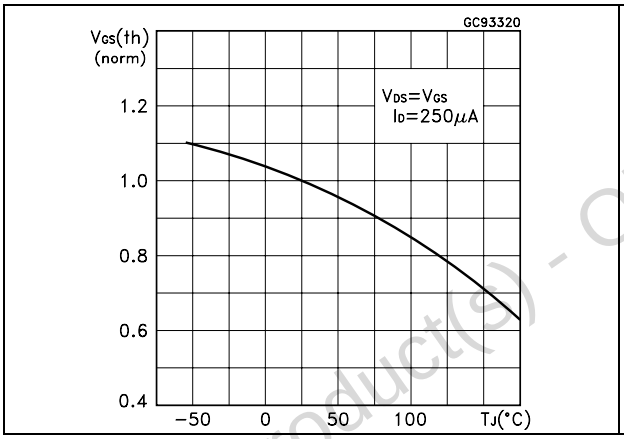


Figure 10. Normalized on resistance vs. temperature

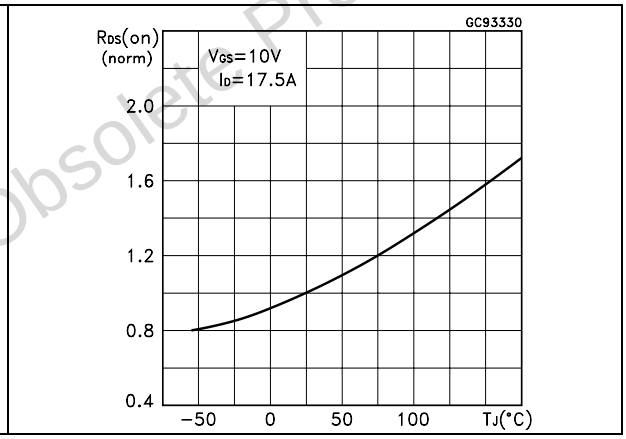
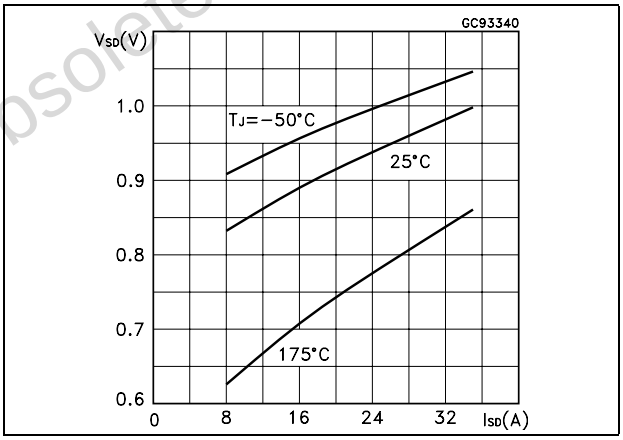


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load

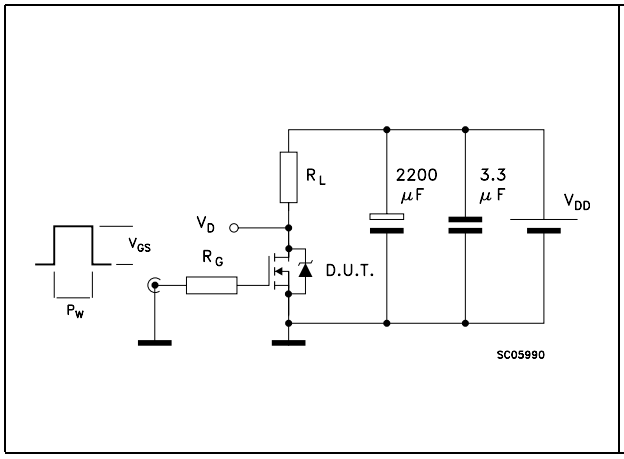


Figure 13. Gate charge test circuit

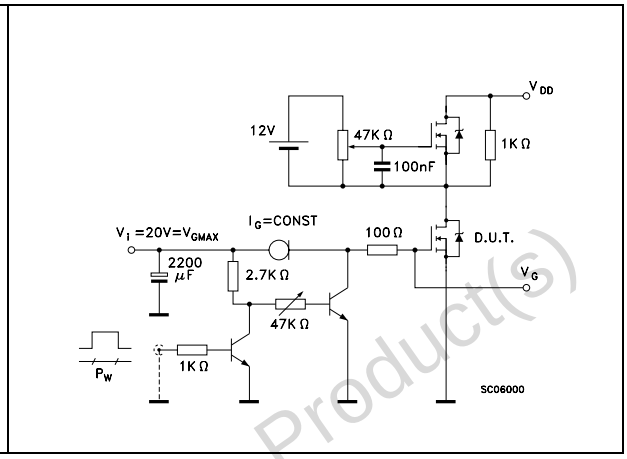


Figure 14. Test circuit for inductive load switching and diode recovery times

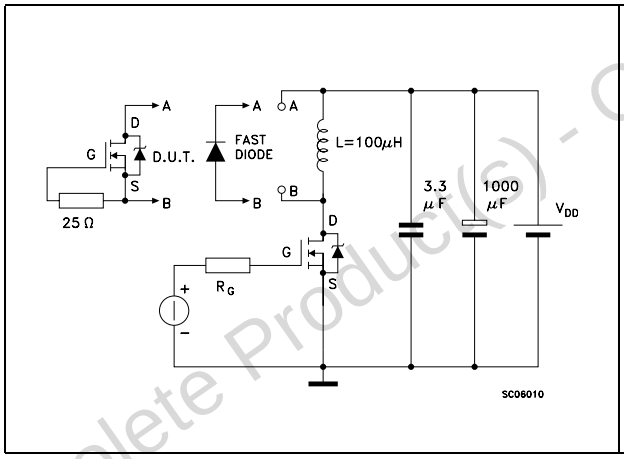


Figure 15. Unclamped Inductive load test circuit

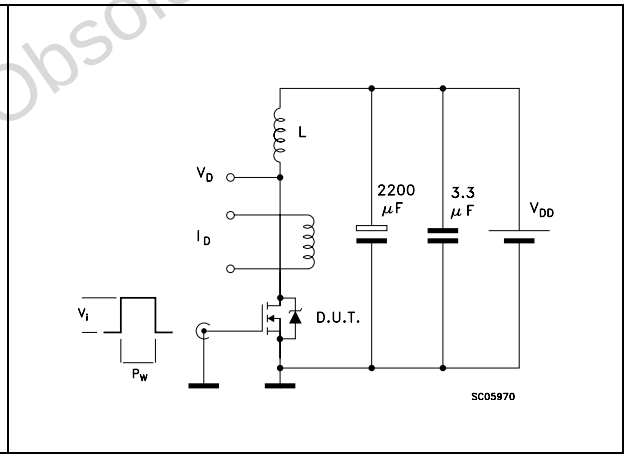


Figure 16. Unclamped inductive waveform

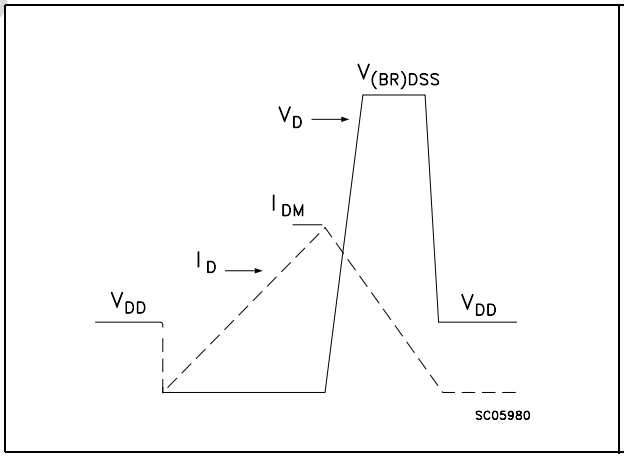
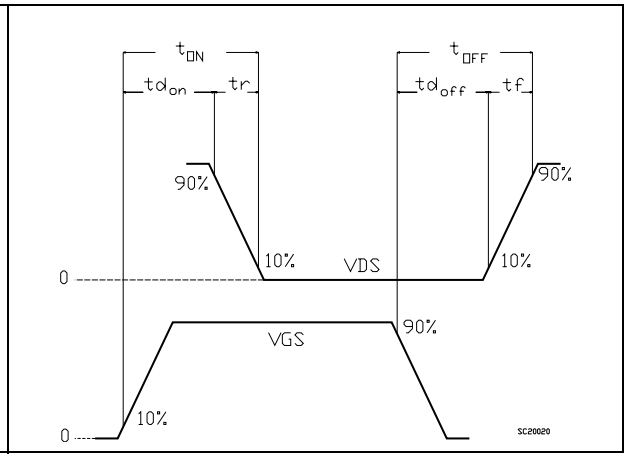


Figure 17. Switching time waveform

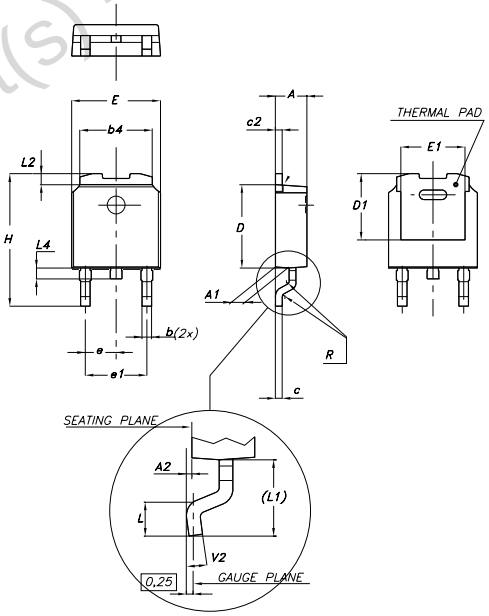


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

DPAK MECHANICAL DATA

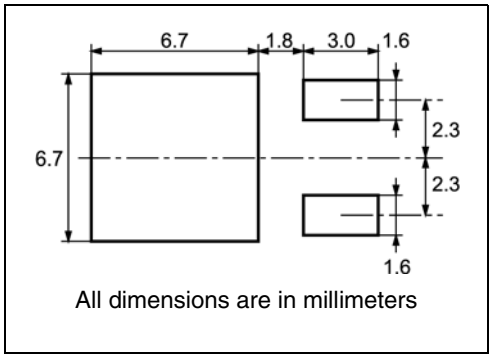
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



0068772-F

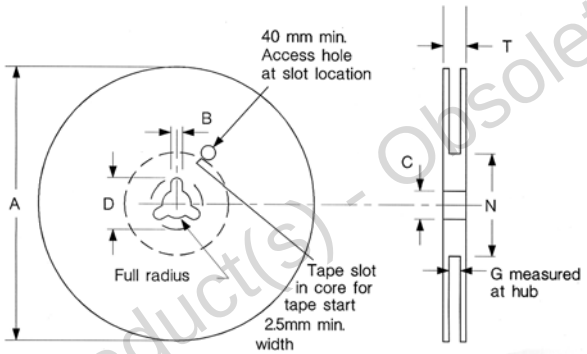
5 Packing mechanical data

DPAK FOOTPRINT



All dimensions are in millimeters

TAPE AND REEL SHIPMENT



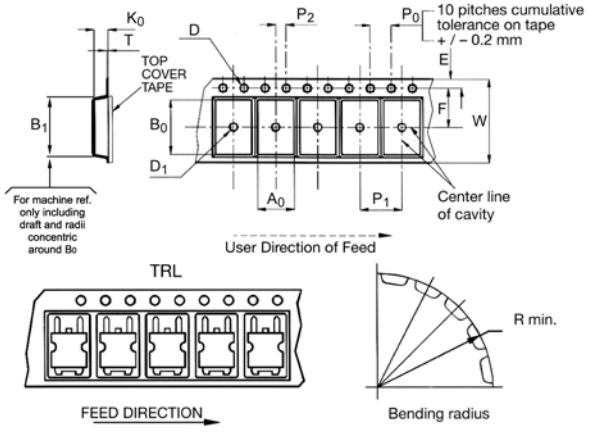
REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641



6 Revision history

Table 6. Revision history

Date	Revision	Changes
21-Jun-2004	2	Preliminary version
06-Jul-2006	3	New template, no content change
14-sep-2006	4	Removed IPAK
20-Feb-2007	5	Typo mistake on page 1