



## STE45NK80ZD

N-channel 800V - 0.11 $\Omega$  - 45A ISOTOP  
SuperFREDmesh™ MOSFET

### General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>w</sub>
STE45NK80ZD	800V	<0.13 $\Omega$	45A	600W

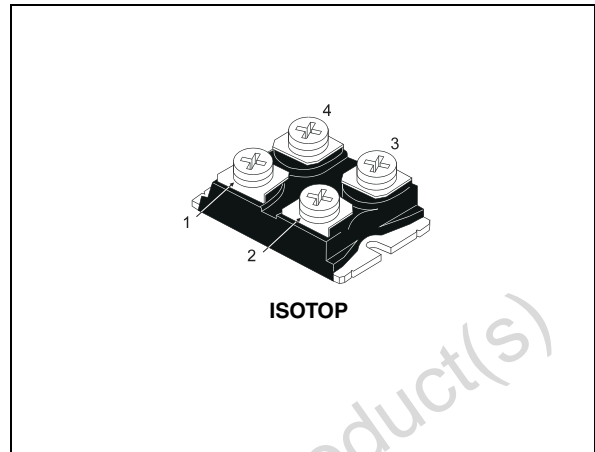
- Extremely high dv/dt capability
- 100% avalanche tested
- Very low intrinsic capacitances
- Very good manufacturing repeatability

### Description

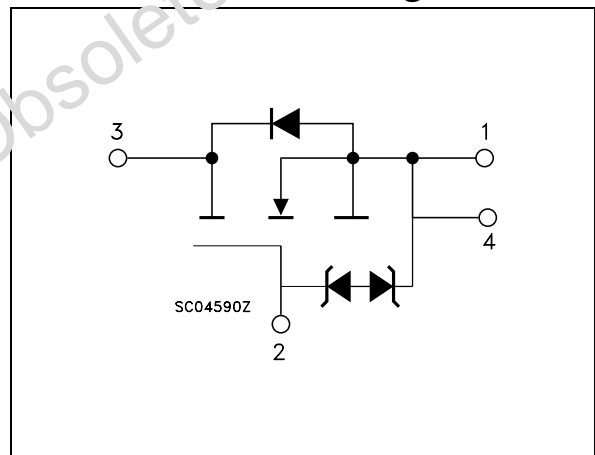
The SuperFREDMesh™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

### Applications

- Switching application



### Internal schematic diagram



### Order codes

Part number	Marking	Package	Packaging
STE45NK80ZD	E45NK80ZD	ISOTOP	Tube

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Obsolete Product(s) - Obsolete Product(s)

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	800	V
$V_{DGR}$	Drain-gate voltage ( $R_{GS} = 20 \text{ kW}$ )	800	V
$V_{GS}$	Gate- source voltage	$\pm 30$	V
$I_D$	Drain Current (continuous) at $T_C = 25^\circ\text{C}$ (Steady State)	45	A
$I_D$	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	28	A
$I_{DM}^{(1)}$	Drain Current (pulsed)	180	A
$P_{TOT}$	Total Dissipation at $T_C = 25^\circ\text{C}$ (steady state)	600	W
$P_{TOT}$	Derating factor	5	W/°C
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5kW)	7	KV
$dv/dt^{(2)}$	Peak diode recovery voltage slope	8	V/ns
$V_{ISO}$	Insulation withstand voltage (AC-RMS) from all four terminals to external heatsink	2500	V
$T_j$ $T_{stg}$	Operating junction temperature Storage temperature	- 65 to 150	°C

1. Pulse width limited by safe operating area

2.  $I_{SD} \leq 45\text{A}$ ,  $di/dt \leq 500 \text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ .

**Table 2. Thermal data**

$R_{thj-case}$	Thermal Resistance Junction-case Max	0.2	°C/W
$R_{thj-amb}$	Thermal Resistance Junction-ambient Max	40	°C/W

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j \text{ max}$ )	45	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 35 \text{ V}$ )	1.2	J

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}\text{C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1 \text{ mA}$ , $V_{GS} = 0$	800			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ , $T_C = 125^{\circ}\text{C}$			10 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 150\mu\text{A}$	2.5	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{V}$ , $I_D = 22.5 \text{ A}$		0.11	0.13	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{V}$ , $I_D = 22.5 \text{ A}$		35		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{V}$ , $f = 1 \text{ MHz}$ , $V_{GS} = 0$		26000 1620 260		pF pF pF
$C_{oss \text{ eq.}}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0\text{V}$ , $V_{DS} = 0\text{V}$ to 720V		700		pF
$t_{d(on)}$ $t_r$ $t_{d(off)}$ $t_f$	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 400 \text{ V}$ , $I_D = 20 \text{ A}$ $R_G = 4.7\Omega$ , $V_{GS} = 10 \text{ V}$ (see <a href="#">Figure 18</a> )		105 128 350 174		ns ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 400 \text{ V}$ , $I_D = 40 \text{ A}$ , $V_{GS} = 10\text{V}$		558 121 307	781	nC nC nC

1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

2.  $C_{oss \text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 6. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current				45	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				180	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 45\text{ A}$ , $V_{GS} = 0$			1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 40\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 50\text{ V}$ , $T_j = 25^\circ\text{C}$		375		ns
$Q_{rr}$	Reverse recovery charge			4.65		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			24.8		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 40\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 50\text{ V}$ , $T_j = 150^\circ\text{C}$		568		ns
$Q_{rr}$	Reverse recovery charge			9.66		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			34		A

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

**Table 7. Gate-source zener diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$ (open drain)	30			V

## 2.1 Protection features of gate-to-source zener diodes

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.2 Electrical characteristics (curves)

Figure 1. Safe operating area

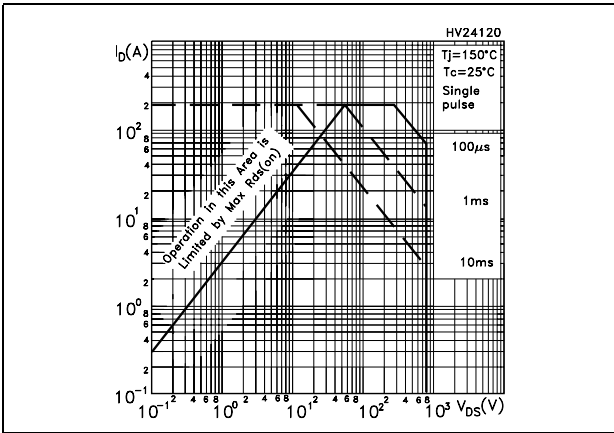


Figure 2. Thermal impedance

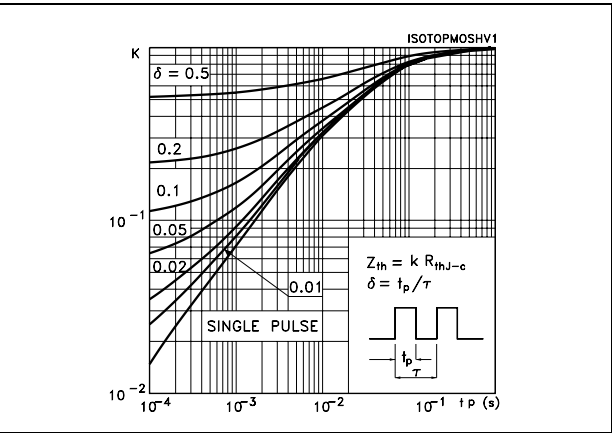


Figure 3. Output characteristics

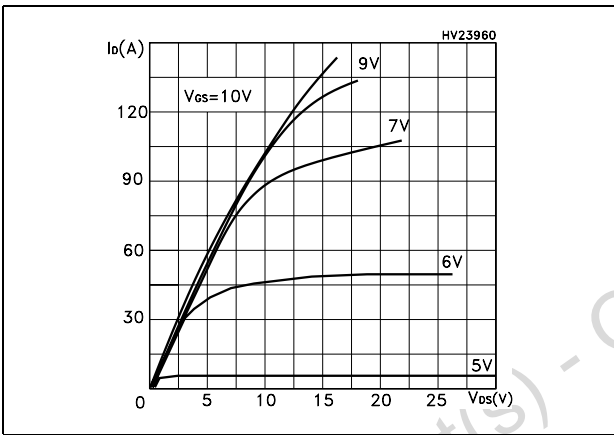


Figure 4. Transfer characteristics

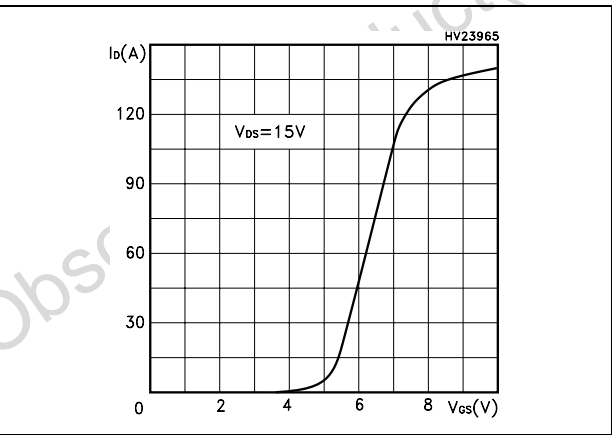


Figure 5. Transconductance

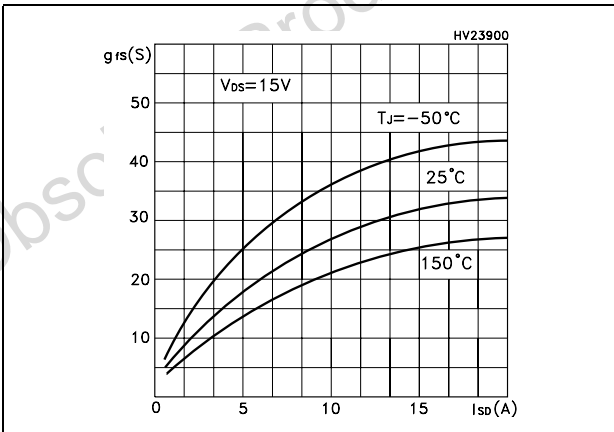


Figure 6. Static drain-source on resistance

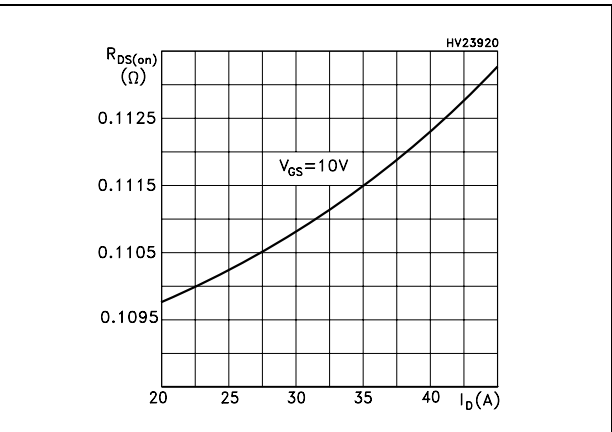


Figure 7. Gate charge vs gate-source voltage    Figure 8. Capacitance variations

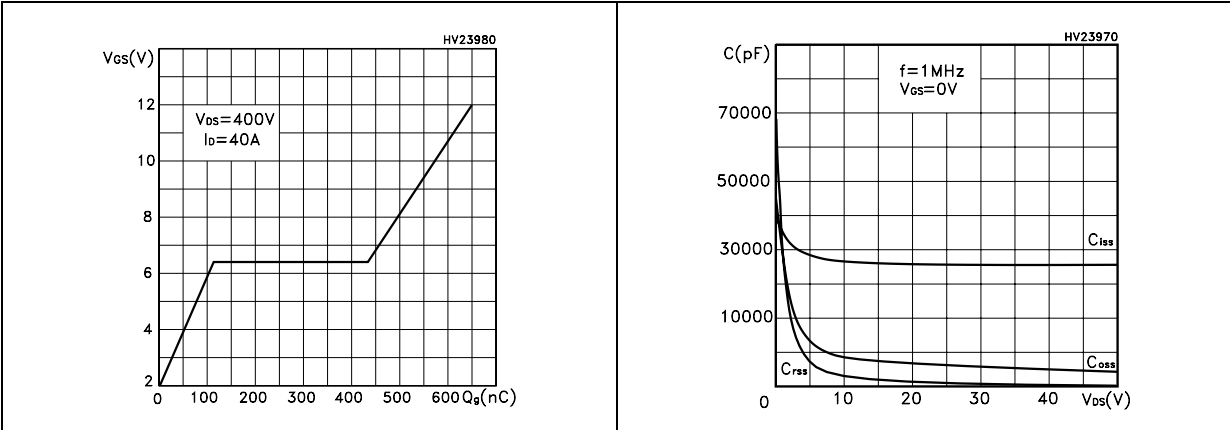


Figure 9. Normalized gate threshold voltage vs temperature    Figure 10. Normalized on resistance vs temperature

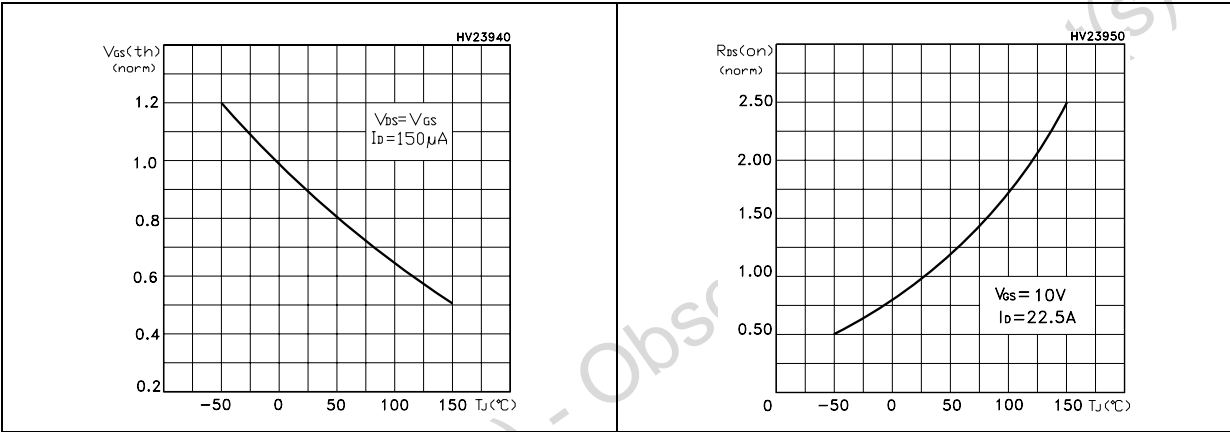
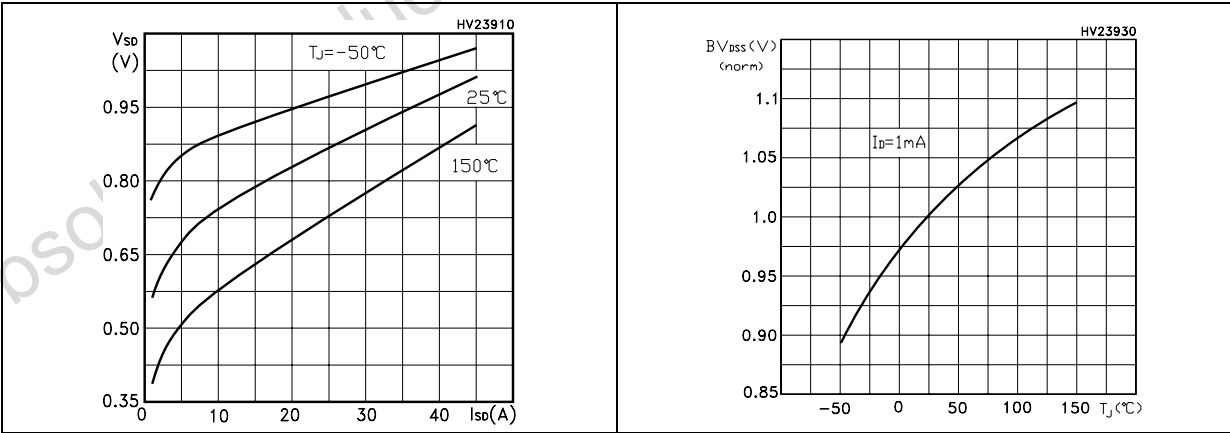
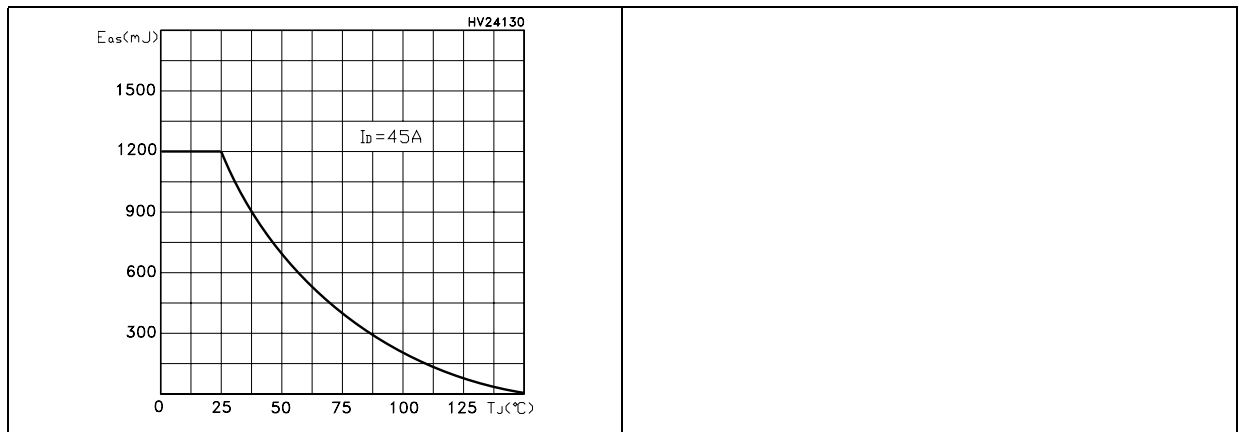


Figure 11. Source-drain diode forward characteristics    Figure 12. Normalized  $B_{V_{DS}}$  vs temperature



**Figure 13. Avalanche energy vs starting  $T_j$** 

### 3 Test circuit

Figure 14. Unclamped Inductive load test circuit

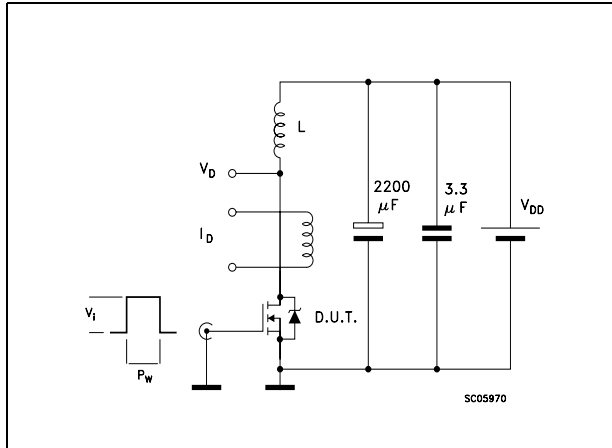


Figure 15. Unclamped inductive waveform

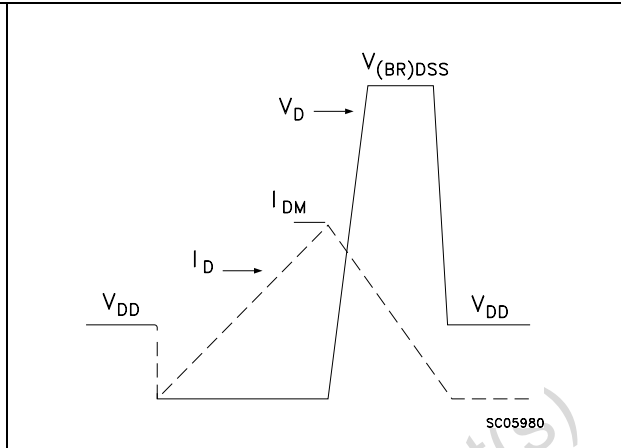


Figure 16. Switching times test circuit for resistive load

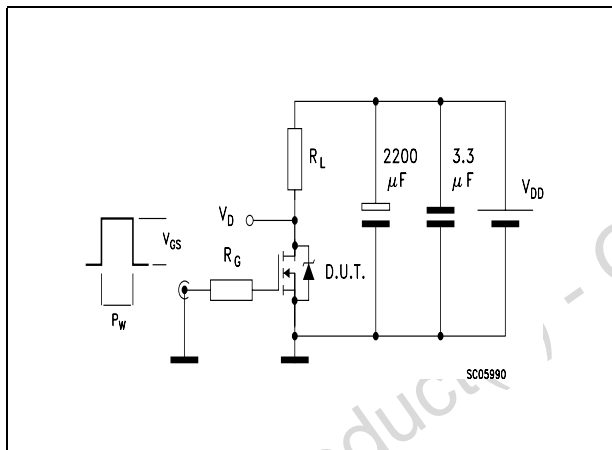


Figure 17. Gate charge test circuit

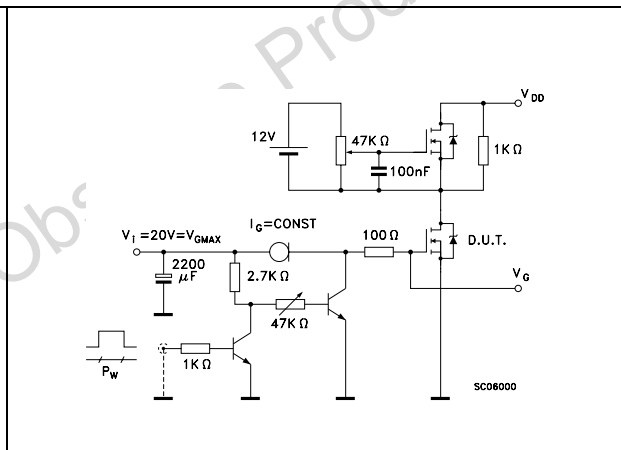
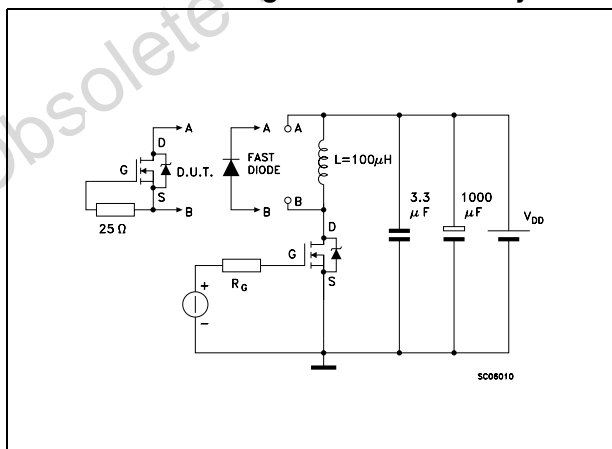


Figure 18. Test circuit for inductive load switching and diode recovery times



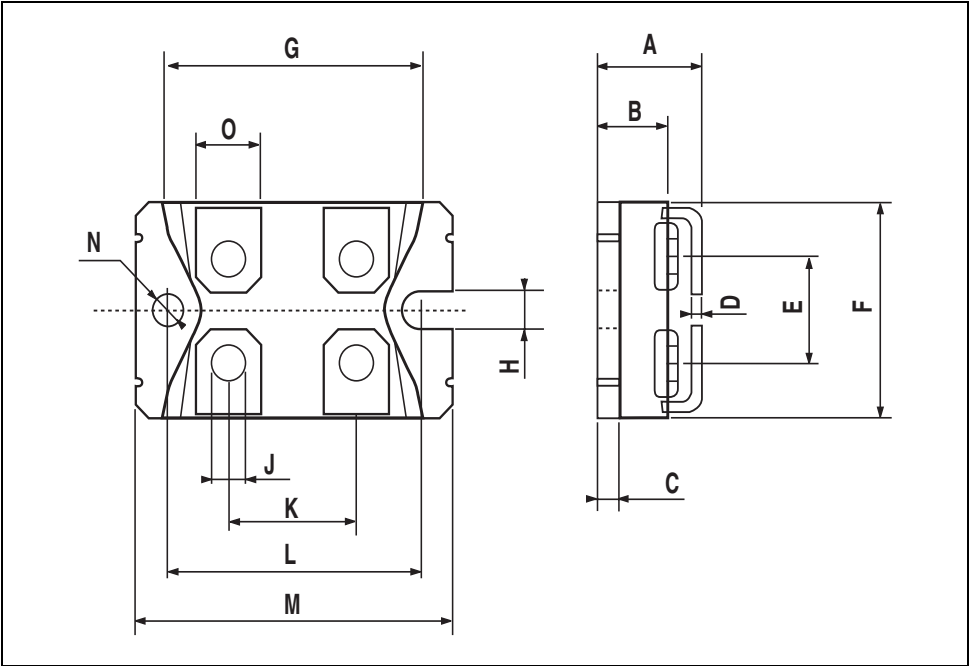
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

Obsolete Product(s) - Obsolete Product(s)

ISOTOP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	11.8		12.2	0.466		0.480
B	8.9		9.1	0.350		0.358
C	1.95		2.05	0.076		0.080
D	0.75		0.85	0.029		0.033
E	12.6		12.8	0.496		0.503
F	25.15		25.5	0.990		1.003
G	31.5		31.7	1.240		1.248
H	4			0.157		
J	4.1		4.3	0.161		0.169
K	14.9		15.1	0.586		0.594
L	30.1		30.3	1.185		1.193
M	37.8		38.2	1.488		1.503
N	4			0.157		
O	7.8		8.2	0.307		0.322



## 5 Revision history

**Table 8. Document revision history**

Date	Revision	Changes
24-May-2005	1	First Release
10-Jun-2005	2	Inserted new row in <a href="#">Table 6.: Switching times</a>
28-Sep-2005	3	Complete version
14-Oct-2005	4	Modified <a href="#">Figure 3</a> , <a href="#">Figure 6</a>
06-Mar-2006	5	New Stylesheet
29-Mar-2006	6	Modified value on <a href="#">Table 4.</a>
27-Jun-2006	7	New template, no content change

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