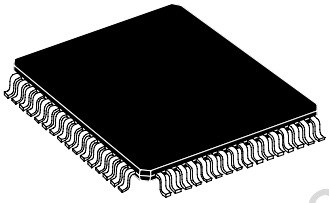
STV6412A

Audio/video switch matrix

Features

- I²C bus control
- Standby mode with interrupt signal output
- Video section
  - 4 CVBS inputs, 3 CVBS outputs (one with selectable chroma trap filter)
  - 3 Y/C inputs, 2 Y/C outputs
  - 6 dB gain on all CVBS/Y and C outputs
  - Integrated 150 Ω buffers
  - 1 Y/C adder
  - 2 RGB/FB inputs, 1 tri-state RGB/FB output with 6 dB adjustable gain (from +3dB to +9dB)
  - Video muting on all outputs
  - 2 slow blanking inputs/outputs
  - Sync bottom clamp on all CVBS/Y and RGB inputs, average clamp on C Inputs
  - Bandwidth: 15 MHz
  - Crosstalk: 50 dB minimum
- Audio Section
  - 4 stereo inputs, 3 stereo outputs
  - 1 mono-sound output
  - stereo-to-mono sound capability
  - 0/6/9 dB selectable gain on one stereo input
  - Full range volume control with soft control
  - Audio muting on all outputs



LQFP64L(14 x 14 x 1.4 mm)
(Low-profile Quad Flat Package)

Order code: STV6412ADT

Description

The STV6412A is a highly integrated I²C bus-controlled audio and video switch matrix, optimized for use in digital set-top box applications. It provides all the audio and video routings required in a full two SCART set-top box design.

Contents

1 General overview

1.1 Pin connections

Figure 1. Pinout dagram

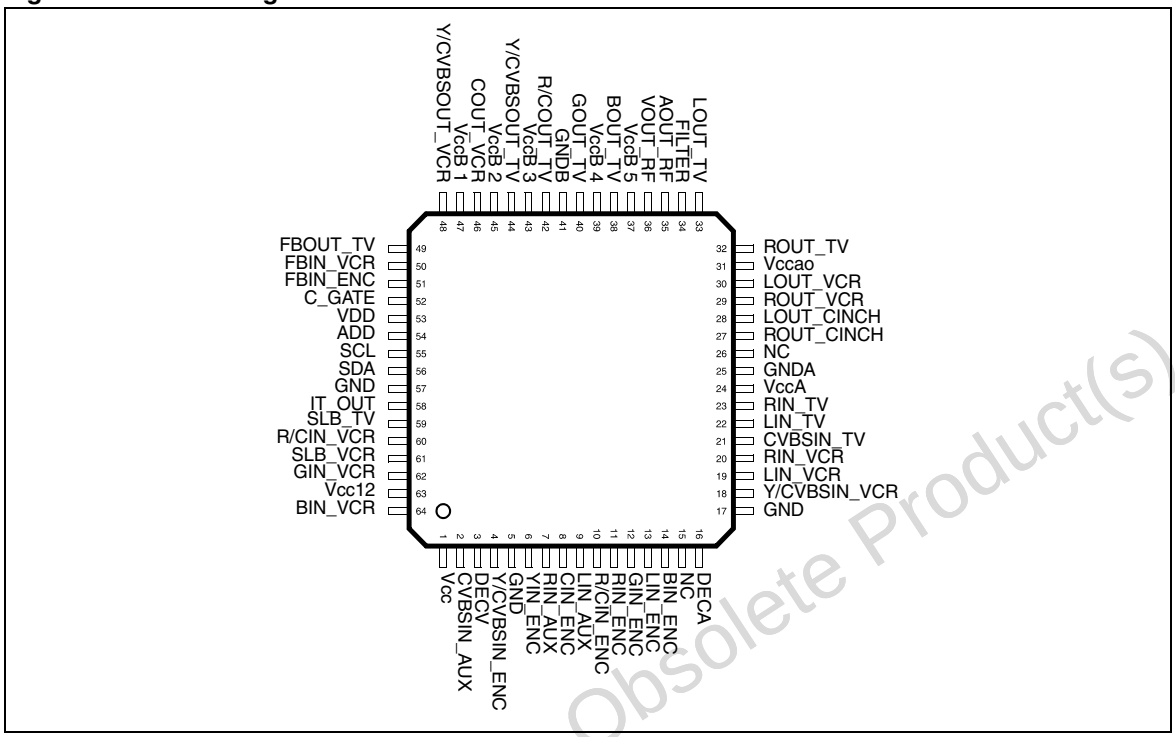


Table 1. Pin description

Pin no.	Symbol	Description
1	V_{CC}	+5 V supply
2	CVBSIN_AUX	CVBS input from auxiliary
3	DECV	Video decoupling capacitor
4	Y/CVBSIN_ENC	Y/CVBS input from encoder
5	GND	Ground
6	YIN_ENC	Y input from encoder
7	RIN_AUX	Audio right input from auxiliary
8	CIN_ENC	Chroma input from encoder
9	LIN_AUX	Audio left, input from auxiliary
10	R/CIN_ENC	Red/Chroma input from encoder
11	RIN_ENC	Audio right, input from encoder
12	GIN_ENC	Green input from encoder
13	LIN_ENC	Audio left, input from encoder

Table 1. Pin description (continued)

Pin no.	Symbol	Description
14	BIN_ENC	Blue input from encoder
15	NC	Not connected
16	DECA	Audio decoupling capacitor
17	GND	Ground
18	Y/CVBSIN_VCR	Y/CVBS input from VCR SCART
19	LIN_VCR	Audio left, input from VCR SCART
20	RIN_VCR	Audio right, input from VCR SCART
21	CVBSIN_TV	CVBS input from TV SCART
22	LIN_TV	Audio left, input from TV SCART
23	RIN_TV	Audio right, input from TV SCART
24	V_{CCA}	Audio supply voltage - or - audio supply decoupling
25	GNDA	Audio ground
26	NC	Not connected
27	ROUT_CINCH	Audio right output to cinch
28	LOUT_CINCH	Audio left output to cinch
29	ROUT_VCR	Audio right output to VCR SCART
30	LOUT_VCR	Audio left output to VCR SCART
31	V_{CCAO}	Audio output supply voltage - or - main audio supply voltage
32	ROUT_TV	Audio right output to TV SCART
33	LOUT_TV	Audio left output to TV SCART
34	FILTER	Chroma trap filter
35	AOUT_RF	Audio (L+R) output to RF modulator
36	VOUT_RF	CVBS video output to RF modulator
37	V_{CCB5}	Video output buffer supply pin
38	BOUT_TV	Blue output to TV SCART
39	V_{CCB4}	Video output buffer supply pin
40	GOUT_TV	Green output to TV SCART
41	GNDB	Video buffer ground
42	R/COUT_TV	Red/Chroma output to TV SCART
43	V_{CCB3}	Video output buffer supply pin
44	Y/CVBSOUT_TV	Y/CVBS output to TV SCART
45	V_{CCB2}	Video output buffer supply pin
46	COUT_VCR	Chroma output to VCR SCART
47	V_{CCB1}	Video output buffer supply pin
48	Y/CVBSOUT_VCR	Y/CVBS output to VCR SCART

Table 1. Pin description (continued)

Pin no.	Symbol	Description
49	FBOUT_TV	Fast blanking output to TV SCART
50	FBIN_VCR	Fast blanking input from VCR SCART
51	FBIN_ENC	Fast blanking input from encoder
52	C_GATE	External MOS command for C_VCR bidirectional mode
53	V_{DD}	+5 V I^2C supply
54	ADD	I^2C address selection
55	SCL	I^2C bus clock
56	SDA	I^2C bus data
57	GND	Ground digital
58	IT_OUT	Interrupt output
59	SLB_TV	Slow blanking input/output from TV SCART
60	R/CIN_VCR	Red input (or C input) from VCR SCART
61	SLB_VCR	Slow blanking input/output from VCR SCART
62	GIN_VCR	Green input from VCR SCART
63	V_{CC12}	+12 V supply
64	BIN_VCR	Blue input from VCR SCART

1.2 Block diagrams

Figure 2. STV6412A block diagram

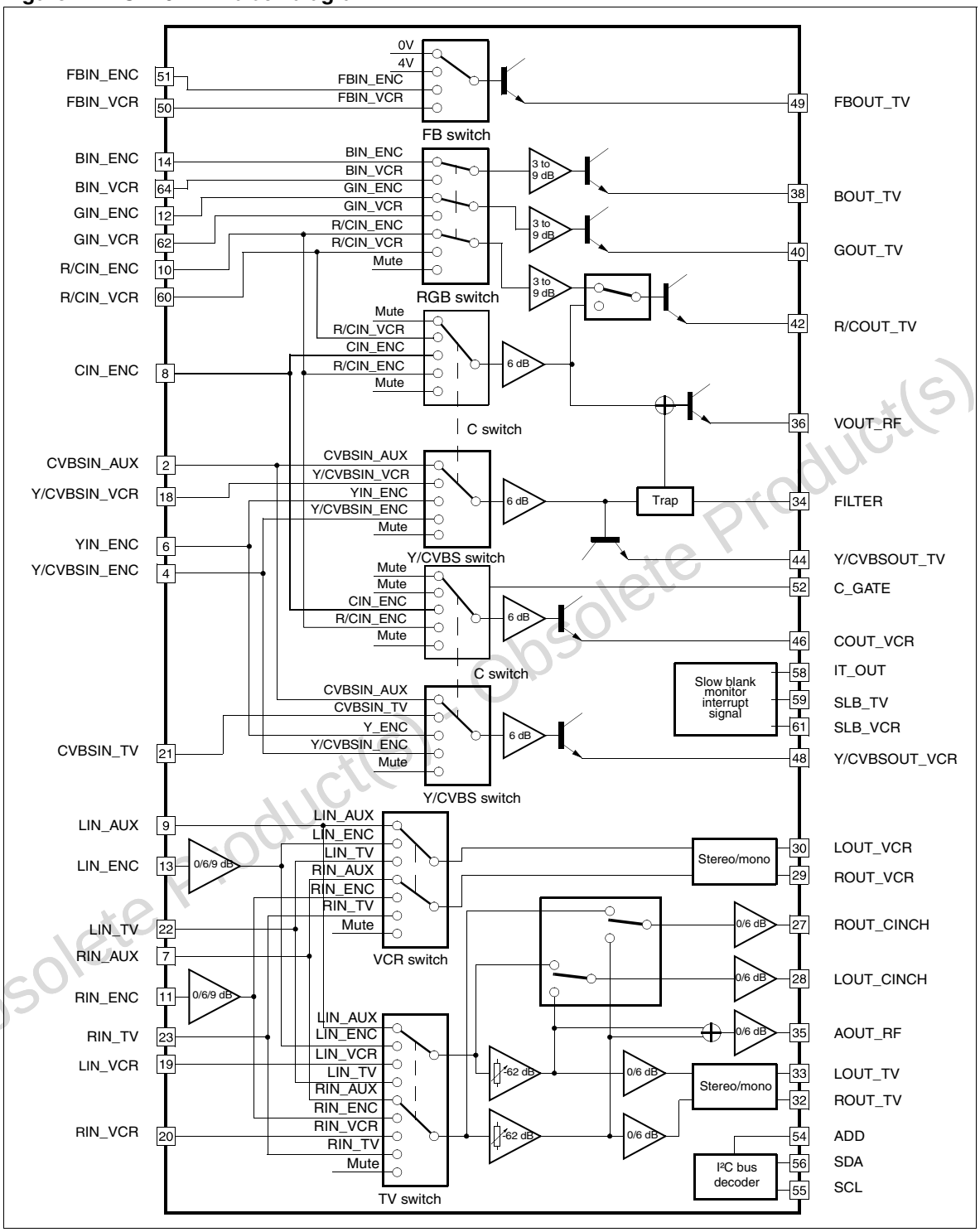
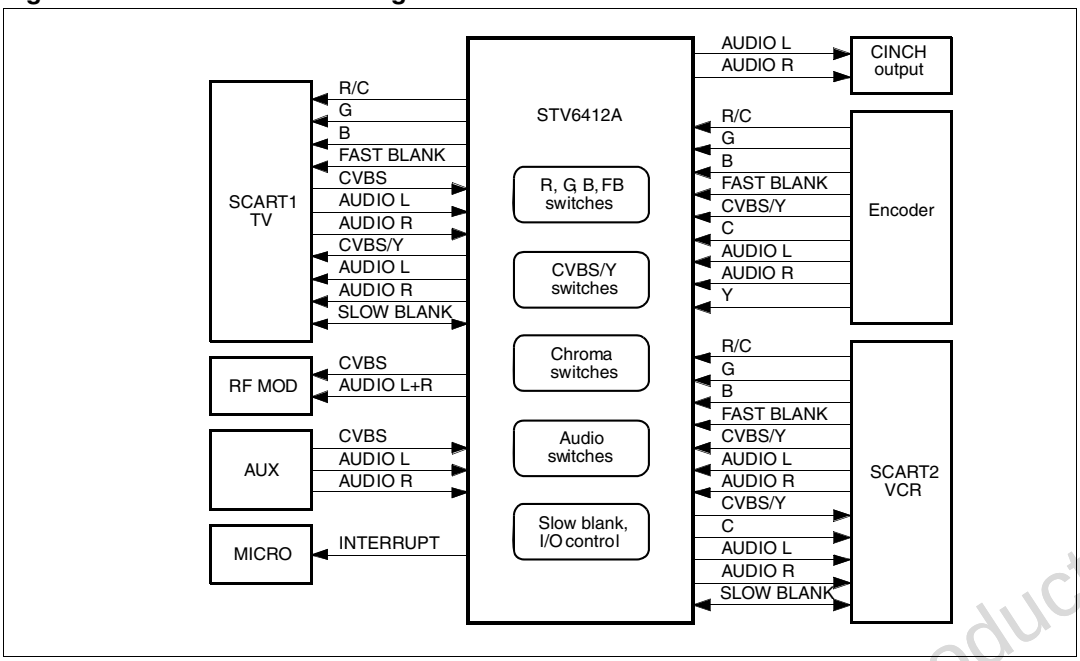


Figure 3. Functional block diagram



2 Electrical characteristics

2.1 Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{CC12}	Supply voltage for:	- Slow blanking sections	13.2	V
V_{CCAO}		- Audio drivers	13.2	V
V_{CCA}		- Internal digital audio parts	10	V
V_{DD}		- Digital parts	6	V
V_{cc}, V_{CCBi}		- Video sections	6	V
V_I	Voltage at pin I to GND:	- Audio pins	0, V_{CCA}	V
		- Video pins	0, V_{CC} or V_{CCBi}	V
		- Bus pins	0, 5.5	V
		- Slow blanking pins	0, V_{CC12}	V
V_{ESD}	Maximum ESD voltage allowed. 100 pF capacitor discharged through 1.5 kΩ serial resistor (human body model)		±4	kV
T_{oper}	Operating ambient temperature		0, +70	°C
T_{stg}	Storage temperature		-20, +150	°C

2.2 Thermal data

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction-ambient thermal resistance (maximum)	48	°C/W

2.3 Latch up

At an ambient temperature of 25 °C, all pins meet the following specifications:

- I trigger = 200 mA or I trigger = 200 mA.
- Pin 58 (IT_OUT) does not meet this specification and the trigger current must be limited to -100 mA.

2.4 Recommended operating conditions

T_{amb} = 25 °C, V_{CCAO} = 12 V, V_{CC} = 5 V, V_{CC12} = 12 V, V_{DD} = 5 V

R_{GA} = 600 Ω, R_{LOUTA} = 10 kΩ, R_{GV} = 50 Ω, R_{LOUTV} = 150 Ω, unless otherwise specified.

Table 2. Supply voltages

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DD}	Digital supply voltage		4.75	5	5.25	V
V_{CCAO}	Audio operating supply voltage	- Decoupling capacitor on V_{CCA} - Connected to V_{CCA}	11.2 8.5	12 9	12.8 9.5	V V
V_{CC}	Video operating supply voltage		4.75	5	5.25	V
V_{CC12}	Slow blanking control supply voltage		11.2	12	12.8	V

Table 3. Active mode (all channels ON)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{DD}	Digital supply current	V_{DD} = 5 V		4.5	10	mA
I_{CCA}	Audio supply current	V_{CCAO} = 12 V, no load		9	15	mA
I_{CCV}	Total video supply current (V_{CC}+V_{CCB1}+V_{CCB2}+V_{CCB3}+V_{CCB4}+V_{CCB5})	V_{CC} = 5 V, no load		43	60	mA
I_{CC12}	12 V Supply Current	V_{CC12} = 12 V SLB input mode SLB output mode, no load		0 2.5	1 4	mA

Table 4. Standby mode (all channels OFF)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{DD}	Digital supply current	V_{DD} = 5 V		4.5	10	mA
I_{CCAstd}	Audio supply current	V_{CCA0} = 12 V, no load		3		mA
I_{CCVstd}	Total video supply current	V_{CC} = 5 V		1		mA

2.5 Audio section characteristics

T_{amb} = 25°C, V_{CCAO} = 12 V, V_{CC} = 5 V, V_{CC12} = 12 V, V_{DD} = 5 V

R_{GA} = 600 Ω, R_{LOUTA} = 10 kΩ, R_{GV} = 50 Ω, R_{LOUTV} = 150 Ω, unless otherwise specified.

Table 5. Audio section characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
SVR100	Supply voltage rejection	V_{RIPPLE} = 500m V_{RMS} at f = 100 Hz, Gain= 0 dB, DECA filter cap = 47 µF DECA filter cap = 220 µF	60	70 80		dB dB
SVR1K	Supply voltage rejection	V_{RIPPLE} = 500m V_{RMS} at f = 1 kHz, Gain = 0 dB	70	80		dB
V_{INDC}	Input DC Level	V_{CCA} = 9 V		$V_{CCA/2}$		V
V_{INAC}	Input signal amplitude				2	V_{RMS}
R_{IN}	Input resistance		30	50		kΩ

Table 5. Audio section characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$R_{INmatch}$	Input resistance matching			±2	±10	%
F_{RANGE}	Bandwidth	-3 dB, 0.5 V_{RMS}, R_{LOAD} = 10 kΩ, gain = 0 dB	50			kHz
Flatness	Spread of gain in audio band	-0.5 V_{RMS}, 20 Hz to 20 kHz, gain = 0 dB			0.5	dB
CS	Channel separation, from audio inputs between L & R of TV outputs	V_{IN} = 0.5 V_{RMS}, f = 1 kHz, on one input, R_{LOAD} = 10 kΩ, gain = 0 dB	80 70	90 74		dB dB
Ci	Channel isolation from video inputs	V_{IN} = 1 V_{pp}, f = 15 kHz, on one point		85		dB
V_{OUT}	Output DC Level	V_{CCA} = 9 V		$V_{CCA/2}$		V
V_{OFF}	DC offset change	Switching between inputs		1	±15	mV
R_{OUT}	Output resistance			60	120	W
PHD	Phase dDifference	f = 1 kHz, 1 V_{RMS} input on each input channel			3	° deg.
ASN	S/N Ratio	f = 1 kHz, 1 V_{RMS} input (gain = 0dB) weighted CCIR 468-4 quasi peak	70			dB
eNI	Equivalent RMS Input voltage noise	BW = 20 Hz, 20 kHz flat, gain = 0 dB		5		µV
G0	0 dB gain	0.5 V_{RMS}, R_{LOAD} = 10 kΩ, gain = 0 dB	-0.5		+0.5	dB
G_{STEP}	Gain step	-62 dB to +6 dB (see *Figure 2*)		2		dB
G_{MATCH1}	Gain matching between different inputs of one output	V_{IN} = 0.5 V_{RMS}, 1 kHz, Gain = 0 dB	-0.5		0.5	dB
G_{MATCH2}	Gain matching between left/right outputs of one input channel	V_{IN} = 0.5 V_{RMS}, 1 kHz, Gain = 0 dB	-0.5		0.5	dB
THD0 THD6 THD9	Total harmonic distortion ENC input at 0 dB ENC input at 6 dB ENC input at 9 dB	V_{OUT} = 0.5 V_{RMS}, 1 kHz, LPF @ 80 kHz		0.01 0.01 0.01	0.1 0.1 0.1	% % %
V_{CL}	Output clipping level	THD = 0.2%, 1 kHz	2.1	2.3		V_{RMS}
R_L	Output load resistance	V_{IN} = 1 V_{RMS}, THD = 0.3%, Gain = 0 dB	2	2.25		kΩ
Mute	Mute suppression	V_{IN} = 0.5 V_{RMS}, on one point	-90			dB

2.6 Video section characteristics

T_{amb} = 25 °C, V_{CCAO} = 12 V, V_{CC} = 5 V, V_{CC12} = 12 V, V_{DD} = 5 V

R_{GA} = 600 Ω, R_{LOUTA} = 10 kΩ, R_{GV} = 50 Ω, R_{LOUTV} = 150 Ω, unless otherwise specified.

Table 6. Video section characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DCIN}	DC input level	Bottom synch pulse		2		V
I_{CLAMP}	Clamping current	at VDCIN -400 mV	1	2		mA
I_{LEAK}	Input leakage current	VIN = VDCIN +1 V		1	10	µA
C_{IN}	Input capacitance			2		pF
V_{IN}	Max input signal	VCC = 5 V		1.5		V_{PP}
DYN	Dynamic output signal	VCC = 5 V		3		V_{PP}
BW	Bandwidth at -3 dB Y/CVBS RGB Y/C mixer (on VOUT-RF)	 VIN = 1 VPP VIN = 1 VPP VIN = 1 VPP, VINC = muted	 12 12 8	 15 15 10		 MHz MHz MHz
Flatness	Spread of gain in video band (15 kHz - 5 MHz) Y/CVBS RGB Y/C Mixer (on VOUT-RF)	 VIN = 1 VPP VIN = 1 VPP VIN = 1 VPP, VINC = muted			 +/-0.5 +/-0.5 +/-1.5	 dB dB dB
CTi	Crosstalk isolation between input channel	VIN = 1 VPP at f = 4.43 MHz, on one point		60		dB
CTo	Crosstalk isolation between output channel	VIN = 1 VPP at f = 4.43 MHz, on one point, RLOAD = 150Ω		50		dB
R_{OUT}	Output resistance			5	10	Ω
G_{RGB}	Gain at RGB outputs	V_{IN} = 1 V_{pp}, gain set to 6 dB	5.5	6	6.5	dB
G_{RGBM}	Gain matching between R, G, B	V_{IN} = 1 V_{PP}, gain set to 6 dB	-0.3	0	0.3	dB
$G_{RGBSTEP}$	Step of gain	3 dB to 6 dB	0.75	1	1.25	dB
G_{YCVBS}	Gain on Y,/CVBS channels	V_{IN} = 1 V_{PP}	5.5	6	6.5	dB
G_{YCVBSM}	Gain matching between Y, CVBS inputs	V_{IN} = 1 V_{PP}	-0.5	0	0.5	dB
DC_{OUT}	DC output voltage	Bottom sync pulse		0.6		V
$DC_{OUT\ RF}$	RF output voltage	Bottom sync pulse		1		V
DPHI	Differential phase	V_{IN} = 1 V_{PP} at f = 4.43 MHz		1	5	° deg.
DG	Differential gain	V_{IN} = 1 V_{PP} at f = 4.43 MHz		1	5	%
Mute	Mute suppression	V_{IN} = 1 V_{PP} at f = 5 MHz on one point	-55			dB
LNL	Luminance non-linearity			0.3	3	%
VSN	Video S/N ratio	Refer to *Note 1*	65			dB

Note: 1 S/N = 20 log (V_{OUT} Black to White = 0.7 V_{PP} / V_{Noise} (mV_{RMS}) weighted CCIR 567).

2.7 Chroma section characteristics

T_{amb} = 25 °C, V_{CCAO} = 12 V, V_{CC} = 5 V, V_{CC12} = 12 V, V_{DD} = 5 V

R_{GA} = 600 Ω, R_{LOUTA} = 10 kΩ, R_{GV} = 50 Ω, R_{LOUTV} = 150 Ω, unless otherwise specified.

Table 7. Chroma section characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DCIN}	DC input level			3		V
R_{IN}	Input resistance		30	50		kΩ
C_{IN}	Input capacitance			2		pF
V_{IN}	Max input signal			1.5		V_{PP}
DYN	Dynamic output signal			3		V_{PP}
DC_{OUT}	DC output VCR voltage			2.2		V
CBW	Chroma Bandwidth	C_{IN} = 1 V_{PP} at -3 db	10			MHz
CTi	Crosstalk isolation between input channel	V_{IN} = 1 V_{PP} at f = 4.43 MHz, on one input		55		dB
CTo	Crosstalk isolation between output channel	V_{IN} = 1 V_{PP} at f = 4.43 MHz, on one input, R_{LOAD} = 150 Ω		50		dB
R_{OUT}	Output resistance			5	10	W
G_{OUTC}	Gain at OUTC	V_{IN} = 1 V_{pp}	5.5	6	6.5	dB
G_{CM}	Gain matching between C inputs	V_{IN} = 1 V_{PP}	-0.5	0	0.5	dB
Mute	Mute suppression	V_{IN} = 1 V_{PP} at f = 4.43 MHz on one input	-55			dB
CToYdel	Chroma to luma delay, source Y/C	Pin other than VOUT_RF, V_{PP} @ 4.43 MHz,			20	ns
CToYdel	Chroma to luma delay, source Y/C	Pin VOUT_RF			20	ns

2.8 Blanking section

T_{amb} = 25 °C, V_{CCAO} = 12 V, V_{CC} = 5 V, V_{CC12} = 12 V, V_{DD} = 5 V

R_{GA} = 600 Ω, R_{LOUTA} = 10 kΩ, R_{GV} = 50 Ω, R_{LOUTV} = 150 Ω, unless otherwise specified.

Table 8. Slow blanking section

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Input mode						
SLBlow	Input low level threshold		2.5	3.25	4	V
SLBhigh	Input high level threshold		7.5	8.25	9	V
I_{IN}	Input current			50	100	µA
Output mode						
SLBlow	Output low level (int. TV)		0	0.02	1.5	V

Table 8. Slow blanking section (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
SLBmed	Output medium level (ext. 16/9)		5	5.75	6.5	V
SLBhigh	Output high level (ext. 4/3)		10	11	12	V

Table 9. Fast blanking section

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Input mode						
FBlow/high	Input low/high level threshold		0.4	0.7	0.9	V
I_{IN}	Input current			2	10	µA
Output mode						
FB_{LOW} FB_{HIGH}	Output low level Output high level	R_{LOAD} = 150 Ω	 3.0	 3.4	0.5 3.8	V V
FB_{DEL}	Fast blanking RGB delay	At 50% on digital RGB transients, at 2 V on FB rise transient, at 1 V on FB fall, C_{LOAD} = 10pF maximum		15		ns
FB_{TRANS}	FB transitions at FB output Rise Time Fall Time	C_{LOAD} = 10 pF maximum between 10% and 90% between 90% and 10%		 10 10		 ns ns

Table 10. C_Gate function output

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
C_GATE-H	Pull-up resistor value to V_{CCB1}			20		kΩ
C_GATE-L	Output low level	I_{IN} = 0 mA I_{IN} = 1 mA			0.3 0.7	V V

Interrupt output (refer to *Note 1*)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
IT-Leak	High level leakage	External pull-up to 5 V			10	µA
IT-Low	Output low level (active)	I_{IN} = 0 mA I_{IN} = 1 mA			0.3 0.7	V V

Table 11. Address selection input

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
ADDsel_L	Address selection low level			0	0.2	V
ADDsel_H	Address selection high level		2.5		V_{DD}	V
I_{LEAK}	Leakage current				10	µA

Note: 1 The interrupt is forced to a low level when a change is detected on slow blanking inputs. It can be used in standby mode to wake up the microprocessor. It is released when the I^2C bus register is read.

2.9 I²C bus characteristics

T_{amb} = 25°C, V_{CCAO} = 12 V, V_{CC} = 5 V, V_{CC12} = 12 V, V_{DD} = 5 V

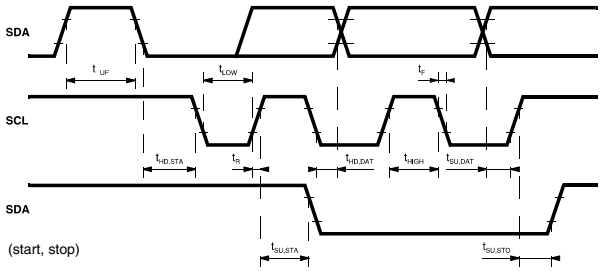
R_{GA} = 600Ω, R_{LOUTA} = 10kΩ, R_{GV} = 50Ω, R_{LOUTV} = 150Ω, unless otherwise specified.

Table 12. I²C bus characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
SCL						
V_{IL}	Low level input voltage		-0.3		1.5	V
V_{IH}	High level input voltage		2.3		5.5	V
I_{LI}	Input leakage current	V_{IN} = 0 to 5.5 V	-10	0	10	µA
SDA						
V_{IL}	Low level input voltage		-0.3		1.5	V
V_{IH}	High level input voltage		2.3		5.5	V
I_{LI}	Input leakage current	V_{IN} = 0 to 5.5 V	-10	0	10	µA
C_I	Input capacitance				10	pF
t_R	Input rise time	1.5 V to 3 V			1	µs
t_F	Input fall time	3 V to 1.5 V			300	ns
V_{OL}	Low level output voltage	I_{OL} = 3 mA			0.4	V
t_F	Output fall time	3 V to 1.5 V			250	ns
C_L	Load capacitance				400	pF
Timing						
t_{LOW}	Clock low period		4.7			µs
t_{HIGH}	Clock high period		4			µs
$t_{SU,DAT}$	Data setup time		250			ns
$t_{HD,DAT}$	Data hold time		0		340	ns
$t_{SU,STO}$	Setup time from clock high to stop		4			µs
t_{BUF}	Start setup time following a stop		4.7			µs
$t_{HD,STA}$	Start hold time		4			µs
$t_{SU,STA}$	Start Setup time following clock low to high transition		4.7			µs

Note: 1 The device can also operate at 400 kHz and is capable of interfacing with +3.3 V or + 5 V logic levels.

Figure 4. I²C bus timing



3 I²C bus selection

Data transfers follow the usual I²C format; that is, after the start condition (S), a 7-bit slave address is sent, followed by an eight-bit data direction bit (W). An 8-bit sub-address is sent to select a register, followed by an 8-bit data word to be included in the register. The IC's I²C bus decoder enables the automatic incrementation mode in write mode.

String format

Write only mode (S = Start condition, P = Stop condition, A = Acknowledge)

S	Slave address	0	A	Sub-address	A	Data	A	P

Read only mode

S	Slave address	1	A	Data	A	P

Slave address

Address	A6	A5	A4	A3	A2	A1	A0
Value	1	0	0	1	0	1	X

Auto increment mode

S	Slave address	0	A	Sub-address	A	Data0	A	Data1	A	....	Data*n*	A	P
						Sub-address		Sub-address +1			Sub-address + N		

3.1 I²C bus addresses

Write address: 1001 01X0, read address: 1001 01X1

Selection pin grounded address: X = 0, write address = 94(hex), read address = 95(hex)

Selection pin to supply address: X = 1, write address = 96(hex), read address = 97(hex)

Table 13. Input signal summary (write mode)

Reg addr (hex)	Data							
	d7	d6	d5	d4	d3	d2	d1	d0
Audio								
00	TV stereo mono	TV 0/6 dB	TV volume-62 dB to 0 dB - 2 dB steps					Soft volume mode
01	VCR stereo Mono	Not used (see *Note 1*)	VCR audio switch control		CINCH audio gain	TV/CINCH audio switch control		

Table 13. Input signal summary (write mode) (continued)

Reg addr (hex)	Data							
	d7	**d6**	**d5**	**d4**	**d3**	**d2**	**d1**	**d0**
Video								
02	VCR Chroma muted	VCR video and Chroma switch control			TV Chroma muted	TV video and Chroma switch control		
03	RGB and FB tri-state	RGB gain			RGB switch control		Fast blanking mode/input selection	
Miscellaneous								
04	IT enable	SLB mode	Not used (see *Note 1*)	VCR-C output control	VCR-C gate control	RF trap filter control	RF adder control	TV R or C output selection
05	VCR slow blanking		TV slow blanking		ENC audio Input gain 0/6/9 dB		VCR R/C sub clamp	ENC R/C sub clamp
STB-BY								
06	RF outputs	TV outputs	CINCH outputs	VCR outputs	AUX inputs	TV inputs	VCR inputs	ENC inputs

Note: 1 Unused data must be set to "0".

Table 14. TV audio output

Reg. addr (hex)	Description	Bits	Data								Comments
			d7	**d6**	**d5**	**d4**	**d3**	**d2**	**d1**	**d0**	
00	Soft volume change	1	X X	X X	X X	X X	X X	X X	X X	0 1	Active Disabled
	Level adjustment	5	X X	X X	0 1	0 1	0 1	0 1	0 1	X X	0 dB -62 dB (-2 dB/step)
	6 dB extra gain	1	X X	0 1	X X	X X	X X	X X	X X	X X	0 dB +6 dB
	TV stereo or mono mode	1	0 1	X X	X X	X X	X X	X X	X X	X X	0 = stereo 1 = mono

Table 15. Audio selection & VCR audio output

Reg. addr (hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
01	TV & CINCH audio output selection	3	X	X	X	X	X	0	0	0	Muted
			X	X	X	X	X	0	0	1	Encoder L/R selected
			X	X	X	X	X	0	1	0	VCR L/R selected
			X	X	X	X	X	0	1	1	AUX L/R selected
			X	X	X	X	X	1	0	0	TV L/R selected
			X	X	X	X	X	1	0	1	Not allowed
			X	X	X	X	X	1	1	0	Not allowed
			X	X	X	X	X	1	1	1	Not allowed
	CINCH audio gain	1	X	X	X	X	0	X	X	X	0 dB
			X	X	X	X	1	X	X	X	Follow TV gain
	VCR audio output selection	2	X	X	0	0	X	X	X	X	Muted
			X	X	0	1	X	X	X	X	Encoder L/R selected
			X	X	1	0	X	X	X	X	TV L/R selected
			X	X	1	1	X	X	X	X	AUX L/R selected
	VCR stereo or mono mode	1	0	X	X	X	X	X	X	X	0 = stereo
			1	X	X	X	X	X	X	X	1 = mono

Table 16. TV & VCR video selection

Reg. addr (hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
02	TV video output selection	3	X	X	X	X	X	0	0	0	Y/CVBS muted & Chroma muted
			X	X	X	X	X	0	0	1	Y/CVBS_ENC & R/C_ENC
			X	X	X	X	X	0	1	0	Y_ENC & C_ENC
			X	X	X	X	X	0	1	1	Y/CVBS_VCR & R/C_VCR
			X	X	X	X	X	1	0	0	CVBS_AUX & Chroma muted
			X	X	X	X	X	1	0	1	Not allowed
			X	X	X	X	X	1	1	0	Not allowed
			X	X	X	X	X	1	1	1	Not allowed
	TV Chroma output control	1	X	X	X	X	0	X	X	X	Chroma defined by d2d1d0
			X	X	X	X	1	X	X	X	Chroma force to mute
	VCR video output selection	3	X	0	0	0	X	X	X	X	Y/CVBS muted & Chroma muted
			X	0	0	1	X	X	X	X	Y/CVBS_ENC & R/C_ENC
			X	0	1	0	X	X	X	X	Y_ENC & C_ENC
			X	0	1	1	X	X	X	X	CVBS_TV & Chroma muted
			X	1	0	0	X	X	X	X	CVBS_AUX & Chroma muted
			X	1	0	1	X	X	X	X	Not allowed
			X	1	1	0	X	X	X	X	Not allowed
			X	1	1	1	X	X	X	X	Not allowed
	VCR Chroma output control	1	0	X	X	X	X	X	X	X	Chroma defined by d6d5d4
			1	X	X	X	X	X	X	X	Chroma force to mute

Table 17. RGB & fast blanking outputs

Reg. addr (hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
03	Fast blanking control	2	X	X	X	X	X	X	0	0	FB forced to low level
			X	X	X	X	X	X	0	1	FB forced to high level
			X	X	X	X	X	X	1	0	FB from encoder
			X	X	X	X	X	X	1	1	FB from VCR
	RGB selection	2	X	X	X	X	0	0	X	X	Muted
			X	X	X	X	0	1	X	X	RGB_ENC selected
			X	X	X	X	1	0	X	X	RGB_VCR selected
			X	X	X	X	1	1	X	X	Not allowed
	RGB gain	2	X	X	0	0	X	X	X	X	+6 dB gain
			X	X	0	1	X	X	X	X	+5 dB gain
			X	X	1	0	X	X	X	X	+4 dB gain
			X	X	1	1	X	X	X	X	+3 dB gain
		1	X	0	X	X	X	X	X	X	+0 dB extra gain
			X	1	X	X	X	X	X	X	+3 dB for weak input signals
	RGB and fast blanking control	1	0	X	X	X	X	X	X	X	RGB and FB outputs high impedance state
			1	X	X	X	X	X	X	X	RGB and FB outputs active

Table 18. RF & miscellaneous control

Reg. addr (hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
04	R/C TV output selection	1	X	X	X	X	X	X	X	0	Red signal selected
			X	X	X	X	X	X	X	1	Chroma signal selected
	RF output: adder control and chroma sub-carrier filter selection	2	X	X	X	X	X	X	0	X	CVBS to RF output
			X	X	X	X	X	X	1	X	Y + C to RF output
			X	X	X	X	X	0	X	X	Filter not active
			X	X	X	X	X	1	X	X	Filter active
	C_Gate output control	1	X	X	X	X	0	X	X	X	High level
			X	X	X	X	1	X	X	X	Low level
	C_VCR output control	1	X	X	X	0	X	X	X	X	Tri-state mode (high impedance)
			X	X	X	1	X	X	X	X	Active
	Slow blanking mode	1	X	0	X	X	X	X	X	X	Normal mode
			X	1	X	X	X	X	X	X	SLB TV is driven by SLB VCR
	IT enable	1	0	X	X	X	X	X	X	X	No interrupt flag
			1	X	X	X	X	X	X	X	IT enable

Table 19. Slow blanking & inputs contro

Reg. addr (hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
05	Encoder R/Csub clamp	1	X X	X X	X X	X X	X X	X X	X X	0 1	Bottom level clamp Average level clamp
	VCR R/Csub clamp	1	X X	X X	X X	X X	X X	X X	0 1	X X	Bottom level clamp Average level clamp
	Encoder input level adjustment	2	X X X	X X X	X X X	X X X	0 0 1	0 1 0	X X X	X X X	0 dB for normal audio inputs +6 dB for weak audio inputs +9 dB for weak audio inputs
	Slow blanking TV SCART	2	X X X X	X X X X	0 0 1 1	0 1 0 1	X X X X	X X X X	X X X X	X X X X	Input mode only Output < 2 V Output 16/9 format Output 4/3 format
	Slow blanking VCR SCART	2	0 0 1 1	0 1 0 1	X X X X	X X X X	X X X X	X X X X	X X X X	X X X X	Input mode only Output < 2 V Output 16/9 format Output 4/3 format

Table 20. Standby modes

Reg. addr (hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
06	ENC inputs	1	X X	X X	X X	X X	X X	X X	X X	0 1	Inputs active Inputs disabled
	VCR inputs	1	X X	X X	X X	X X	X X	X X	0 1	X X	Inputs active Inputs disabled
	TV inputs	1	X X	X X	X X	X X	X X	0 1	X X	X X	Inputs active Inputs disabled
	AUX inputs	1	X X	X X	X X	X X	0 1	X X	X X	X X	Inputs active Inputs disabled
	VCR outputs	1	X X	X X	X X	0 1	X X	X X	X X	X X	Audio & video outputs ON Audio & video outputs OFF
	CINCH outputs	1	X X	X X	0 1	X X	X X	X X	X X	X X	Audio & video outputs ON Audio & video outputs OFF
	TV outputs	1	X X	0 1	X X	X X	X X	X X	X X	X X	Audio & video outputs ON Audio & video outputs OFF
	RFmod outputs	1	0 1	X X	X X	X X	X X	X X	X X	X X	Audio & video outputs ON Audio & video outputs OFF
	Full stop		1	1	1	1	1	1	1	1	Only I^2C bus and slow blanking detection parts are supplied.

Table 21. Output signals (read mode)

Reg. addr (hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
	Slow blanking TV SCART	2	X X X	X X X	X X X	X X X	X X X	X X X	0 1 1	1 0 1	Input <2 V Input 16/9 format Input 4/3 format
	Slow blanking VCR SCART	2	X X X	X X X	X X X	X X X	0 1 1	1 0 1	X X X	X X X	Input <2 V Input 16/9 format Input 4/3 format
	Interrupt flag	1	X X	X X	X X	0 1	X X	X X	X X	X X	No change since read One change has been detected (refer to *Note 1*)

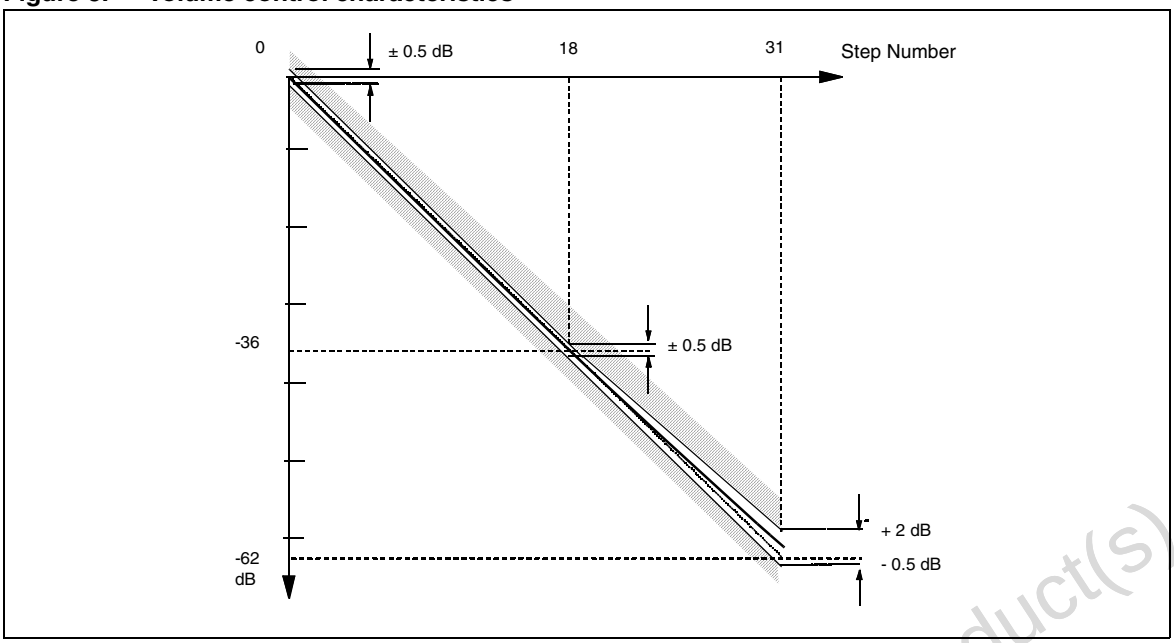
Note: 1 The interrupt flag will be cleared when this register is read. To prepare for a new interrupt, a "1" must be re-written in the IT enable bit (Reg. 04, d7).

3.2 Power-on reset — bus register initial conditions

Power-on reset is active when the supply V_{DD} is less than 3.5 volts.
Non-significant bits (X) are pre-set to "0"

Reg. addr (hex)	Data								Comments
	d7	d6	d5	d4	d3	d2	d1	d0	
00	0	0	0	0	0	0	0	0	Audio TV and cinch outputs are in stereo mode, 0 dB gain adjustment.
01	0	0	0	0	0	0	0	0	TV, cinch and VCR audio outputs are muted. VCR output is in stereo mode.
02	0	0	0	0	0	0	0	0	VCR, TV and RFmod video outputs are muted.
03	0	0	0	0	0	0	0	0	Fast blanking is forced to '0'. RGB outputs are muted and in high impedance.
04	0	0	0	0	0	0	0	0	C_GATE is high. C_VCR is high impedance.
05	0	0	0	0	0	0	0	0	Encoder and VCR R/Csub bottom level clamp, RGB outputs 6 dB gain, and slow blanking parts are in read mode.
06	0	0	0	0	0	0	0	0	All internal blocks are ON.

Figure 5. Volume control characteristics



4 Input/output groups

Figure 6. Bottom clamped video inputs (pins 2, 4, 6, 12, 14, 18, 21, 62, and 64)

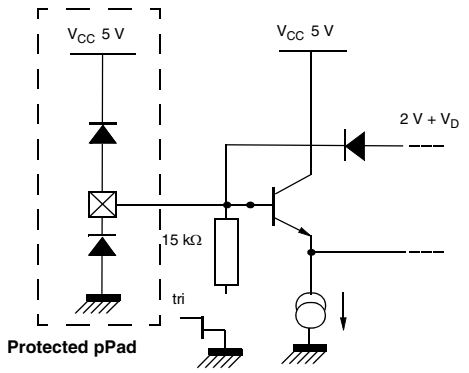


Figure 7. R/C clamped video inputs (pins 10 and 60

R/C inputs may be configured either as a bottom clamped input or as an average clamped input. In either case, the simplified input schematic is very close to one of the graphics shown above.

Figure 8. Fast blanking inputs (pins 50, 51)

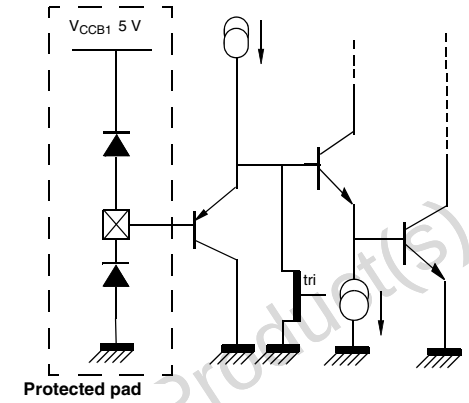


Figure 9. Average clamped video inputs (pin 8)

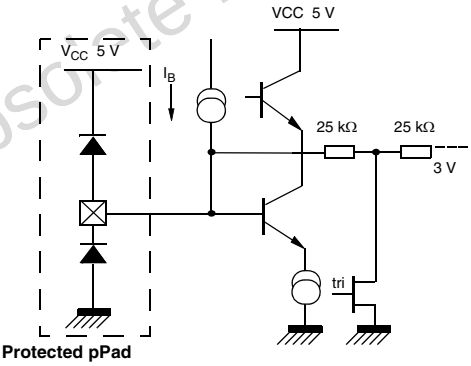


Figure 10. C gate logical output (pin 52)

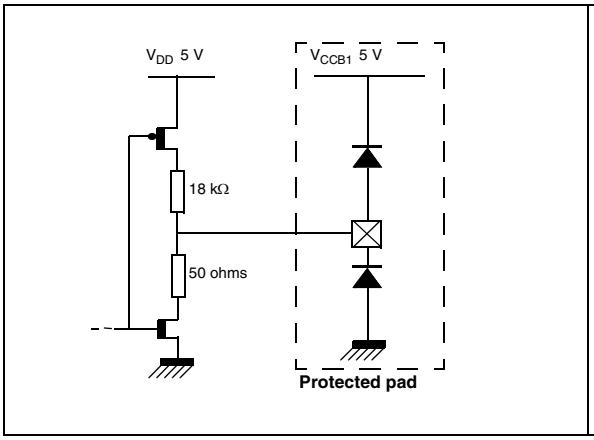


Figure 11. Fast blanking output (pin 49)

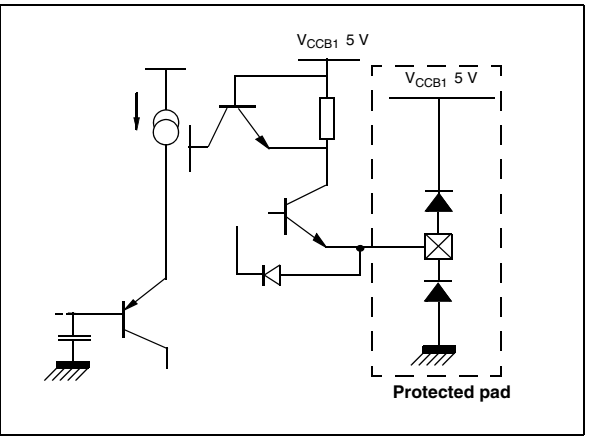


Figure 12. Video outputs (pins 38, 40, 42, 44, 46, 48)

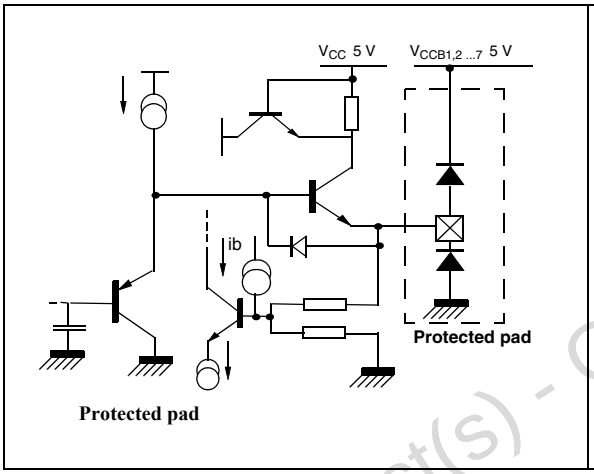


Figure 13. Audio inputs (pins 7, 9 11, 13, 19, 20, 22, 23)

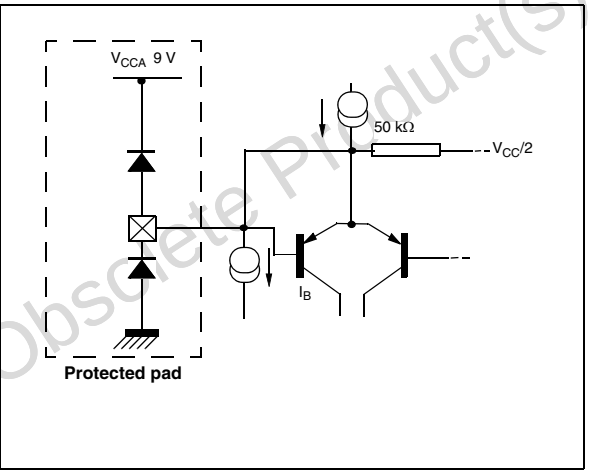


Figure 14. Slow blanking I/O (pins 59, 61)

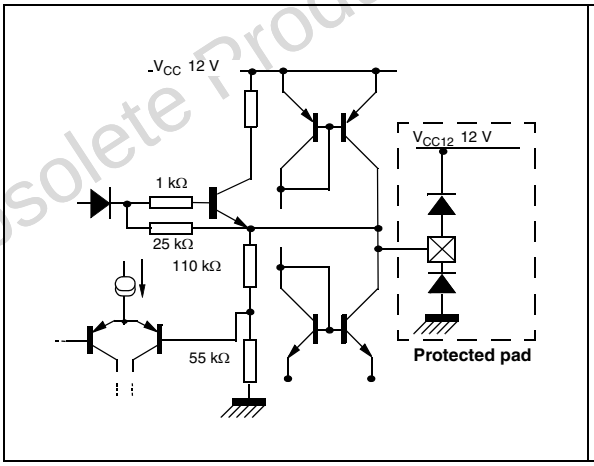


Figure 15. Trap filter (pin 34)

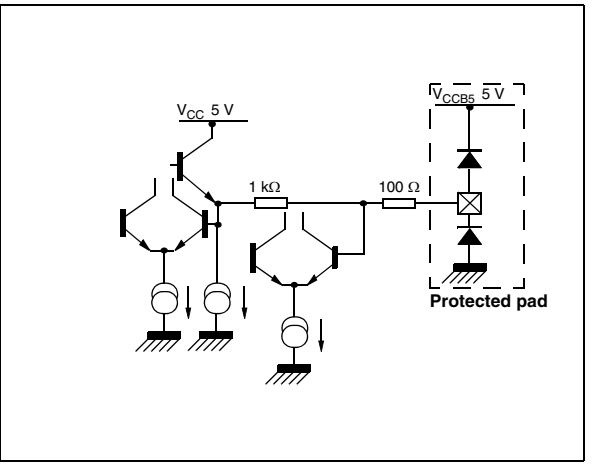


Figure 16. Audio outputs (pins 27, 28, 29, 30, 32, 33,35)

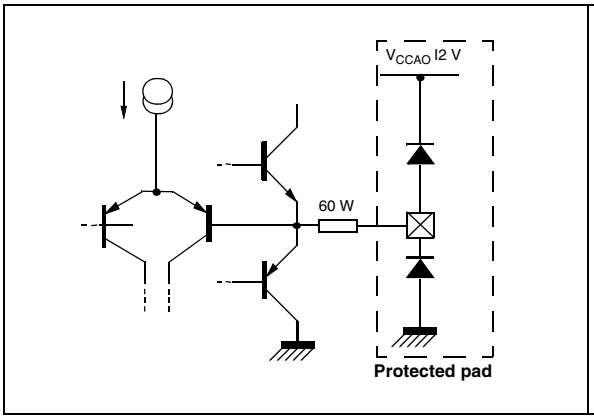


Figure 17. Interrupt output (pin 58)

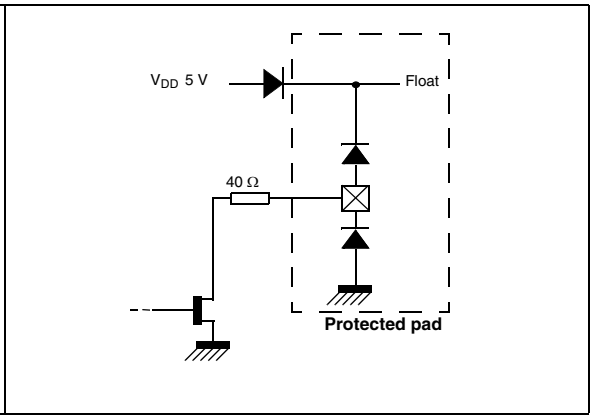


Figure 18. ^{2}C bus (SDA) (pin 56)

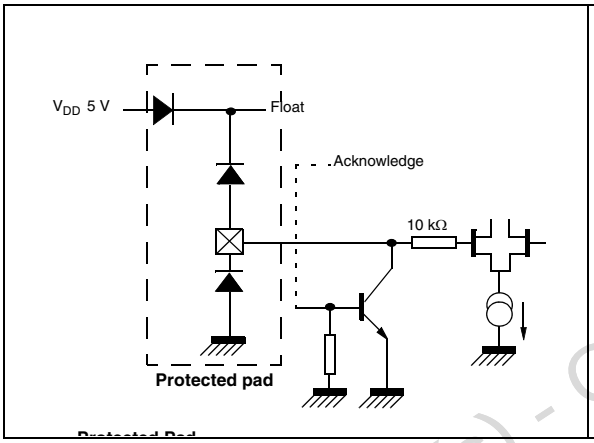


Figure 19. I^{2}C bus (ADD) (pin 54)

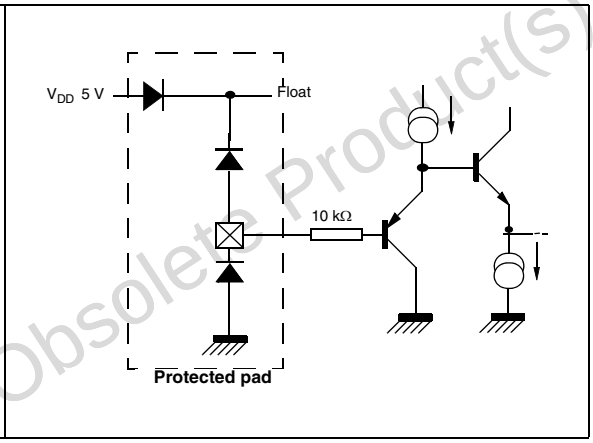


Figure 20. I²C bus (SCL) (pin 55)

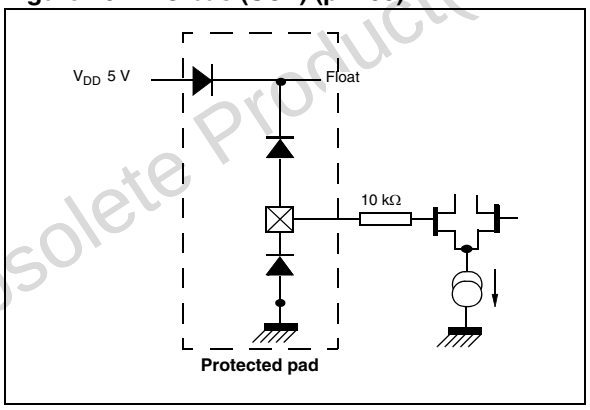
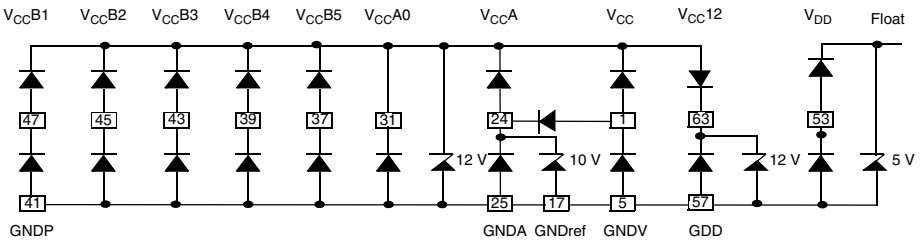


Figure 21. Power supply connection



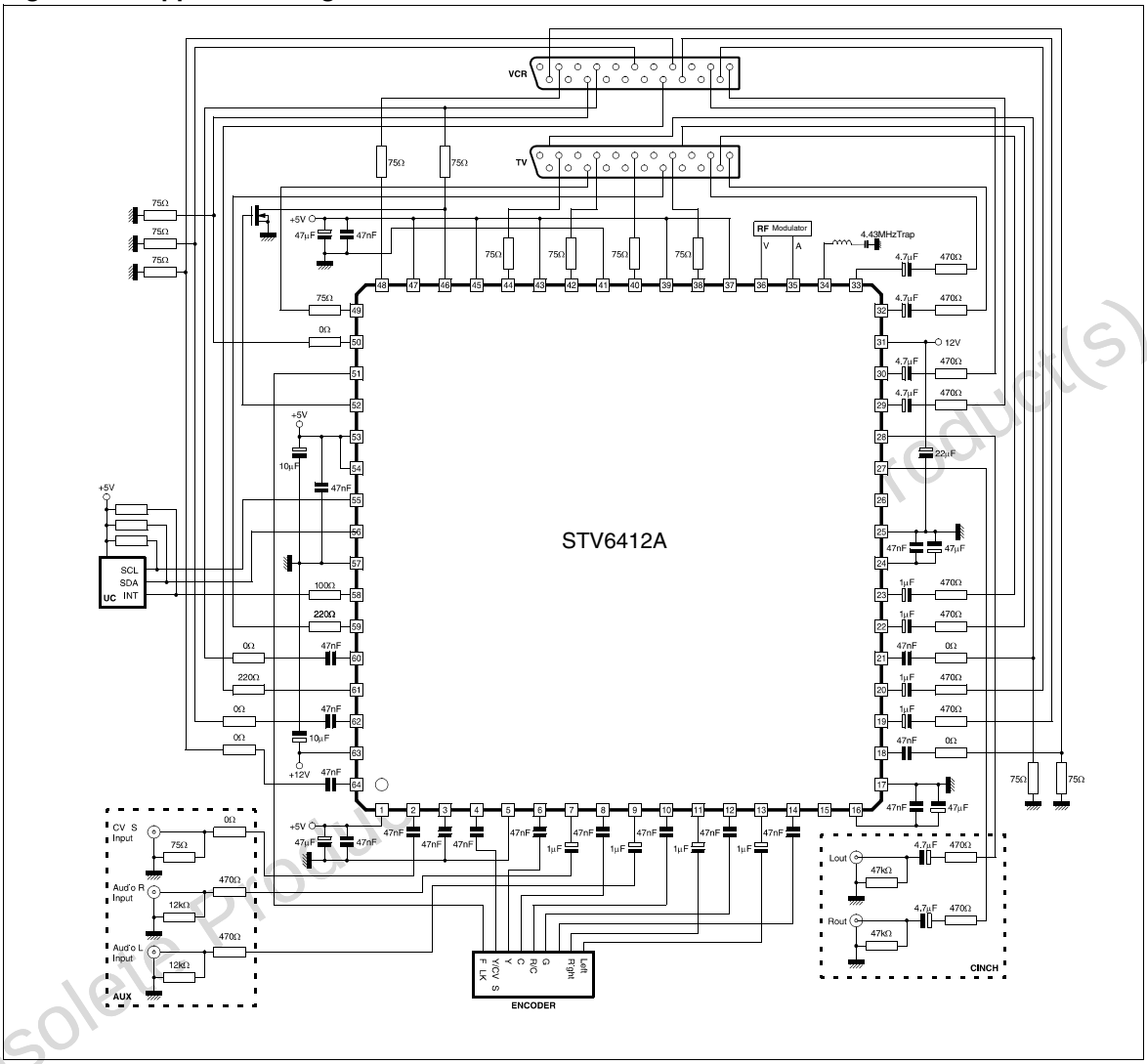
These symbols represent some huge diode and Zener-like components used for ESD protection of the device.

They are not supposed to be paths for any current in normal operation mode.

5 Application diagram

Note: The application diagram presented here is an example only and is subject to change without notice. The real application diagram will depend on application conditions and constraints.

Figure 22. Application diagram



For more details refer to the STV6412 Application Note.

6 Package mechanical data

Figure 23. 64 pin, LQFP64L (low-profile quad flat package) (14 x 14 x 1.4 mm)

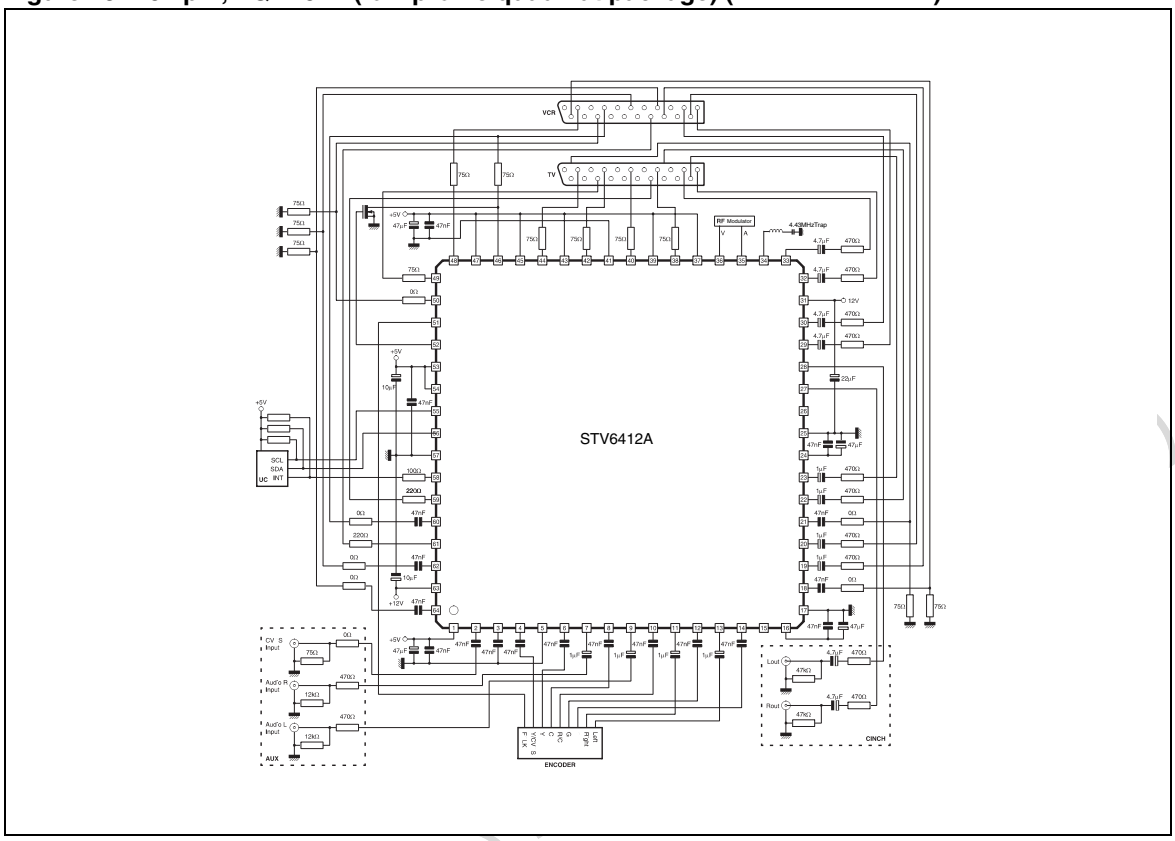


Table 22. LQFP64L package dimensions

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.30	0.37	0.45	0.0118	0.015	0.018
c	0.09		0.20	0.0035		0.0079
ccc			0.10			0.0039
D	15.80	16.00	16.20	0.622	0.630	0.638
D1	13.80	14.00	14.20	0.543	0.551	0.559
D3		12.00			0.472	
e		0.80			0.0315	
E	15.80	16.00	16.20	0.622	0.630	0.638

Table 22. LQFP64L package dimensions (continued)

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
E1	13.80	14.00	14.201	0.543	0.551	0.559
E3		12.00			0.472	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
Degrees						
k	0° minimum 3.5° typical 7° maximum					

7 Revision history

Table 23. Document revision history

Date	Revision	Changes
24-Jan-2006	1	Initial release.
24-Apr-2007	1.1	Reformatted to the new corporate template. Corrections to *Figure 22: Application diagram on page 27* and addition of application diagram disclaimer.
19-Jun-2007	1.2	Changed package type from TQFP64 to LQFP64L. Updated *Figure 23: 64 pin, LQFP64L (low-profile quad flat package) (14 x 14 x 1.4 mm) on page 28*. Updated *Table 22: LQFP64L package dimensions on page 28*.
10-Jul-2007	1.3	Minor corrections.
02-Sep-2009	2	Minor corrections.

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