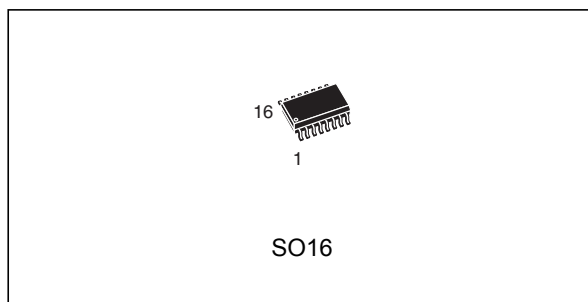


**3 V NVRAM supervisor for LPSRAM**

Datasheet - production data

**Features**

- Convert low power SRAMs into NVRAMs
- 3 V operating voltage
- Precision power monitoring and power switching circuitry
- Automatic write-protection when  $V_{CC}$  is out-of-tolerance
- Choice of supply voltage and power-fail deselect voltage:
  - $V_{CC} = 2.7$  to  $3.6$  V;  $2.55$  V  $\leq V_{PFD} \leq 2.70$  V
- Reset output ( $\overline{RST}$ ) for power on reset
- 1.25 V reference (for PFI/ $\overline{PFO}$ )
- Less than 15 ns chip enable access propagation delay
- Battery low pin ( $\overline{BL}$ )
- RoHS compliant
  - Lead-free second level interconnect

**Description**

The M40SZ100W NVRAM controller is a self-contained device which converts a standard low-power SRAM into a non-volatile memory. A precision voltage reference and comparator monitors the  $V_{CC}$  input for an out-of-tolerance condition.

When an invalid  $V_{CC}$  condition occurs, the conditioned chip enable output ( $\overline{E_{CON}}$ ) is forced inactive to write protect the stored data in the SRAM. During a power failure, the SRAM is switched from the  $V_{CC}$  pin to the external battery to provide the energy required for data retention. On a subsequent power-up, the SRAM remains write-protected until a valid power condition returns.

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# 1 Device overview

Figure 1. Logic diagram

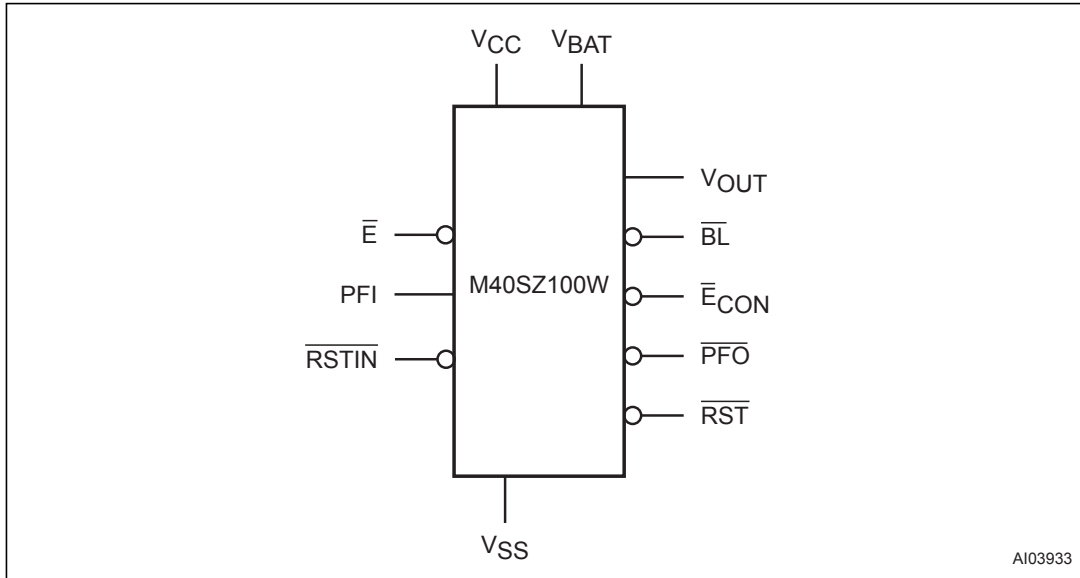


Table 1. Signal names

$\bar{E}$	Chip enable input
$\bar{E}_{CON}$	Conditioned chip enable output
$\bar{RST}$	Reset output (open drain)
$\bar{RSTIN}$	Reset input
$\bar{BL}$	Battery low output (open drain)
$V_{OUT}$	Supply voltage output
$V_{CC}$	Supply voltage
$V_{BAT}$	Backup supply voltage
PFI	Power fail input
$\bar{PFO}$	Power fail output
$V_{SS}$	Ground
NC	Not connected internally

Figure 2. Pin connections

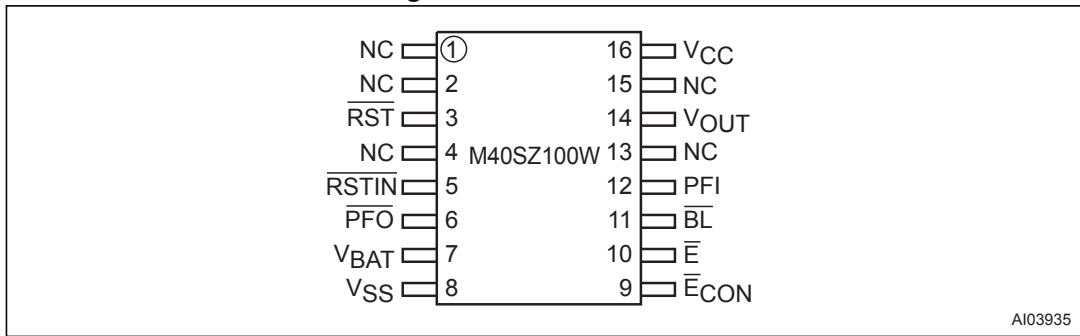
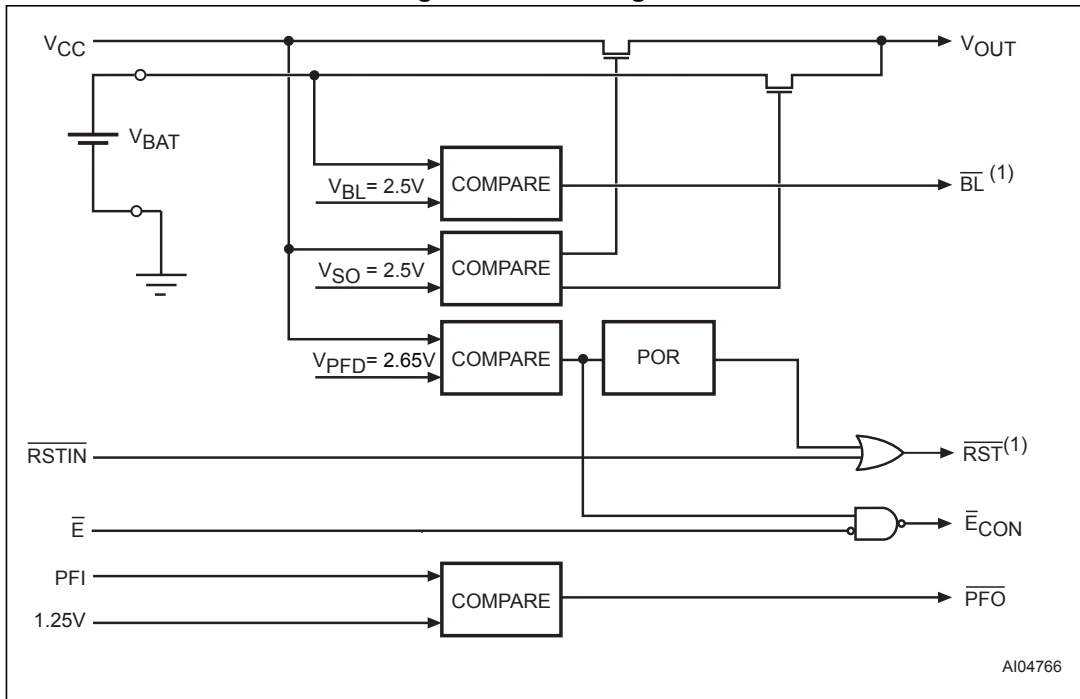
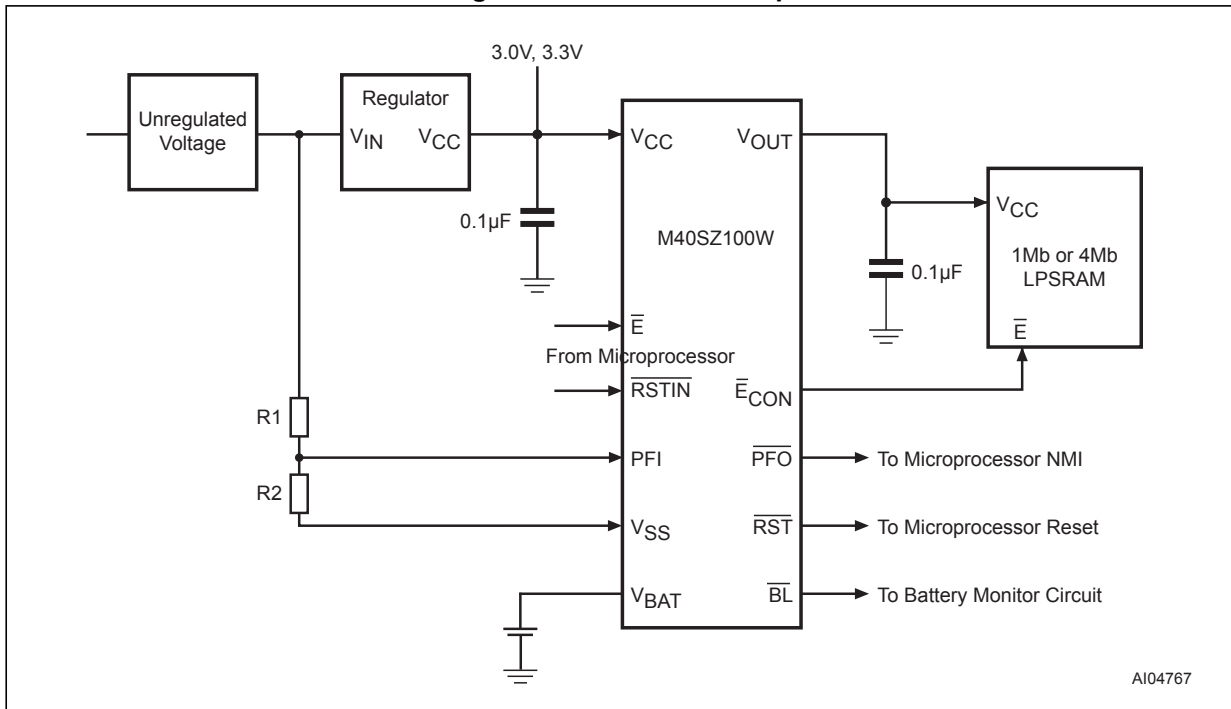


Figure 3. Block diagram



1. Open drain output

Figure 4. Hardware hookup



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## 2 Operation

The M40SZ100W, as shown in [Figure 4 on page 7](#), can control one (two, if placed in parallel) standard low-power SRAM. This SRAM must be configured to have the chip enable input disable all other input signals. Most slow, low-power SRAMs are configured like this, however many fast SRAMs are not. During normal operating conditions, the conditioned chip enable ( $\overline{E}_{CON}$ ) output pin follows the chip enable ( $\overline{E}$ ) input pin with timing shown in [Table 2 on page 10](#). An internal switch connects  $V_{CC}$  to  $V_{OUT}$ . This switch has a voltage drop of less than 0.3 V ( $I_{OUT1}$ ).

When  $V_{CC}$  degrades during a power failure,  $\overline{E}_{CON}$  is forced inactive independent of  $\overline{E}$ . In this situation, the SRAM is unconditionally write protected as  $V_{CC}$  falls below an out-of-tolerance threshold ( $V_{PFD}$ ). For the M40SZ100W the power fail detection value associated with  $V_{PFD}$  is shown in [Table 7 on page 16](#).

If chip enable access is in progress during a power fail detection, that memory cycle continues to completion before the memory is write protected. If the memory cycle is not terminated within time  $t_{WPT}$ ,  $\overline{E}_{CON}$  is unconditionally driven high, write protecting the SRAM. A power failure during a WRITE cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the SRAM's contents. At voltages below  $V_{PFD}(\min)$ , the user can be assured the memory will be write protected within the Write Protect Time ( $t_{WPT}$ ) provided the  $V_{CC}$  fall time does not exceed  $t_F$  (see [Table 2 on page 10](#)).

As  $V_{CC}$  continues to degrade, the internal switch disconnects  $V_{CC}$  and connects the internal battery to  $V_{OUT}$ . This occurs at the switchover voltage ( $V_{SO}$ ). Below the  $V_{SO}$ , the battery provides a voltage  $V_{OHB}$  to the SRAM and can supply current  $I_{OUT2}$  (see [Table 7 on page 16](#)).

When  $V_{CC}$  rises above  $V_{SO}$ ,  $V_{OUT}$  is switched back to the supply voltage. Output  $\overline{E}_{CON}$  is held inactive for  $t_{CEB}$  (120 ms maximum) after the power supply has reached  $V_{PFD}$ , independent of the  $\overline{E}$  input, to allow for processor stabilization (see [Figure 6 on page 10](#)).

### 2.1 Data retention lifetime calculation

Most low power SRAMs on the market today can be used with the M40SZ100W NVRAM controller. There are, however some criteria which should be used in making the final choice of which SRAM to use. The SRAM must be designed in a way where the chip enable input disables all other inputs to the SRAM. This allows inputs to the M40SZ100W and SRAMs to be "Don't care" once  $V_{CC}$  falls below  $V_{PFD}(\min)$  (see [Figure 5 on page 9](#)). The SRAM should also guarantee data retention down to  $V_{CC} = 2.0$  V. The chip enable access time must be sufficient to meet the system needs with the chip enable propagation delays included.

If data retention lifetime is a critical parameter for the system, it is important to review the data retention current specifications for the particular SRAMs being evaluated. Most SRAMs specify a data retention current at 3.0 V. Manufacturers generally specify a typical condition for room temperature along with a worst case condition (generally at elevated temperatures). The system level requirements will determine the choice of which value to use. The data retention current value of the SRAMs can then be added to the  $I_{CCDR}$  value of the M40SZ100W to determine the total current requirements for data retention.

**Caution:** Take care to avoid inadvertent discharge through  $V_{OUT}$  and  $\overline{E}_{CON}$  after battery has been attached.



For a further more detailed review of lifetime calculations, please see application note AN1012.

Figure 5. Power-down timing

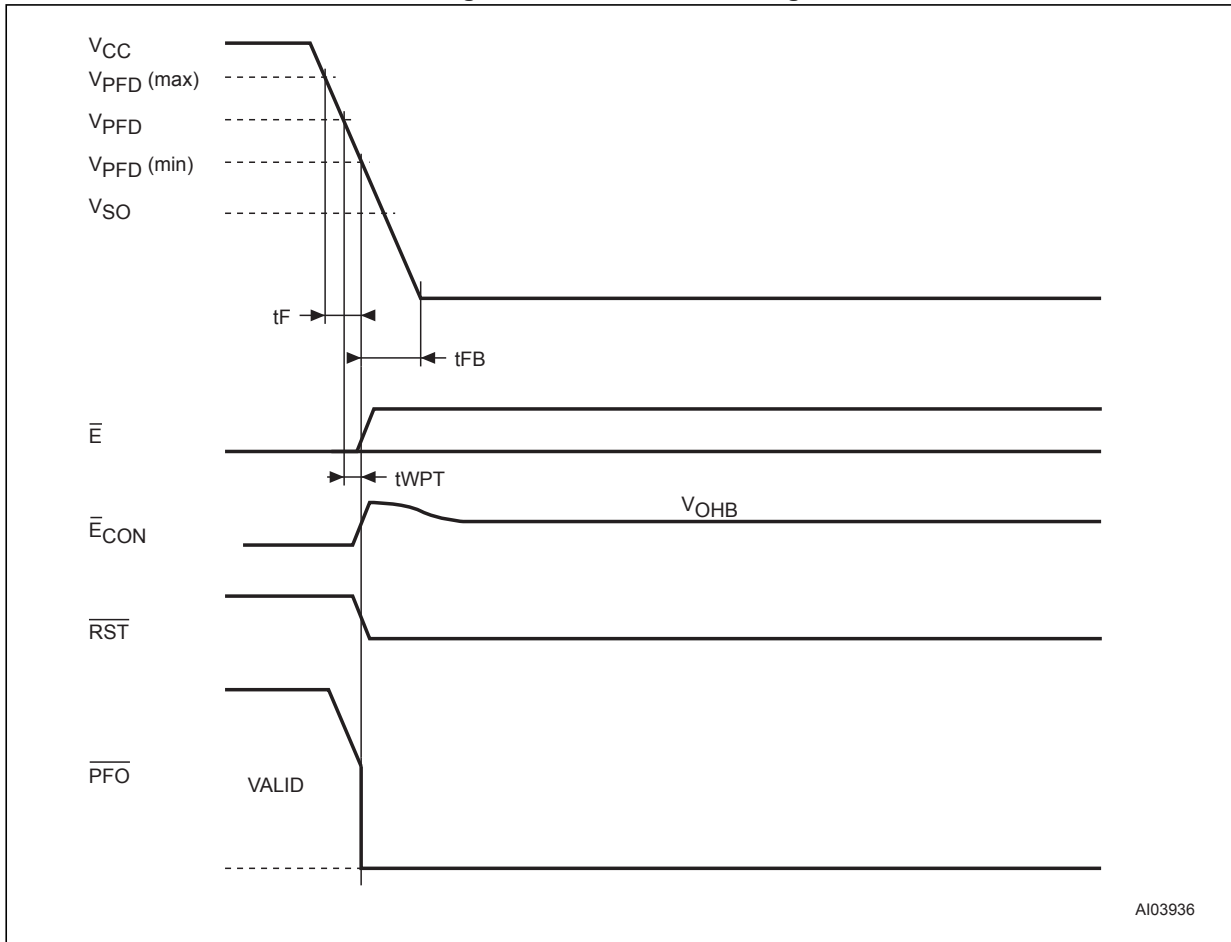
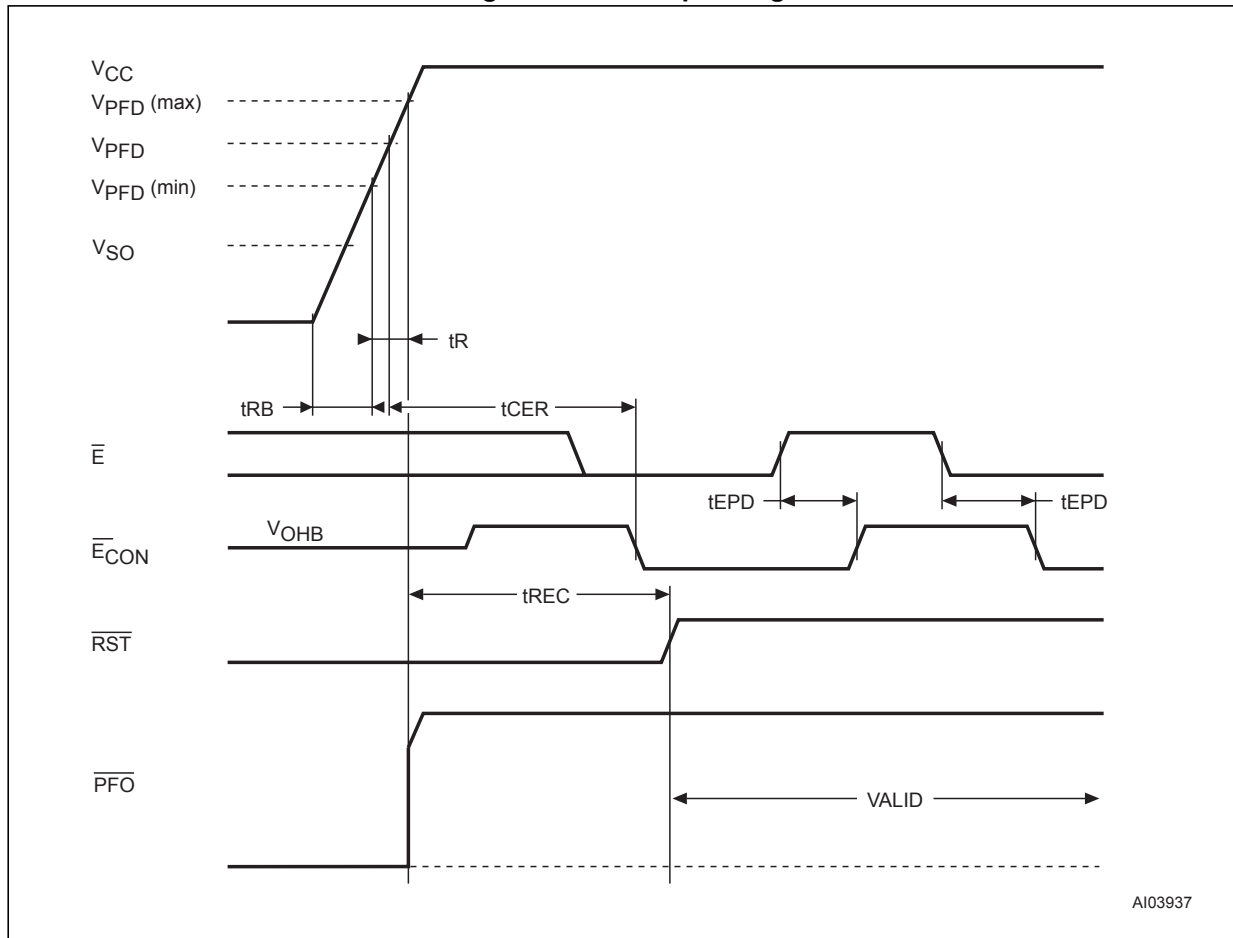


Figure 6. Power-up timing



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Table 2. Power-down/up AC characteristics

Symbol	Parameter <sup>(1)</sup>	Min	Max	Unit
$t_F^{(2)}$	$V_{PFD}(\max)$ to $V_{PFD}(\min)$ $V_{CC}$ fall time	300		$\mu s$
$t_{FB}^{(3)}$	$V_{PFD}(\min)$ to $V_{SS}$ $V_{CC}$ fall time	10		$\mu s$
$t_{PFD}$	PFI to $\bar{PFO}$ propagation delay	15	25	$\mu s$
$t_R$	$V_{PFD}(\min)$ to $V_{PFD}(\max)$ $V_{CC}$ rise time	10		$\mu s$
$t_{EPD}$	Chip enable propagation delay (low or high)		15	ns
$t_{RB}$	$V_{SS}$ to $V_{PFD}(\min)$ $V_{CC}$ rise time	1		$\mu s$
$t_{CER}$	Chip enable recovery	40	120	ms
$t_{REC}$	$V_{PFD}(\max)$ to $\bar{RST}$ high	40	200	ms
$t_{WPT}$	Write protect time	40	200	$\mu s$

- Valid for ambient operating temperature:  $T_A = -40$  to  $85$  °C;  $V_{CC} = 2.7$  to  $3.6$  V (except where noted).
- $V_{PFD}(\max)$  to  $V_{PFD}(\min)$  fall time of less than  $t_F$  may result in deselection/write protection not occurring until  $200$   $\mu s$  after  $V_{CC}$  passes  $V_{PFD}(\min)$ .
- $V_{PFD}(\min)$  to  $V_{SS}$  fall time of less than  $t_{FB}$  may cause corruption of RAM data.

## 2.2 Power-on reset output

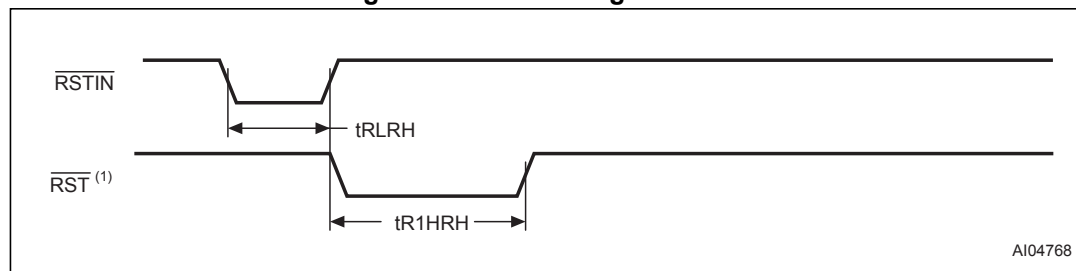
All microprocessors have a reset input which forces them to a known state when starting. The M40SZ100W has a reset output ( $\overline{\text{RST}}$ ) pin which is guaranteed to be low by  $V_{\text{PFD}}$  (see [Table 7 on page 16](#)). This signal is an open drain configuration. An appropriate pull-up resistor to  $V_{\text{CC}}$  should be chosen to control the rise time. This signal will be valid for all voltage conditions, even when  $V_{\text{CC}}$  equals  $V_{\text{SS}}$  (with valid battery voltage).

Once  $V_{\text{CC}}$  exceeds the power failure detect voltage  $V_{\text{PFD}}$ , an internal timer keeps  $\overline{\text{RST}}$  low for  $t_{\text{REC}}$  to allow the power supply to stabilize.

## 2.3 Reset input ( $\overline{\text{RSTIN}}$ )

The M40SZ100W provides one independent input which can generate an output reset. The duration and function of this reset is identical to a reset generated by a power cycle. [Table 3](#) and [Figure 7](#) illustrate the AC reset characteristics of this function. Pulses shorter than  $t_{\text{RLRH}}$  will not generate a reset condition.  $\overline{\text{RSTIN}}$  is internally pulled up to  $V_{\text{CC}}$  through a 100 k $\Omega$  resistor.

Figure 7.  $\overline{\text{RSTIN}}$  timing waveform



1. With pull-up resistor

Table 3. Reset AC characteristics

Symbol	Parameter <sup>(1)</sup>	Min	Max	Unit
$t_{\text{RLRH}}^{(2)}$	RSTIN low to RSTIN high	200		ns
$t_{\text{R1HRH}}^{(3)}$	RSTIN high to RST high	40	200	ms

- Valid for ambient operating temperature:  $T_A = -40$  to  $85$  °C;  $V_{\text{CC}} = 2.7$  to  $3.6$  V (except where noted).
- Pulse width less than 50 ns will result in no RESET (for noise immunity).
- $C_L = 50$  pF (see [Figure 9 on page 15](#)).

## 2.4 Battery low pin

The M40SZ100W automatically performs battery voltage monitoring upon power-up, and at factory-programmed time intervals of at least 24 hours. The Battery Low ( $\overline{\text{BL}}$ ) pin will be asserted if the battery voltage is found to be less than approximately 2.5 V. The  $\overline{\text{BL}}$  pin will remain asserted until completion of battery replacement and subsequent battery low monitoring tests, either during the next power-up sequence or the next scheduled 24-hour interval.

If a battery low is generated during a power-up sequence, this indicates that the battery is below 2.5 V and may not be able to maintain data integrity in the SRAM. Data should be considered suspect, and verified as correct. A fresh battery should be installed.

If a battery low indication is generated during the 24-hour interval check, this indicates that the battery is near end of life. However, data is not compromised due to the fact that a nominal  $V_{CC}$  is supplied. In order to insure data integrity during subsequent periods of battery back-up mode, the battery should be replaced.

The M40SZ100W only monitors the battery when a nominal  $V_{CC}$  is applied to the device. Thus applications which require extensive durations in the battery backup mode should be powered-up periodically (at least once every few months) in order for this technique to be beneficial. Additionally, if a battery low is indicated, data integrity should be verified upon power-up via a checksum or other technique. The  $\overline{BL}$  pin is an open drain output and an appropriate pull-up resistor to  $V_{CC}$  should be chosen to control the rise time.

## 2.5 Power-fail input/output

The power-fail input (PFI) is compared to an internal reference voltage (independent from the  $V_{PFD}$  comparator). If PFI is less than the power-fail threshold ( $V_{PFI}$ ), the power-fail output (PFO) will go low. This function is intended for use as an undervoltage detector to signal a failing power supply. Typically PFI is connected through an external voltage divider (see [Figure 4 on page 7](#)) to either the unregulated DC input (if it is available) or the regulated output of the  $V_{CC}$  regulator. The voltage divider can be set up such that the voltage at PFI falls below  $V_{PFI}$  several milliseconds before the regulated  $V_{CC}$  input to the M40SZ100W or the microprocessor drops below the minimum operating voltage.

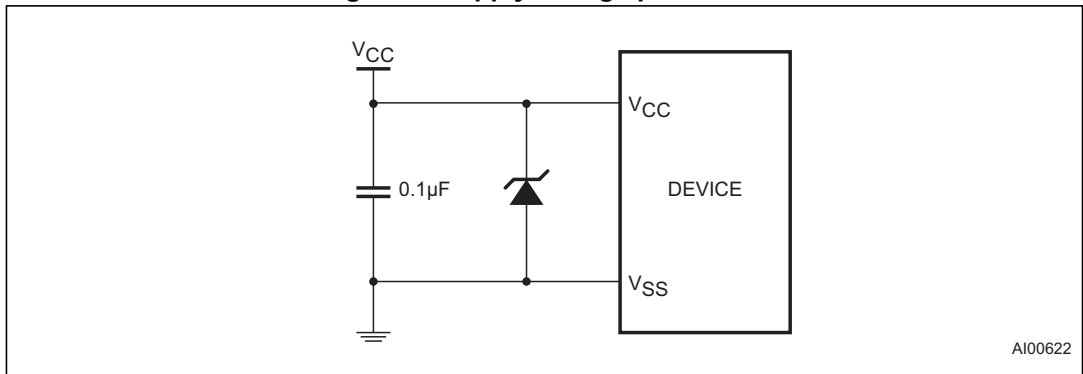
During battery backup, the power-fail comparator turns off and  $\overline{PFO}$  goes (or remains) low. This occurs after  $V_{CC}$  drops below  $V_{PFD}(\min)$ . When power returns,  $\overline{PFO}$  is forced high, irrespective of  $V_{PFI}$  for the write protect time ( $t_{REC}$ ), which is the time from  $V_{PFD}(\max)$  until the inputs are recognized. At the end of this time, the power-fail comparator is enabled and  $\overline{PFO}$  follows PFI. If the comparator is unused, PFI should be connected to  $V_{SS}$  and  $\overline{PFO}$  left unconnected.

## 2.6 $V_{CC}$ noise and negative going transients

$I_{CC}$  transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the  $V_{CC}$  bus. These transients can be reduced if capacitors are used to store energy which stabilizes the  $V_{CC}$  bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1  $\mu\text{F}$  (as shown in [Figure 8 on page 13](#)) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on  $V_{CC}$  that drive it to values below  $V_{SS}$  by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, STMicroelectronics recommends connecting a Schottky diode from  $V_{CC}$  to  $V_{SS}$  (cathode connected to  $V_{CC}$ , anode to  $V_{SS}$ ). Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount.

Figure 8. Supply voltage protection



### 3 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$T_{STG}$	Storage temperature ( $V_{CC}$ off)	-55 to 125	°C
$T_{SLD}^{(1)}$	Lead solder temperature for 10 seconds	260	°C
$V_{IO}$	Input or output voltages	-0.3 to $V_{CC} + 0.3$	V
$V_{CC}$	Supply voltage	-0.3 to 4.6	V
$I_O$	Output current	20	mA
$P_D$	Power dissipation	1	W

1. For SO package, Lead-free (Pb-free) lead finish: reflow at peak temperature of 260 °C (the time above 255 °C must not exceed 30 seconds).

**Caution:** Negative undershoots below -0.3 V are not allowed on any pin while in the battery backup mode.

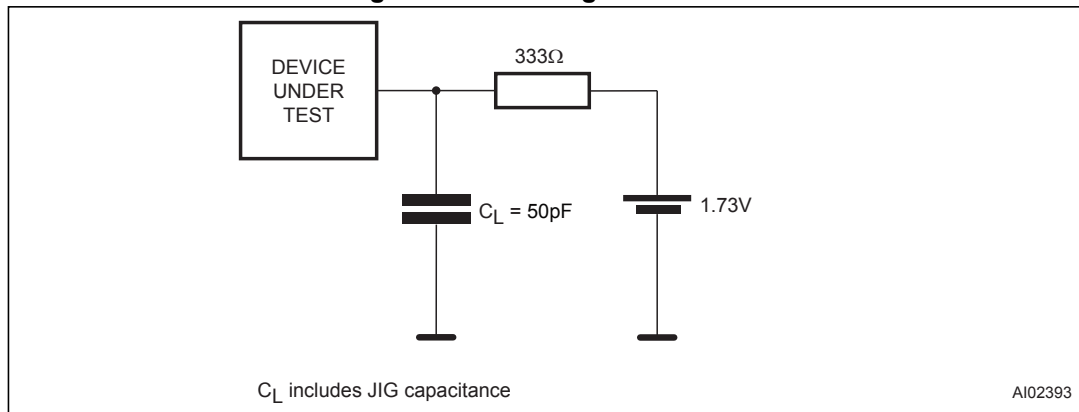
## 4 DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC characteristic tables are derived from tests performed under the measurement conditions listed in [Table 5: DC and AC measurement conditions](#). Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

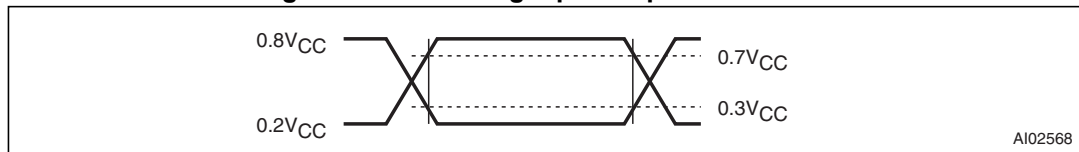
**Table 5. DC and AC measurement conditions**

Parameter	Value
V <sub>CC</sub> supply voltage	2.7 to 3.6 V
Ambient operating temperature	-40 to 85 °C
Load capacitance (C <sub>L</sub> )	50 pF
Input rise and fall times	≤ 5 ns
Input pulse voltages	0.2 to 0.8V <sub>CC</sub>
Input and output timing ref. voltages	0.3 to 0.7V <sub>CC</sub>

**Figure 9. AC testing load circuit**



**Figure 10. AC testing input/output waveforms**



**Table 6. Capacitance**

Symbol	Parameter <sup>(1)(2)</sup>	Min	Max	Unit
C <sub>IN</sub>	Input capacitance	-	7	pF
C <sub>OUT</sub> <sup>(3)</sup>	Output capacitance	-	10	pF

1. Sampled only, not 100% tested.
2. At 25 °C, f = 1 MHz.
3. Outputs deselected.

Table 7. DC characteristics

Sym	Parameter	Test condition <sup>(1)</sup>	Min	Typ	Max	Unit
I <sub>CC</sub>	Supply current	Outputs open			0.5	mA
I <sub>CCDR</sub>	Data retention mode current <sup>(2)</sup>			50	200	nA
I <sub>LI</sub> <sup>(3)</sup>	Input leakage current	$0\text{ V} \leq V_{IN} \leq V_{CC}$			±1	µA
	Input leakage current (PFI)		-25	2	25	nA
I <sub>LO</sub> <sup>(4)</sup>	Output leakage current	$0\text{ V} \leq V_{OUT} \leq V_{CC}$			±1	µA
I <sub>OUT1</sub> <sup>(5)</sup>	V <sub>OUT</sub> current (active)	$V_{OUT} > V_{CC} - 0.3$			100	mA
I <sub>OUT2</sub>	V <sub>OUT</sub> current (battery backup)	$V_{OUT} > V_{BAT} - 0.3$			100	µA
V <sub>BAT</sub>	Battery voltage		2.5	3.0	3.5 <sup>(6)</sup>	V
V <sub>IH</sub>	Input high voltage		$0.7V_{CC}$		$V_{CC} + 0.3$	V
V <sub>IL</sub>	Input low voltage		-0.3		$0.3V_{CC}$	V
V <sub>OH</sub>	Output high voltage <sup>(6)</sup>	I <sub>OH</sub> = -1.0 mA	2.4			V
V <sub>OHB</sub>	V <sub>OH</sub> battery backup <sup>(7)</sup>	I <sub>OUT2</sub> = -1.0 µA	2.5	2.9	3.5	V
V <sub>OL</sub>	Output low voltage	I <sub>OL</sub> = 3.0 mA			0.4	V
	Output low voltage (open drain) <sup>(8)</sup>	I <sub>OL</sub> = 10 mA			0.4	V
V <sub>PFD</sub>	Power-fail deselect voltage		2.55	2.60	2.70	V
V <sub>PFI</sub>	PFI input threshold	V <sub>CC</sub> = 3 V	1.225	1.250	1.275	V
	PFI hysteresis	PFI rising		20	70	mV
V <sub>SO</sub>	Battery backup switchover voltage			2.5		V

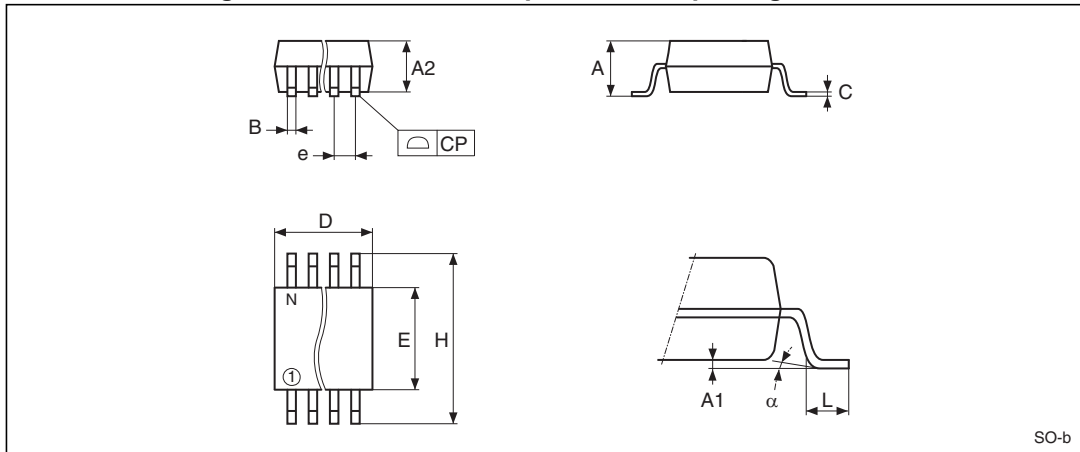
1. Valid for ambient operating temperature: T<sub>A</sub> = -40 to 85 °C; V<sub>CC</sub> = 2.7 to 3.6 V (except where noted).
2. Measured with V<sub>OUT</sub> and  $\overline{E}_{CON}$  open.
3.  $\overline{RSTIN}$  internally pulled-up to V<sub>CC</sub> through 100 kΩ resistor.
4. Outputs deselected.
5. External SRAM must match SUPERVISOR chip V<sub>CC</sub> specification.
6. For  $\overline{PFO}$  pin (CMOS).
7. Chip enable output ( $\overline{E}_{CON}$ ) can only sustain CMOS leakage currents in the battery backup mode. Higher leakage currents will reduce battery life.
8. For  $\overline{RST}$  &  $\overline{BL}$  pins (open drain).



## 5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

**Figure 11. SO16 – 16-lead plastic small package outline**



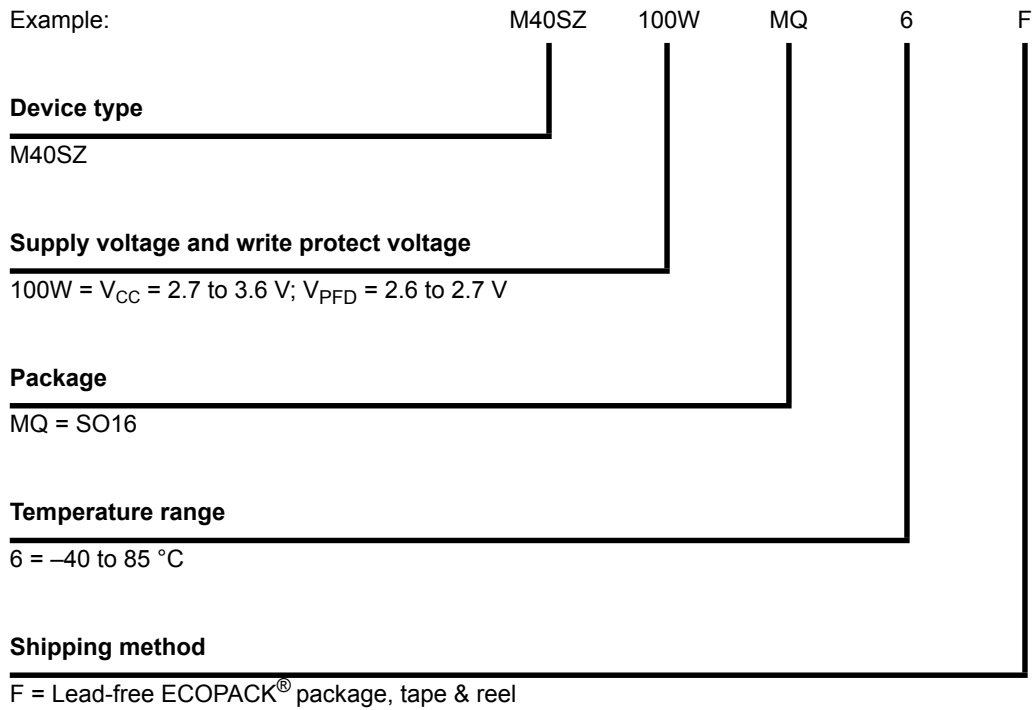
Note: Drawing is not to scale.

**Table 8. SO16 – 16-lead plastic small outline package mechanical data**

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.75			0.069
A1		0.10	0.25		0.004	0.010
A2			1.60			0.063
B		0.35	0.46		0.014	0.018
C		0.19	0.25		0.007	0.010
D		9.80	10.00		0.386	0.394
E		3.80	4.00		0.150	0.158
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
L		0.40	1.27		0.016	0.050
a		0°	8°		0°	8°
N	16			16		
CP			0.10			0.004

## 6 Part numbering

Table 9. Ordering information scheme



For a list of available options (e.g., speed, package) or for further information on any aspect of this device, please contact the ST sales office nearest to you.

## 7 Revision history

**Table 10. Document revision history**

Date	Revision	Changes
Dec-2001	1.0	First issue
13-May-2002	1.1	Modify reflow time and temperature footnote ( <a href="#">Table 4</a> )
01-Aug-2002	1.2	Add marketing status (cover page; <a href="#">Table 9</a> )
15-Sep-2003	1.3	Remove reference to M68xxx (obsolete) part ( <a href="#">Figure 4</a> ); update disclaimer
20-Nov-2007	2	Reformatted document; added lead-free second level interconnect information to cover page and <a href="#">Section 5: Package mechanical data</a> ; updated <a href="#">Table 4</a> and <a href="#">9</a> .
25-Oct-2010	3	Updated cover page, <a href="#">Section 3</a> , <a href="#">Table 9</a> , ECOPACK <sup>®</sup> text in <a href="#">Section 5</a> ; reformatted document; minor textual changes.
16-Dec-2013	4	Removed SNAPHAT and SOH28 package option as well as 5 V part (M40SZ100Y) from datasheet Removed shipping option in tubes from <a href="#">Table 9</a>

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