AM26C32 Quadruple Differential Line Receiver

Check for Samples: AM26C32

FEATURES

- **Meets or Exceeds the Requirements of ANSI TIA/EIA-422-B, TIA/EIA-423-B, and ITU Recommendation V.10 and V.11**
- **Low Power, I_{CC} = 10 mA Typ**
- **±7-V Common-Mode Range With ±200-mV Sensitivity**
- **Input Hysteresis: 60 mV Typ**
- **t_{pd} = 17 ns Typ**
- **Operates From a Single 5-V Supply**
- **3-State Outputs**
- **Input Fail-Safe Circuitry**
- **Improved Replacements for AM26LS32 Device**
- **Available in Q-Temp Automotive**
- **On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.**

APPLICATIONS

- **High-Reliability Automotive Applications**
- **Configuration Control/Print Support**
- **Qualification to Automotive Standards**

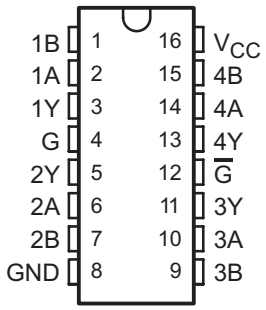
DESCRIPTION

The AM26C32 device is a quadruple differential line receiver for balanced or unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. The 3-state outputs permit connection directly to a bus-organized system. Fail-safe design specifies that if the inputs are open, the outputs always are high.

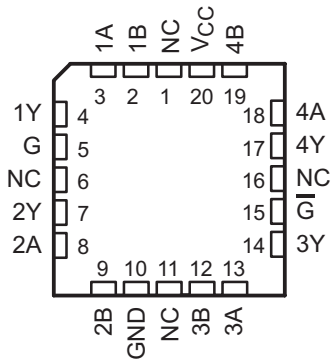
The AM26C32 devices are manufactured using a BiCMOS process, which is a combination of bipolar and CMOS transistors. This process provides the high voltage and current of bipolar with the low power of CMOS to reduce the power consumption to about one-fifth that of the standard AM26LS32, while maintaining ac and dc performance.

The AM26C32C device is characterized for operation from 0°C to 70°C. The AM26C32I device is characterized for operation from −40°C to 85°C. The AM26C32Q is characterized for operation from −40°C to 125°C. The AM26C32M device is characterized for operation over the full military temperature range of −55°C to 125°C.

AM26C32C . . . D, N, OR NS PACKAGE
AM26C32I . . . D, N , NS, OR PW PACKAGE
AM26C32Q . . . D PACKAGE
AM26C32M . . . J OR W PACKAGE
(TOP VIEW)



AM26C32M . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

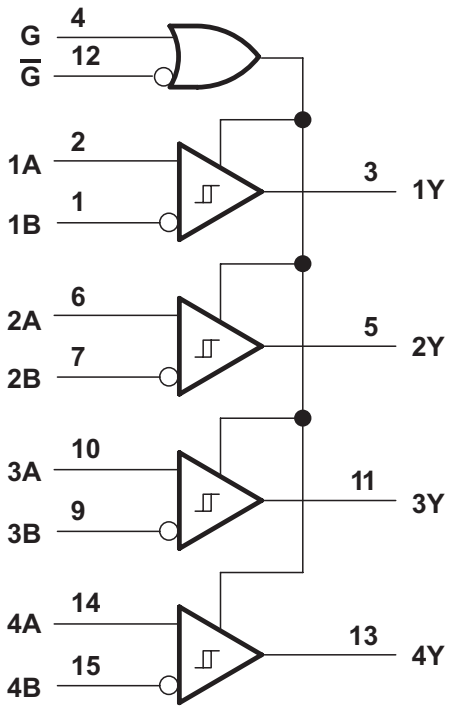
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Function Table (Each Driver)(1)

DIFFERENTIAL INPUT	ENABLES		OUTPUT
	G	$\overline{G}$	Y
$V_{ID} \geq V_{IT+}$	H	X	H
	X	L	H
$V_{IT} < V_{ID} < V_{IT+}$	H	X	?
	X	L	?
$V_{ID} \leq V_{IT-}$	H	X	L
	X	L	L
X	L	H	Z

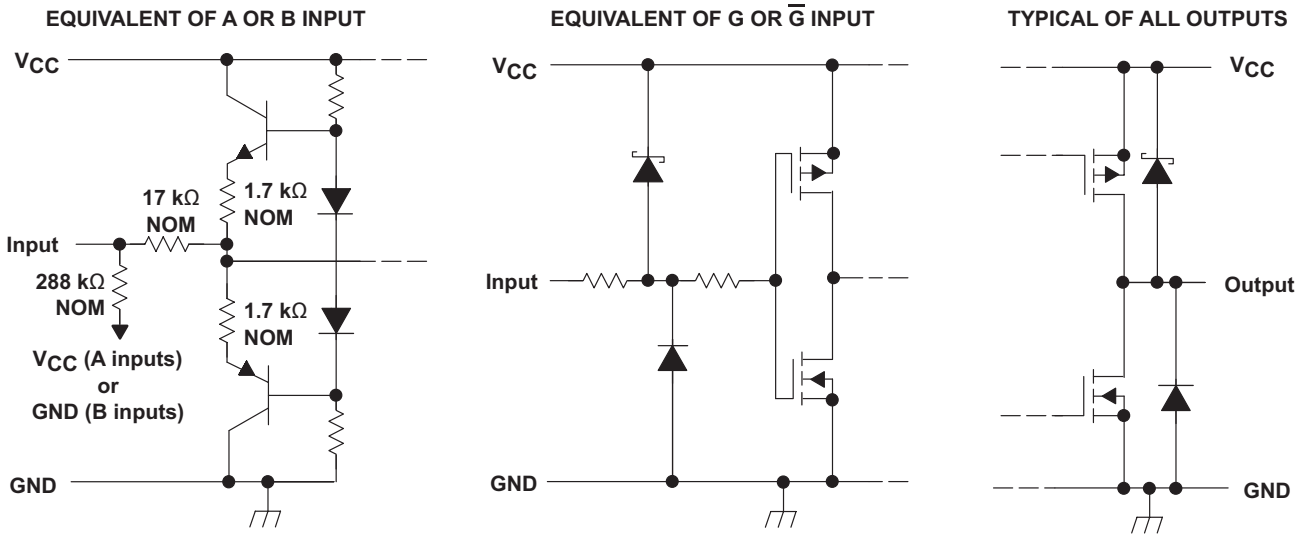
(1) H = High level, L = Low level, X = Irrelevant,
Z = High impedance (off), ? = Indeterminate

Logic Diagram (Positive Logic)



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

Schematics



Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)			7	V
V_I	Input voltage range	A or B inputs	–11	14	V
		G or $\overline{G}$ inputs	–0.5	V_{CC} + 0.5	
V_{ID}	Differential input voltage range		–14	14	V
V_O	Output voltage range		–0.5	V_{CC} + 0.5	V
I_O	Output current			±25	mA
θ_{JA}	Package thermal impedance(3)(4)	D package		73	°C/W
		N package		67	
		NS package		64	
		PW package		108	
T_J	Operating virtual junction temperature			150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential output voltage, V_{OD}, are with respect to network GND. Currents into the device are positive and currents out of the device are negative.
(3) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Common-mode input voltage				±7	V
I_{OH}	High-level output current				–6	mA
I_{OL}	Low-level output current				6	mA
T_A	Operating free-air temperature	AM26C32C	0		70	°C
		AM26C32I	–40		85	
		AM26C32Q	–40		125	
		AM26C32M	–55		125	

Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Differential input high-threshold voltage	$V_O = V_{OH(min)}$, I_{OH} = –440 µA	V_{IC} = –7 V to 7 V			0.2	V
			V_{IC} = 0 V to 5.5 V			0.1	
$V_{IT–}$	Differential input low-threshold voltage	V_O = 0.45 V, I_{OL} = 8 mA	V_{IC} = –7 V to 7 V	–0.2(2)			V
			V_{IC} = 0 V to 5.5 V	–0.1(2)			
V_{hys}	Hysteresis voltage ($V_{IT+} – V_{IT–}$)				60		mV
V_{IK}	Enable input clamp voltage	V_{CC} = 4.5 V, I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –6 mA		3.8			V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_{OL} = 6 mA			0.2	0.3	V
I_{OZ}	Off-state (high-impedance state) output current	$V_O = V_{CC}$ or GND			±0.5	±5	µA
I_I	Line input current	V_I = 10 V, Other input at 0 V				1.5	µA
		V_I = –10 V, Other input at 0 V				–2.5	
I_{IH}	High-level enable current	V_I = 2.7 V				20	µA
I_{IL}	Low-level enable current	V_I = 0.4 V				–100	µA
r_i	Input resistance	One input to ground		12	17		kΩ
I_{CC}	Quiescent supply current	V_{CC} = 5.5 V			10	15	mA

(1) All typical values are at V_{CC} = 5 V, V_{IC} = 0, and T_A = 25°C.
(2) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage.

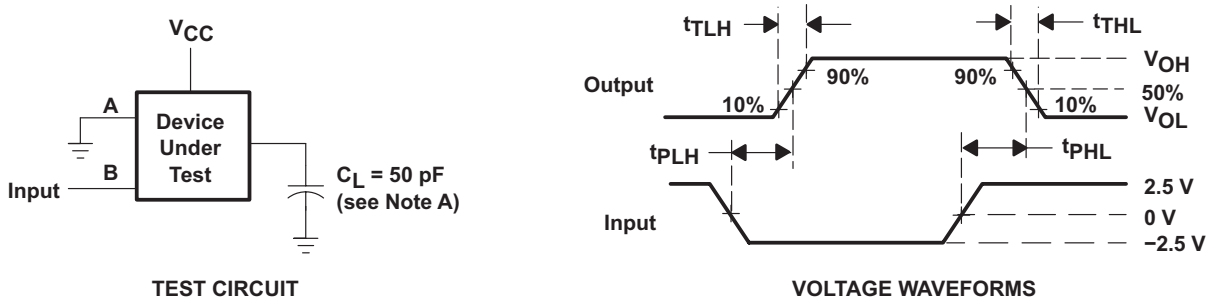
Switching Characteristics

over recommended ranges of operation conditions, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	AM26C32C AM26C32I			AM26C32Q AM26C32M			UNIT
			MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 1	9	17	27	9	17	27	ns
t_{PHL}	Propagation delay time, high- to low-level output		9	17	27	9	17	27	ns
t_{TLH}	Output transition time, low- to high-level output	See Figure 1		4	9		4	10	ns
t_{THL}	Output transition time, high- to low-level output			4	9		4	9	ns
t_{PZH}	Output enable time to high level	See Figure 2		13	22		13	22	ns
t_{PZL}	Output enable time to low level			13	22		13	22	ns
t_{PHZ}	Output disable time from high level	See Figure 2		13	22		13	26	ns
t_{PLZ}	Output disable time from low level			13	22		13	25	ns

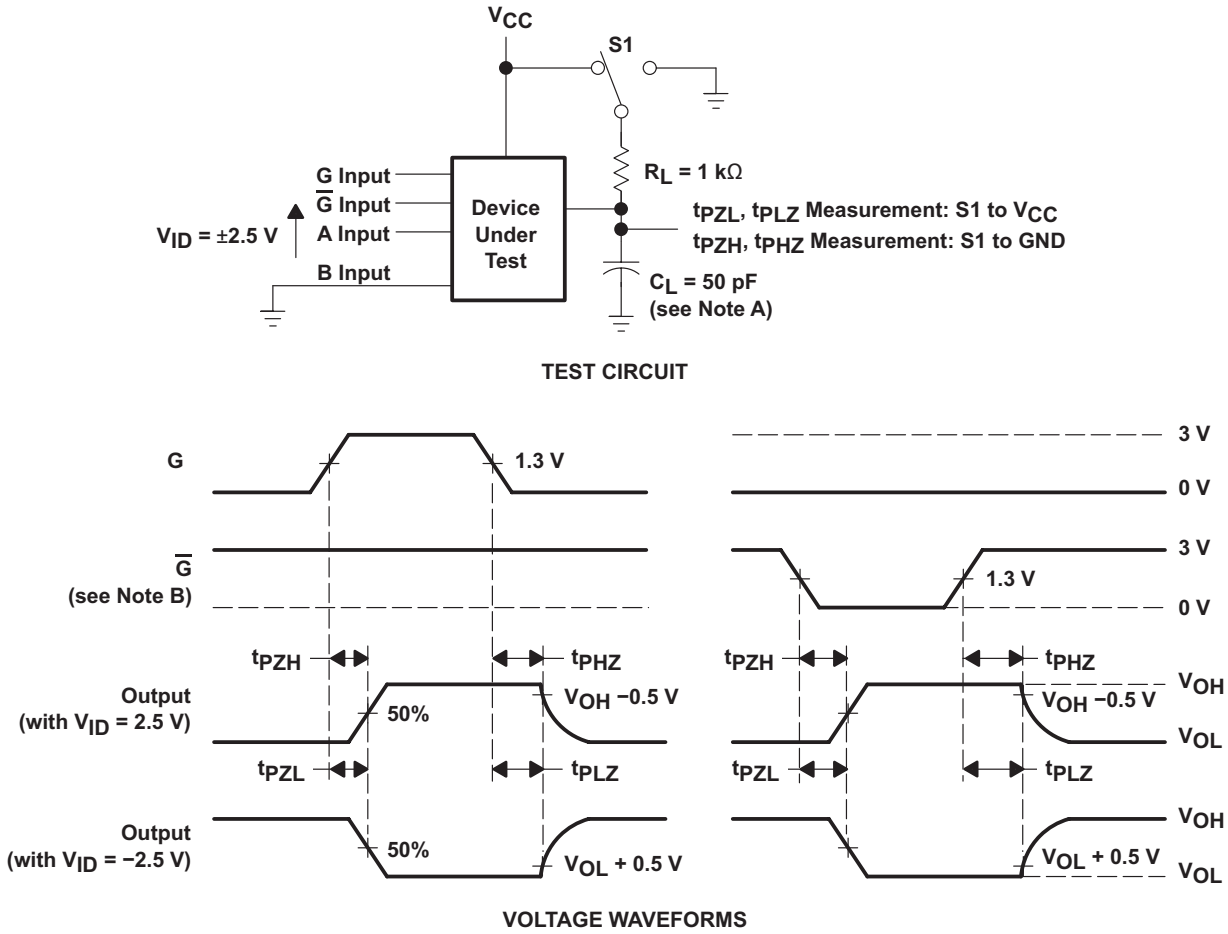
(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

Parameter Measurement Information



A. C_L includes probe and jig capacitance.

Figure 1. Switching Test Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≤ 50%, $t_r = t_f$ = 6 ns.

Figure 2. Enable/Disable Time Test Circuit and Output Voltage Waveforms

REVISION HISTORY

Changes from Revision I (September 2004) to Revision J **Page**

- Updated document to new TI data sheet format - no specification changes. 1
- Deleted Ordering Information table. 1
- Updated Features. 1
- ESD warning. 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9164001Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9164001Q2A AM26C32 MFKB	Samples
5962-9164001QEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9164001QEA AM26C32MJB	Samples
5962-9164001QFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9164001QFA AM26C32MWB	Samples
AM26C32CD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26C32C	Samples
AM26C32CDBLE	OBSOLETE	SSOP	DB	16		TBD	Call TI	Call TI	0 to 70		
AM26C32CDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26C32C	Samples
AM26C32CDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26C32C	Samples
AM26C32CDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26C32C	Samples
AM26C32CDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26C32C	Samples
AM26C32CN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	AM26C32CN	Samples
AM26C32CNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	AM26C32CN	Samples
AM26C32CNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	26C32	Samples
AM26C32CNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	26C32	Samples
AM26C32CNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	26C32	Samples
AM26C32ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26C32I	Samples
AM26C32IDBLE	OBSOLETE	SSOP	DB	16		TBD	Call TI	Call TI	-40 to 85		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AM26C32IDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26C32I	Samples
AM26C32IDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26C32I	Samples
AM26C32IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26C32I	Samples
AM26C32IDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26C32I	Samples
AM26C32IDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26C32I	Samples
AM26C32IN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	AM26C32IN	Samples
AM26C32INE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	AM26C32IN	Samples
AM26C32INSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C32I	Samples
AM26C32IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C32I	Samples
AM26C32IPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C32I	Samples
AM26C32IPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C32I	Samples
AM26C32IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C32I	Samples
AM26C32IPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C32I	Samples
AM26C32MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9164001Q2A AM26C32 MFKB	Samples
AM26C32MJB	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9164001QE A AM26C32MJB	Samples
AM26C32MWB	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9164001QF A AM26C32MWB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AM26C32QD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AM26C32Q	Samples
AM26C32QDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	26C32Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF AM26C32, AM26C32M :

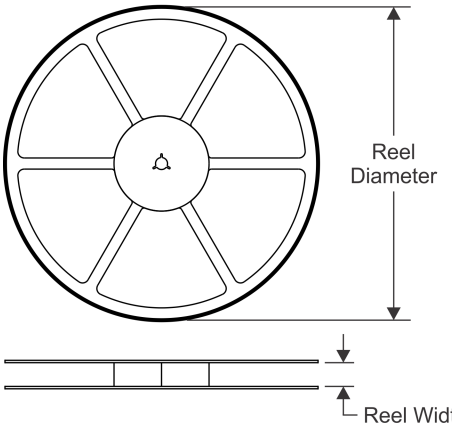
- Catalog: AM26C32
- Enhanced Product: AM26C32-EP, AM26C32-EP
- Military: AM26C32M

NOTE: Qualified Version Definitions:

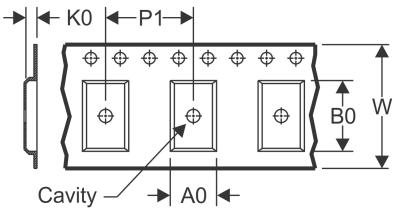
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

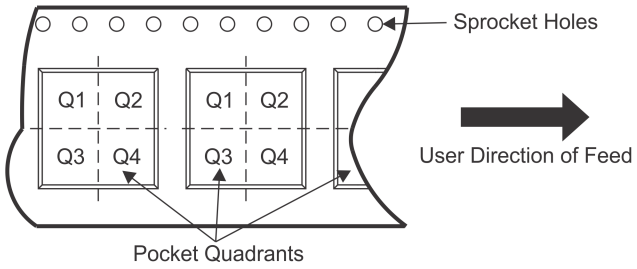


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

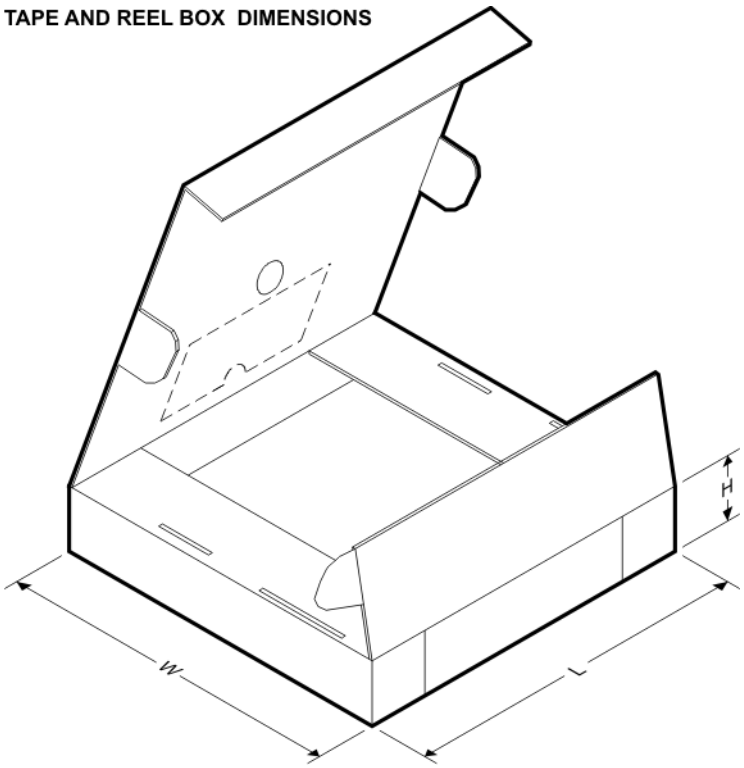
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM26C32CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26C32IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26C32IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



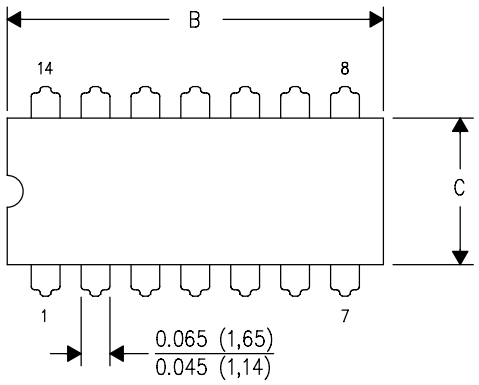
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26C32CDR	SOIC	D	16	2500	333.2	345.9	28.6
AM26C32IDR	SOIC	D	16	2500	333.2	345.9	28.6
AM26C32IPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

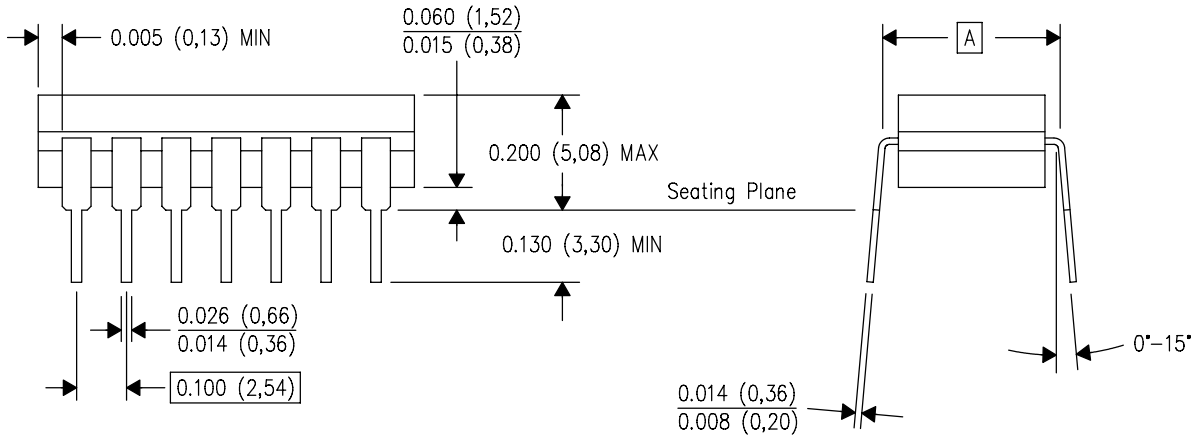
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



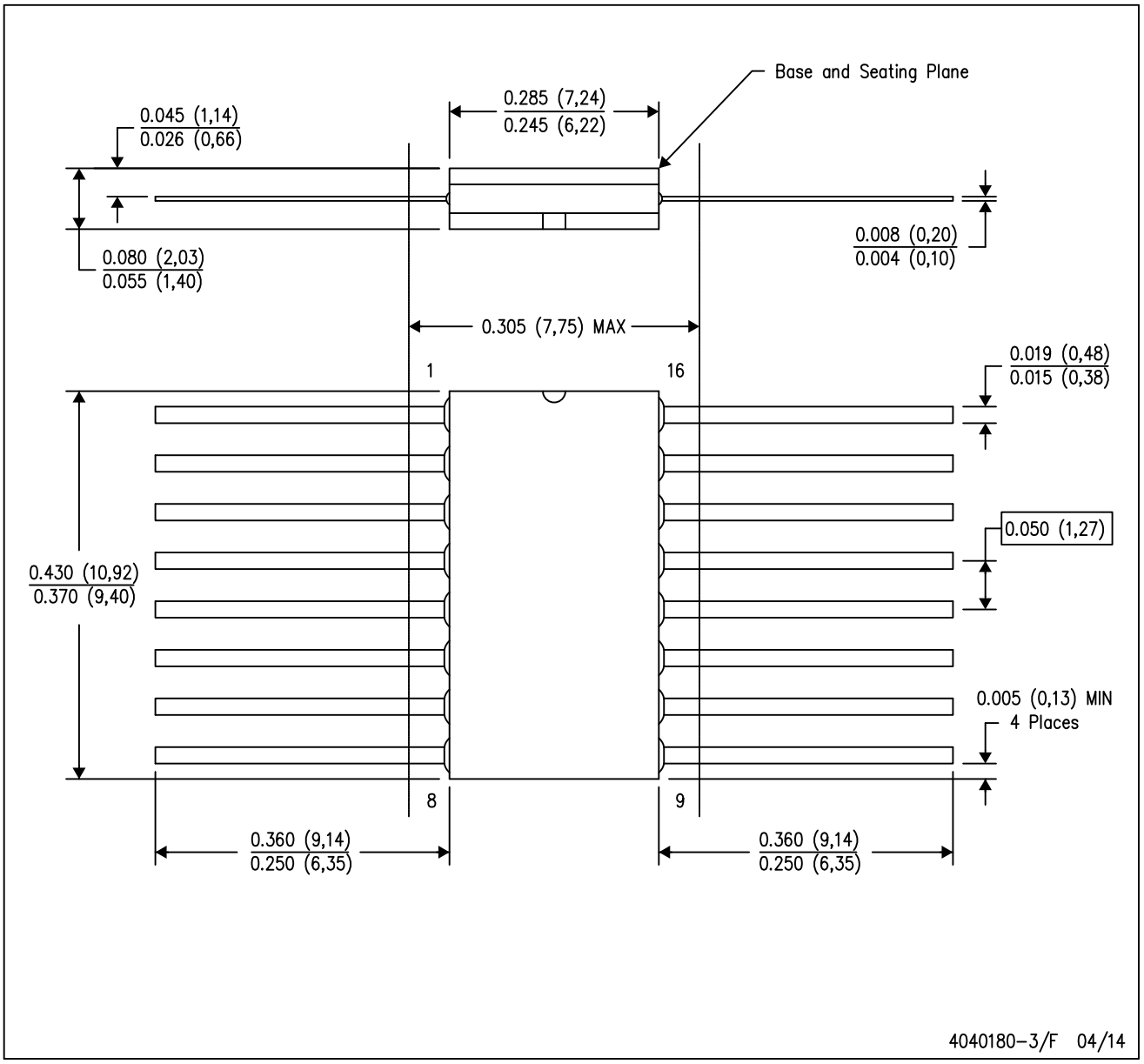
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

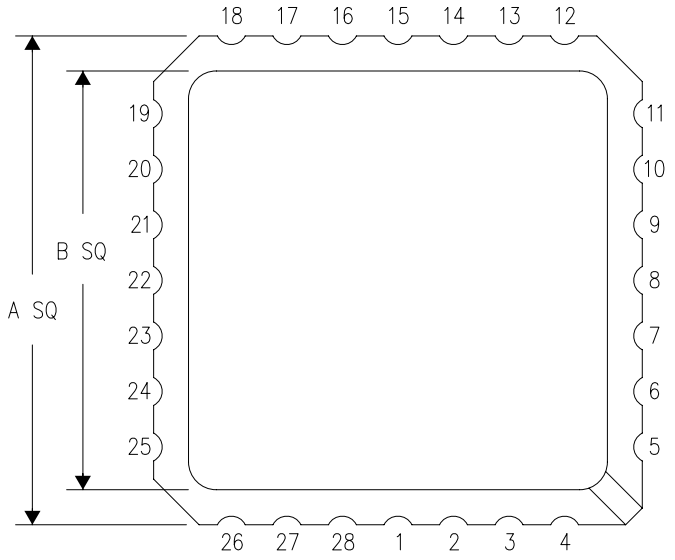
W (R–GDFP–F16) CERAMIC DUAL FLATPACK



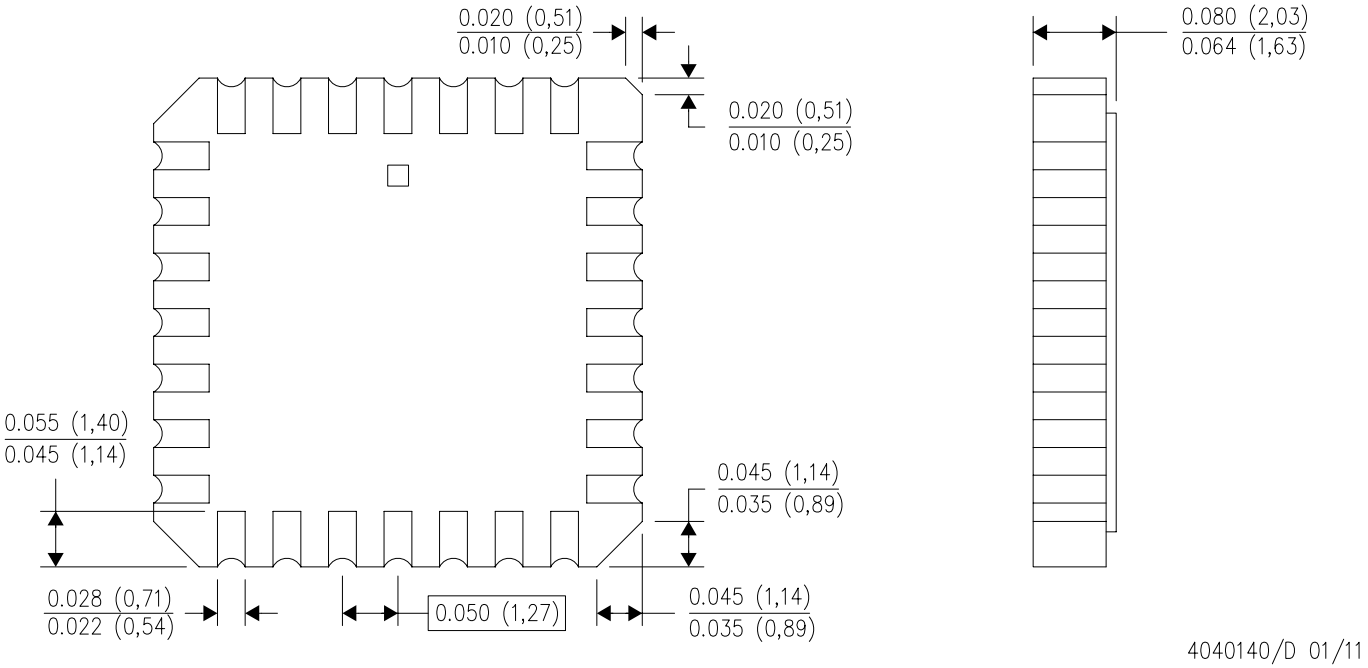
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



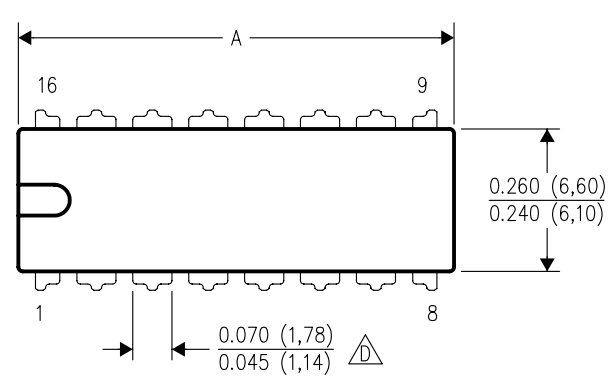
4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

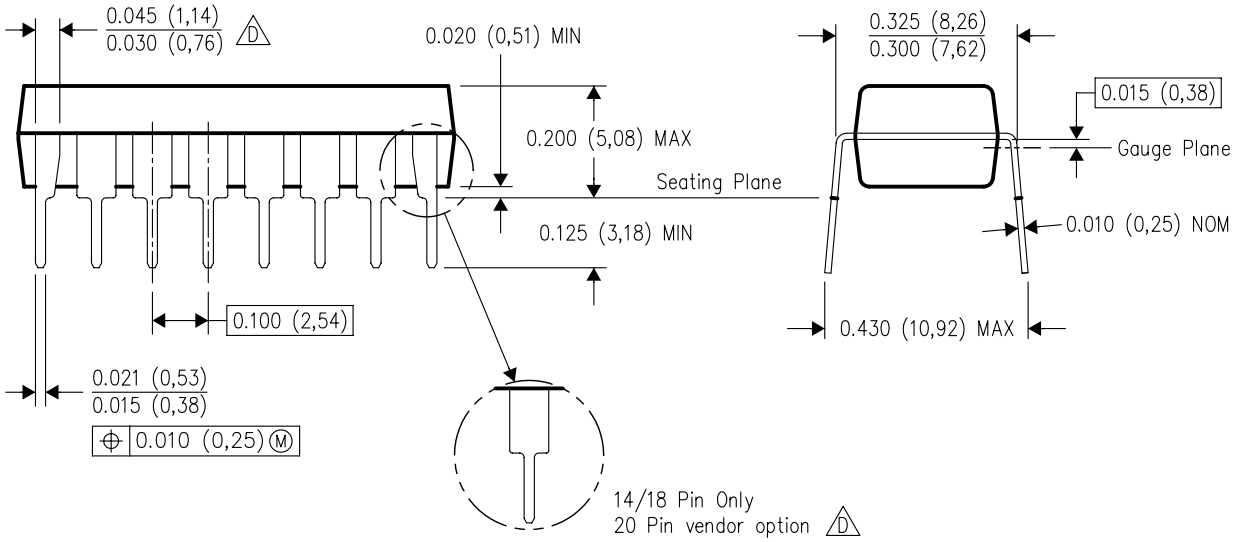
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



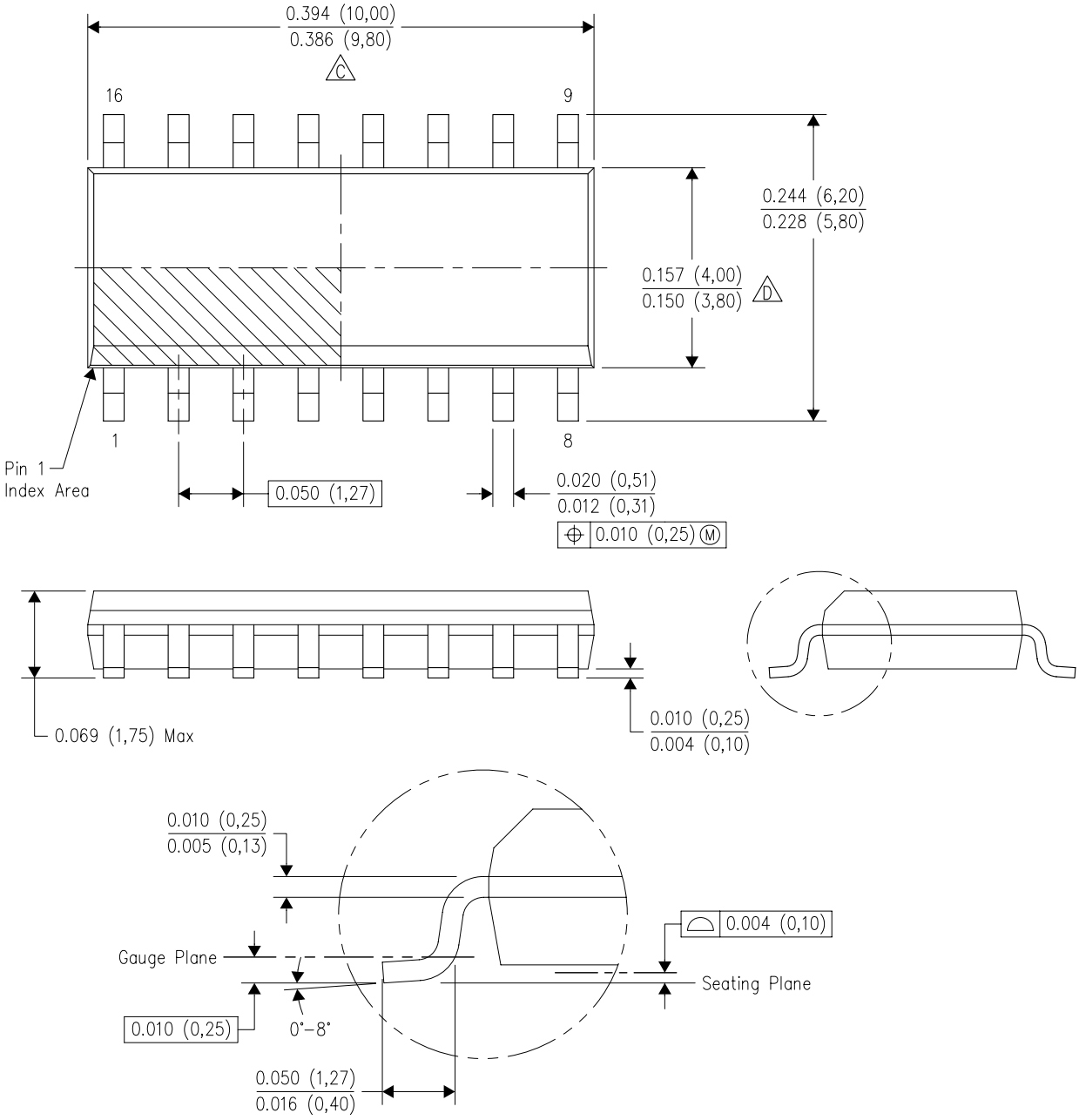
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

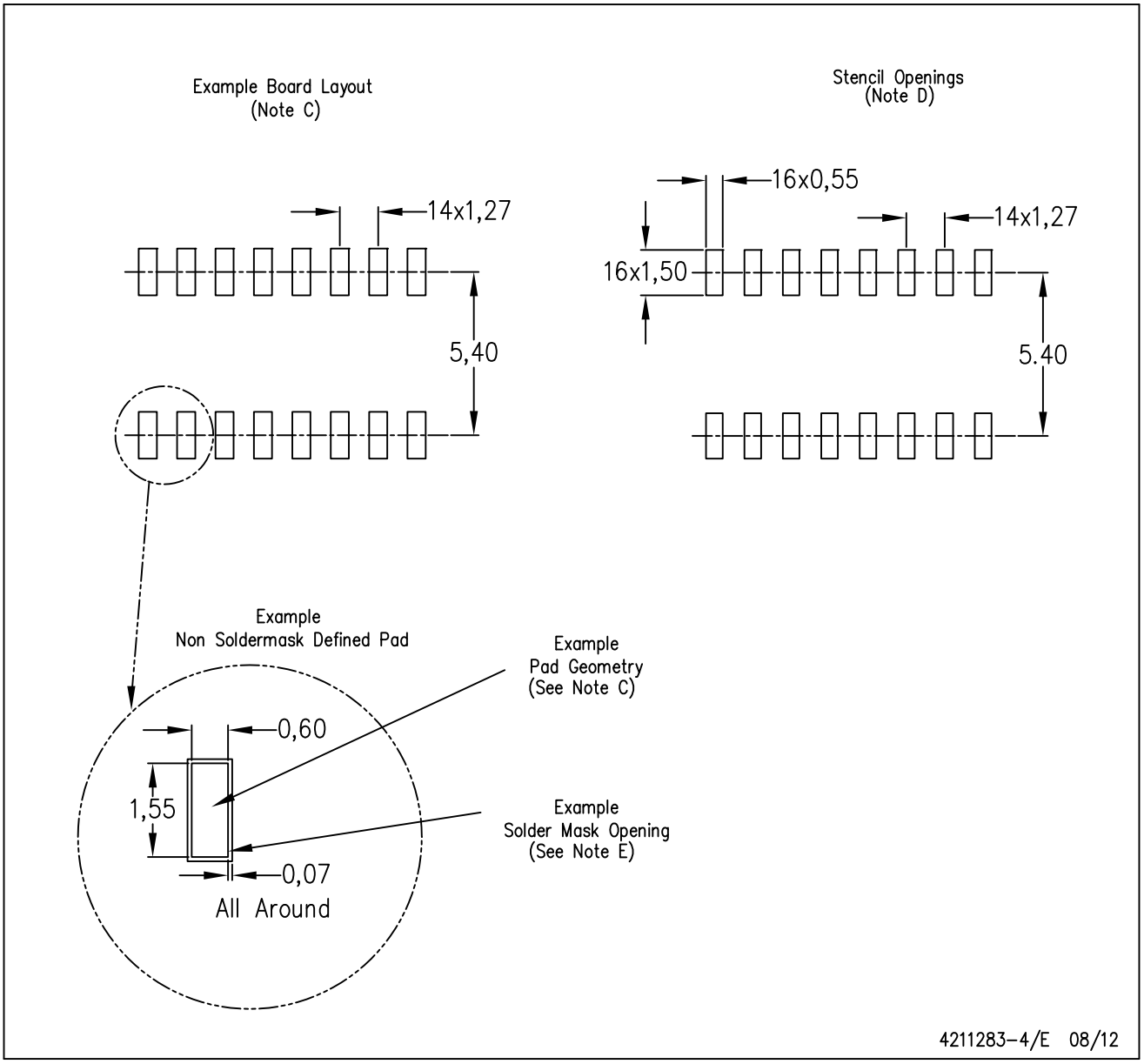
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



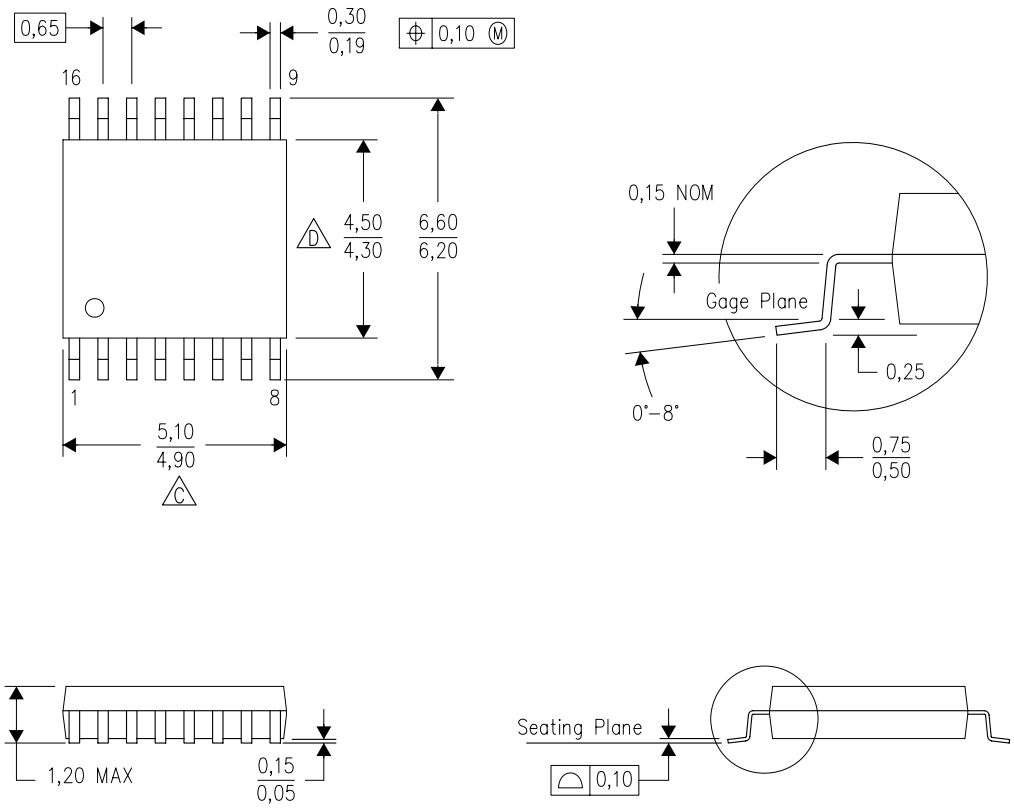
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

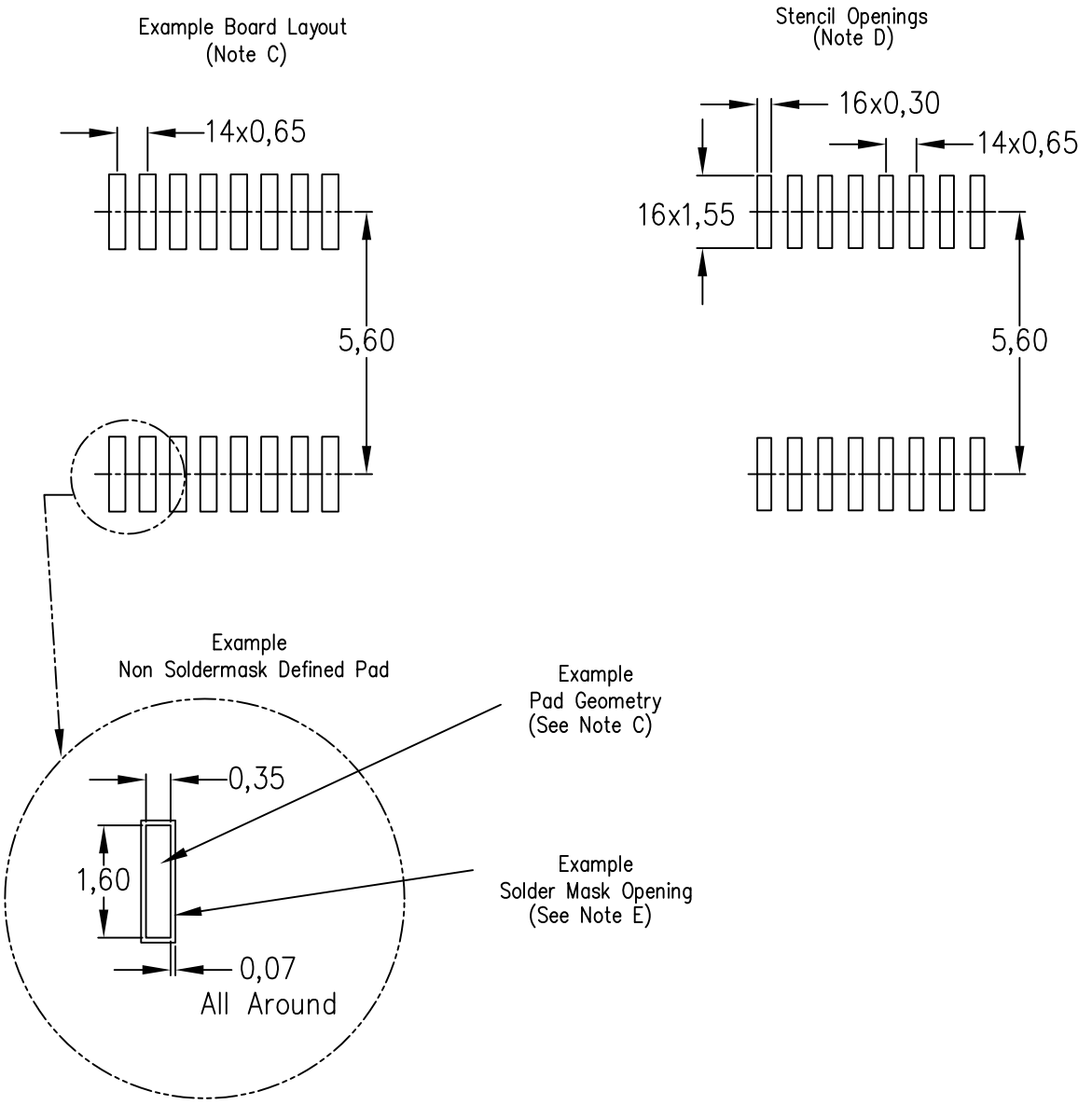
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE

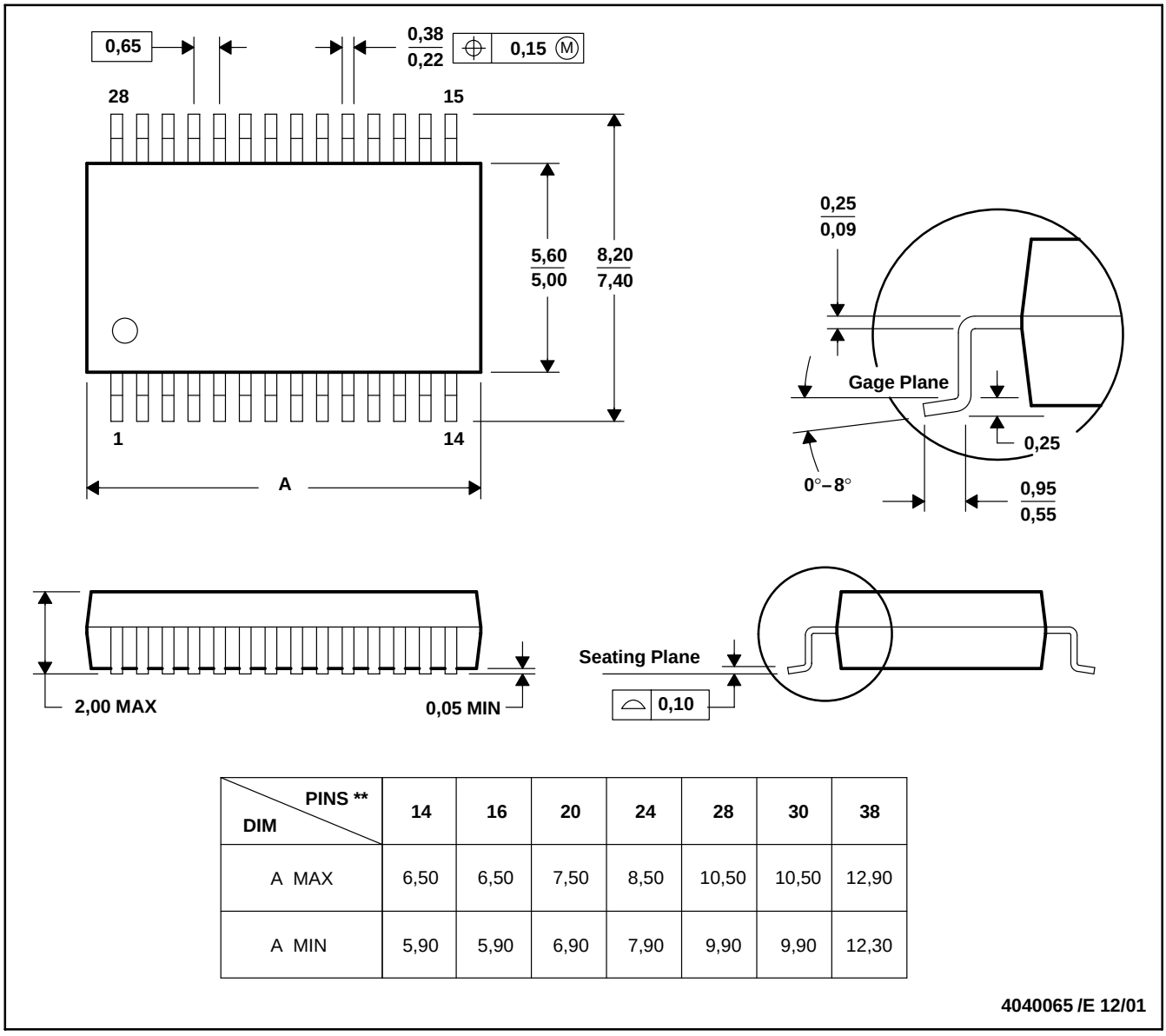


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

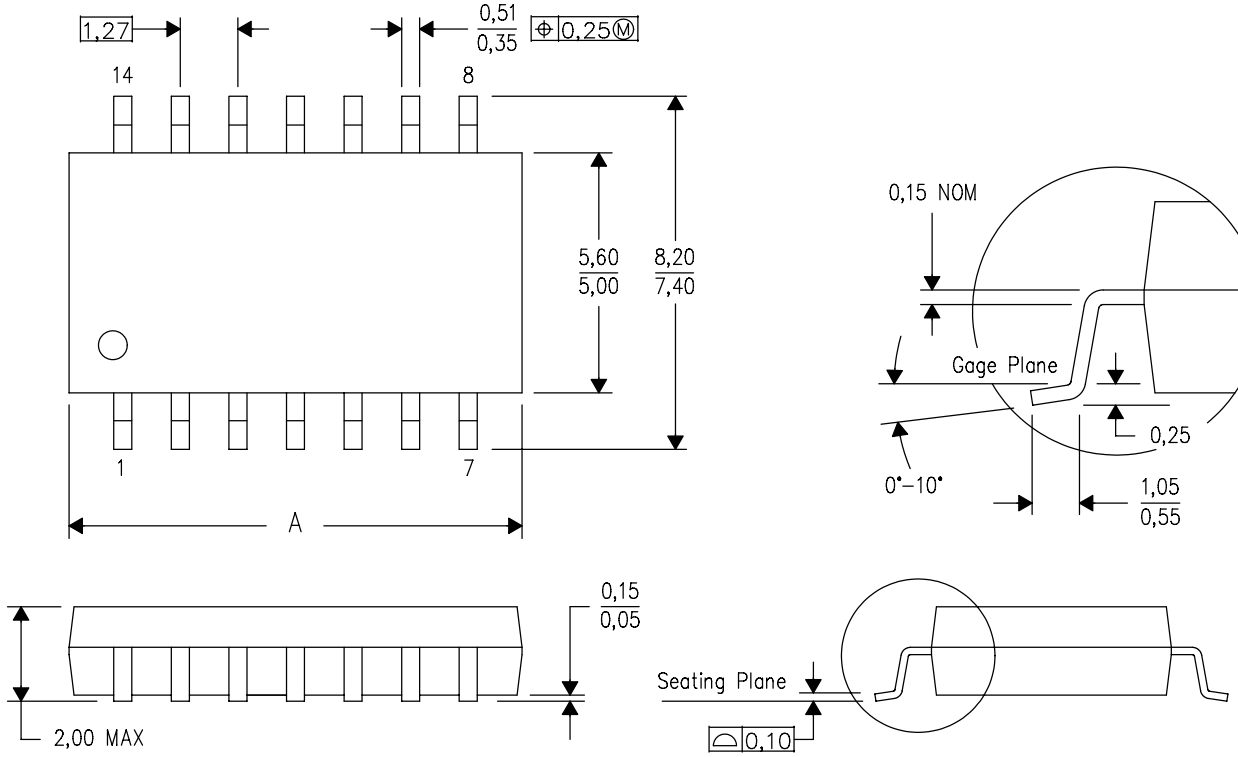
4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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