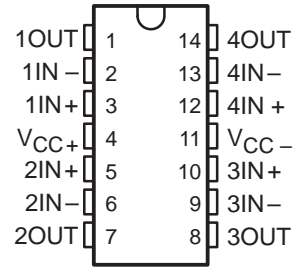


- Low Input Bias Current . . . 50 pA Typ
- Low Input Noise Current  
0.01 pA/√Hz Typ
- Low Total Harmonic Distortion
- Low Supply Current . . . 8 mA Typ
- Gain Bandwidth . . . 3 MHz Typ
- High Slew Rate . . . 13 V/μs Typ
- Pin Compatible With the LM348

**D OR N PACKAGE**  
(TOP VIEW)



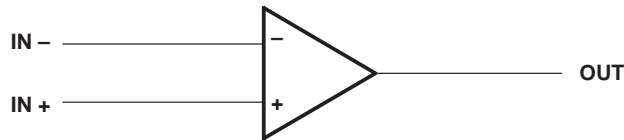
**description**

These devices are low-cost, high-speed, JFET-input operational amplifiers. They require low supply current yet maintain a large gain-bandwidth product and a fast slew rate. In addition, their matched high-voltage JFET inputs provide very low input bias and offset current.

The LF347 and LF347B can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF347 and LF347B are characterized for operation from 0°C to 70°C.

**symbol (each amplifier)**



**AVAILABLE OPTIONS**

T <sub>A</sub>	V <sub>IO</sub> max AT 25°C	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC DIP (N)
0°C to 70°C	10 mV	LF347D	LF347N
	5 mV	LF347BD	LF347BN

The D packages are available taped and reeled. Add R suffix to the device type (e.g., LF347DR).

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, V <sub>CC</sub> +	18 V
Supply voltage, V <sub>CC</sub> -	-18 V
Differential input voltage, V <sub>ID</sub>	±30 V
Input voltage, V <sub>I</sub> (see Note 1)	±15 V
Duration of output short circuit	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

# LF347, LF347B

## JFET-INPUT

### QUAD OPERATIONAL AMPLIFIERS

SLOS013B – MARCH 1987 – REVISED AUGUST 1994

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR	DERATE ABOVE $T_A$	$T_A = 70^\circ\text{C}$ POWER RATING
D	608 mW	7.6 mW/°C	61°C	608 mW
N	680 mW	N/A	N/A	680 mW

#### recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, $V_{CC+}$	3.5	18	V
Supply voltage, $V_{CC-}$	-3.5	-18	V

#### electrical characteristics over operating free-air temperature range, $V_{CC\pm} = \pm 15\text{ V}$ (unless otherwise specified)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	LF347			LF347B			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = 0$ , $R_S = 10\text{ k}\Omega$	25°C	5	10		3	5	mV	
		Full range			13		7		
$\alpha_{VIO}$ Average temperature coefficient of input offset voltage	$V_{IC} = 0$ , $R_S = 10\text{ k}\Omega$		18			18		$\mu\text{V}/^\circ\text{C}$	
$I_{IO}$ Input offset current $\ddagger$	$V_{IC} = 0$	25°C	25	100		25	100	pA	
		70°C		4			4	nA	
$I_{IB}$ Input bias current $\ddagger$	$V_{IC} = 0$	25°C	50	200		50	200	pA	
		70°C		8			8	nA	
$V_{ICR}$ Common-mode input voltage range			$\pm 11$	-12 to 15		$\pm 11$	-12 to 15	V	
$V_{OM}$ Maximum peak output voltage swing	$R_L = 10\text{ k}\Omega$		$\pm 12$	$\pm 13.5$		$\pm 12$	$\pm 13.5$	V	
$A_{VD}$ Large-signal differential voltage	$V_O = \pm 10\text{ V}$ , $R_L = 2\text{ k}\Omega$	25°C	25	100		50	100	V/mV	
		Full range	15			25			
$r_i$ Input resistance	$T_A = 25^\circ\text{C}$		$10^{12}$			$10^{12}$		$\Omega$	
CMRR Common-mode rejection ratio	$R_S \leq 2\text{ k}\Omega$		70	100		80	100	dB	
$k_{SVR}$ Supply-voltage rejection ratio	See Note 2		70	100		80	100	dB	
$I_{CC}$ Supply current			8	11		8	11	mA	

$^\dagger$  Full range is 0°C to 70°C.

$\ddagger$  Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.

NOTE 2: Supply-voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

#### operating characteristics, $V_{CC\pm} = \pm 15\text{ V}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{O1}/V_{O2}$ Crosstalk attenuation	$f = 1\text{ kHz}$		120		dB
SR Slew rate		8	13		V/ $\mu\text{s}$
$B_1$ Unity-gain bandwidth			3		MHz
$V_n$ Equivalent input noise voltage	$f = 1\text{ kHz}$ , $R_S = 20\ \Omega$		18		$\text{nV}/\sqrt{\text{Hz}}$
$I_n$ Equivalent input noise current	$f = 1\text{ kHz}$		0.01		$\text{pA}/\sqrt{\text{Hz}}$



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LF347BD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LF347B	<a href="#">Samples</a>
LF347BDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LF347B	<a href="#">Samples</a>
LF347BN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LF347BN	<a href="#">Samples</a>
LF347BNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LF347BN	<a href="#">Samples</a>
LF347D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LF347	<a href="#">Samples</a>
LF347DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LF347	<a href="#">Samples</a>
LF347DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LF347	<a href="#">Samples</a>
LF347DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LF347	<a href="#">Samples</a>
LF347DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LF347	<a href="#">Samples</a>
LF347N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LF347N	<a href="#">Samples</a>
LF347NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LF347N	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

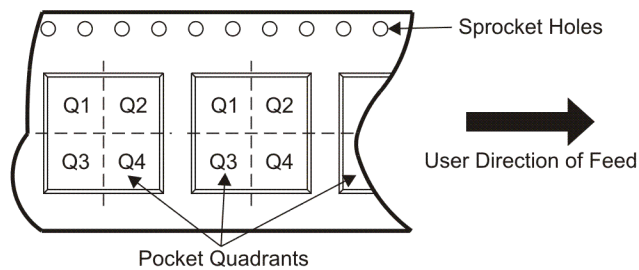
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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LF347BDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LF347DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LF347BDR	SOIC	D	14	2500	333.2	345.9	28.6
LF347DR	SOIC	D	14	2500	333.2	345.9	28.6

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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