



IMPORTANT NOTICE

10 December 2015

1. Global joint venture starts operations as WeEn Semiconductors

Dear customer,

As from November 9th, 2015 NXP Semiconductors N.V. and Beijing JianGuang Asset Management Co. Ltd established Bipolar Power joint venture (JV), **WeEn Semiconductors**, which will be used in future Bipolar Power documents together with new contact details.

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Thank you for your cooperation and understanding,

WeEn Semiconductors





BTA316B-800C

3Q Hi-Com Triac

6 August 2014

Product data sheet

1. General description

Planar passivated high commutation three quadrant triac in a SOT404 plastic package intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. This "series C" triac will commutate the full RMS current at the maximum rated junction temperature without the aid of a snubber.

2. Features and benefits

- 3Q technology for improved noise immunity
- High commutation capability with maximum false trigger immunity
- High immunity to false turn-on by dV/dt
- High voltage capability
- Planar passivated for voltage ruggedness and reliability
- Surface mountable package
- Triggering in three quadrants only

3. Applications

- Electronic thermostats (heating and cooling)
- High power motor controls e.g. washing machines and vacuum cleaners
- Rectifier-fed DC inductive loads e.g. DC motors and solenoids

4. Quick reference data

Table 1. Quick reference data

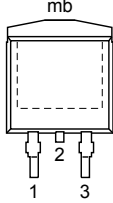

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	800	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	-	140	A
$I_{T(\text{RMS})}$	RMS on-state current	full sine wave; $T_{mb} \leq 101\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	16	A
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 7	2	-	35	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 7	2	-	35	mA



Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	2	-	35	mA

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 <p>D2PAK (SOT404)</p>	
2	T2	main terminal 2		
3	G	gate		
mb	T2	mounting base; main terminal 2		

6. Ordering information

Table 3. Ordering information

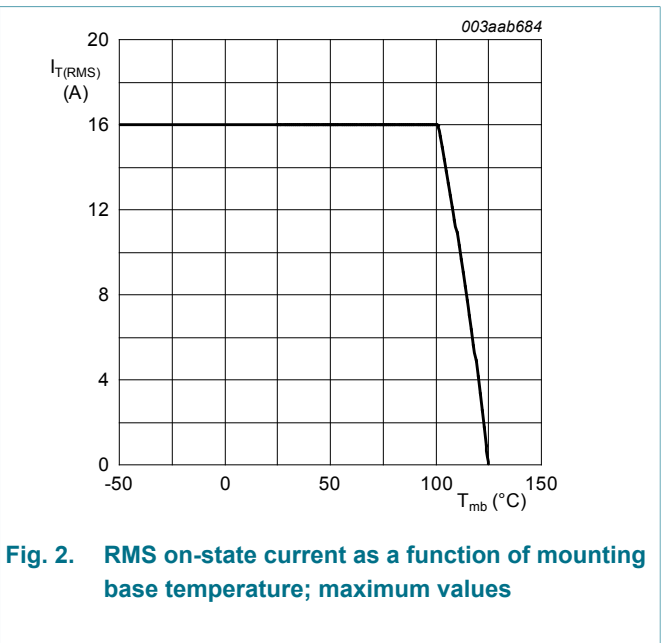
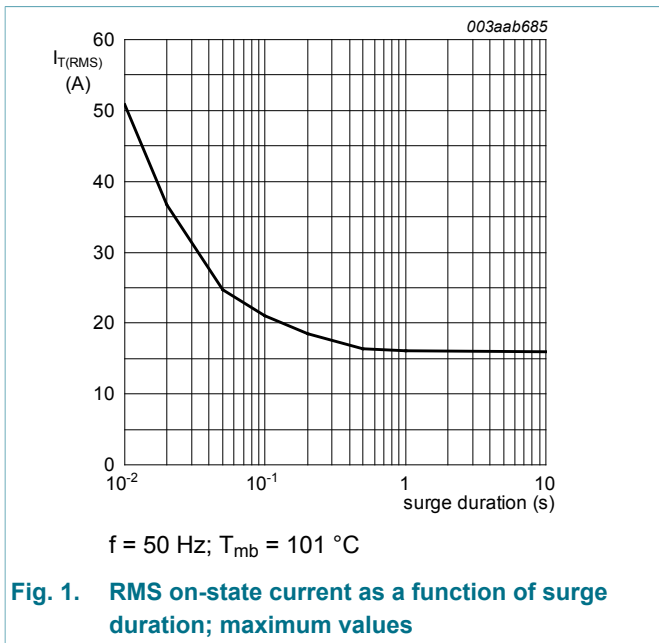
Type number	Package		
	Name	Description	Version
BTA316B-800C	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 101\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	16	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	140	A
		full sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 16.7\text{ ms}$	-	150	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; SIN	-	98	A^2s
di_T/dt	rate of rise of on-state current	$I_T = 20\text{ A}$; $I_G = 0.2\text{ A}$; $di_G/dt = 0.2\text{ A}/\mu\text{s}$	-	100	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		-	2	A
P_{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
T_{stg}	storage temperature		-40	150	$^{\circ}\text{C}$
T_j	junction temperature		-	125	$^{\circ}\text{C}$



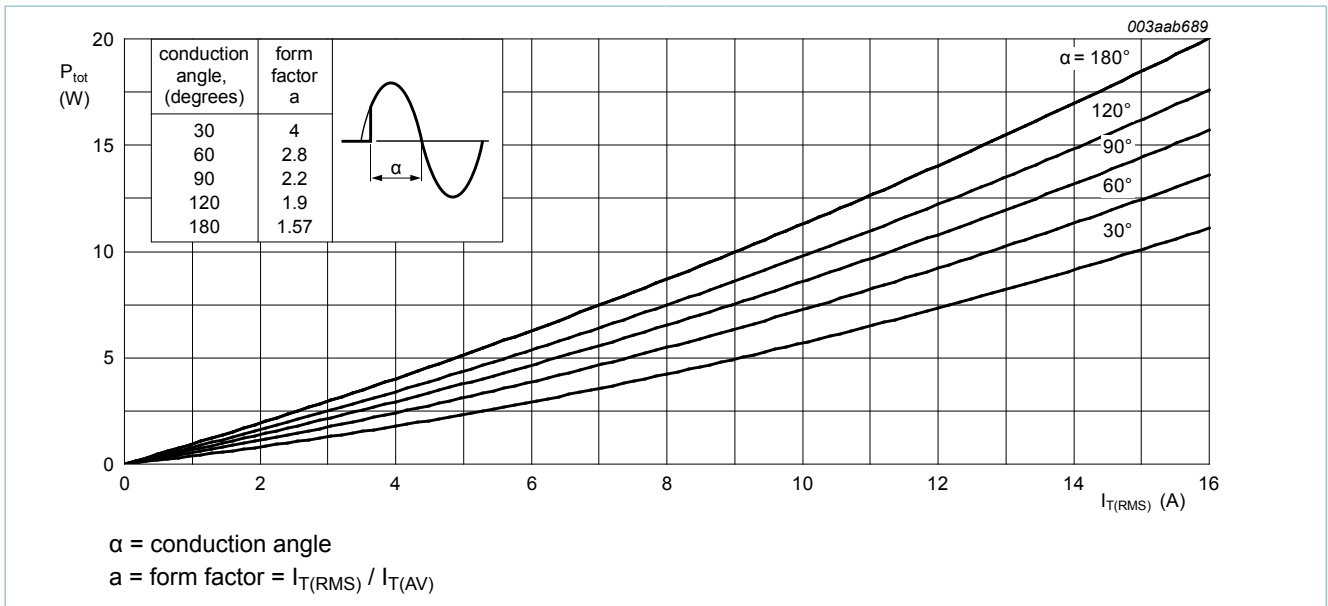


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

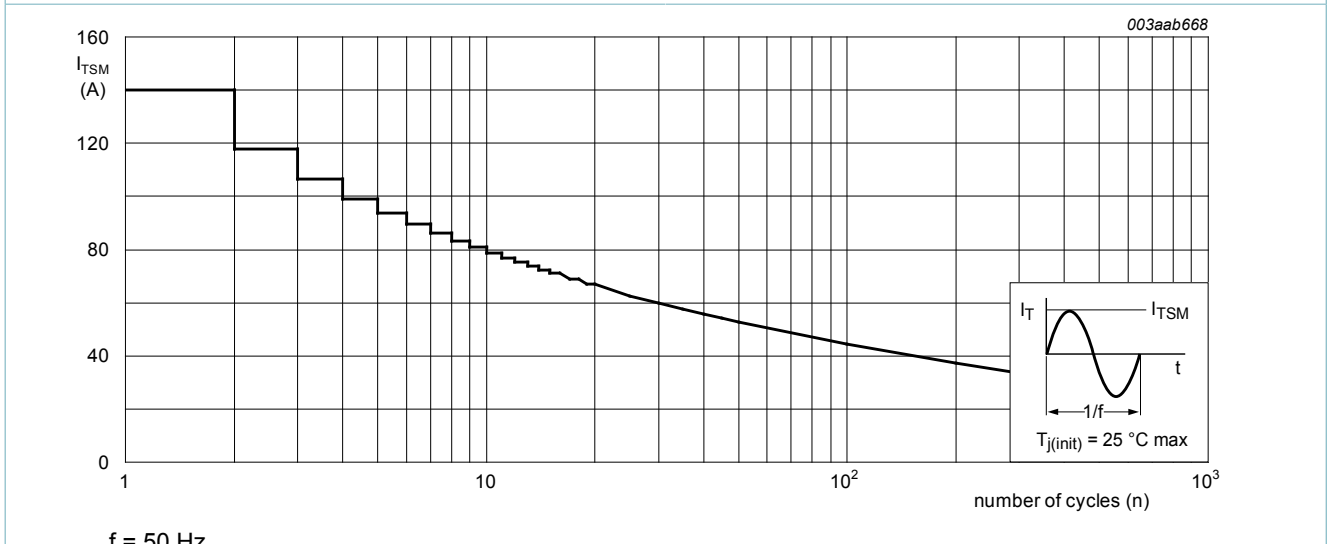
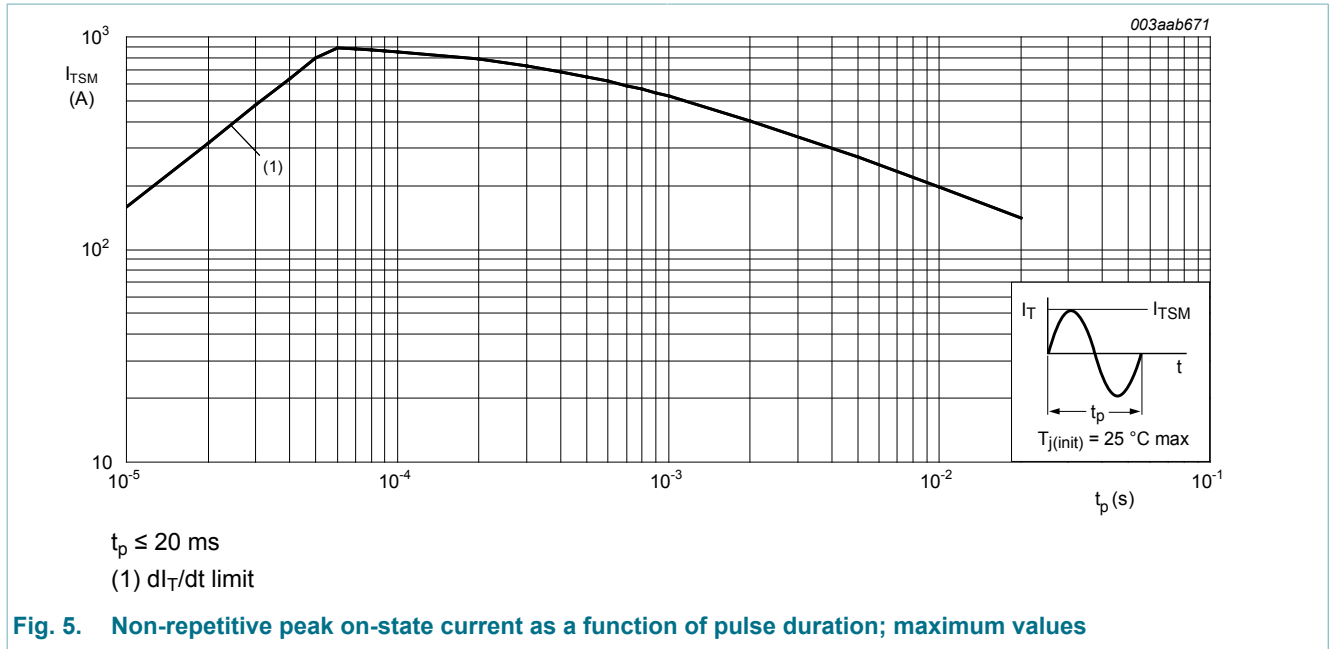


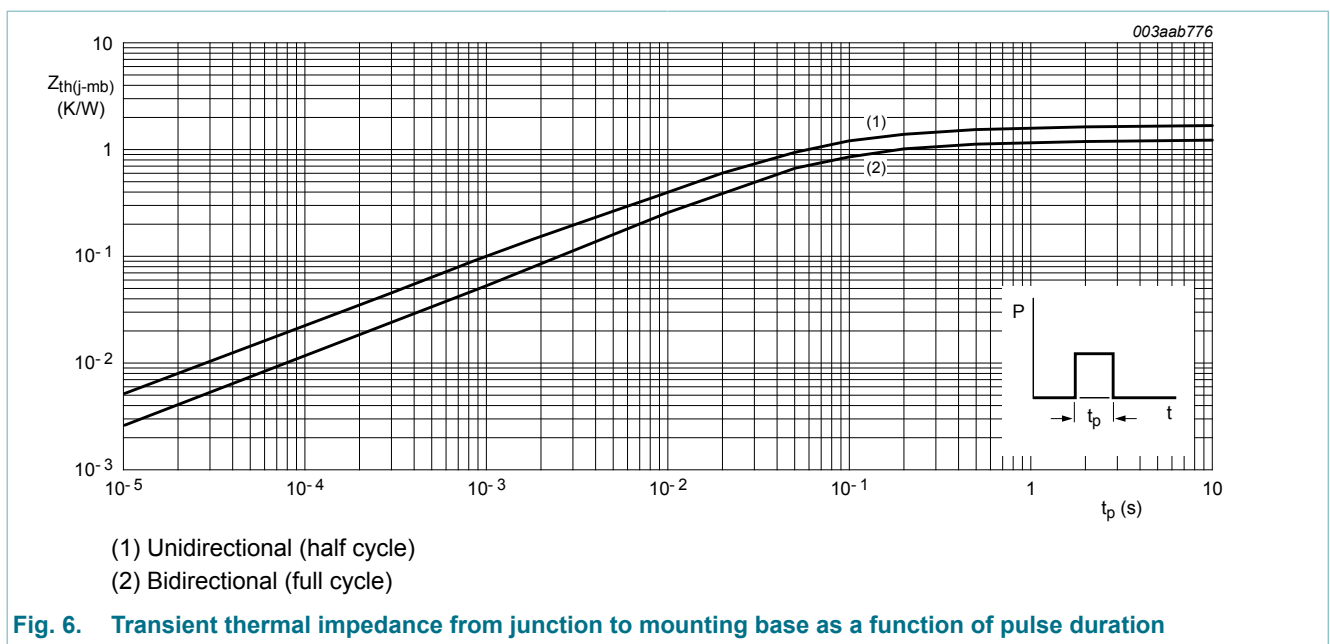
Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



8. Thermal characteristics

Table 5. Thermal characteristics

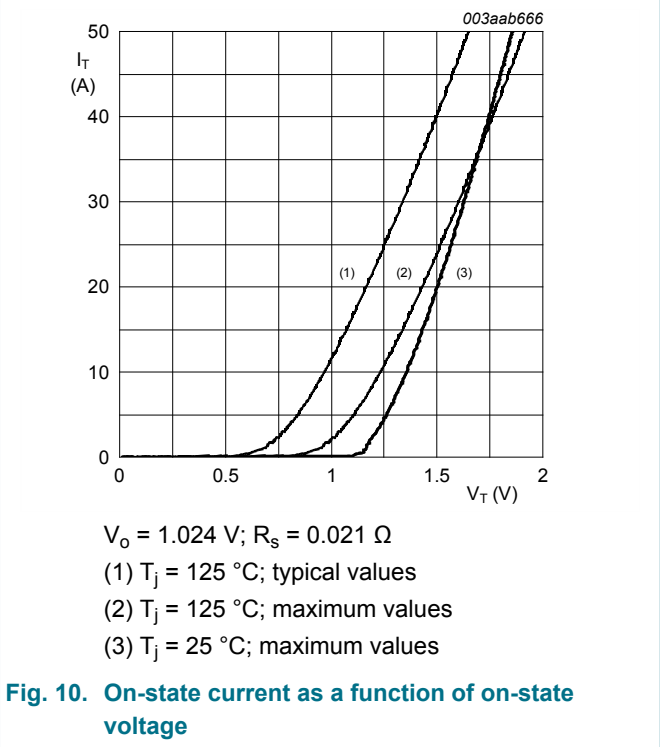
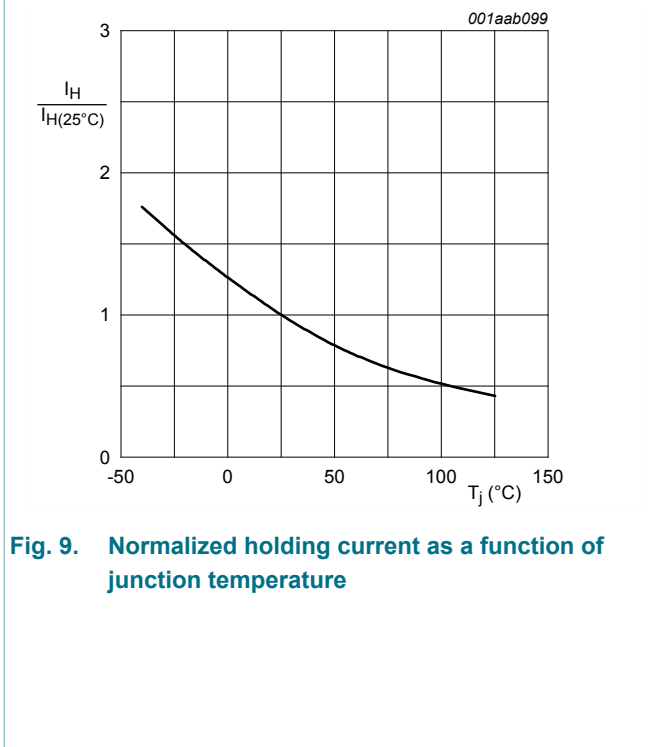
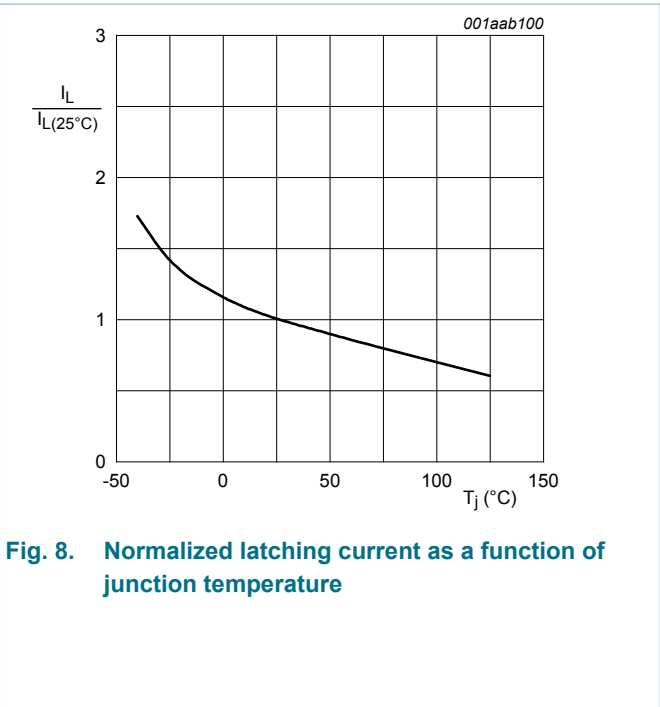
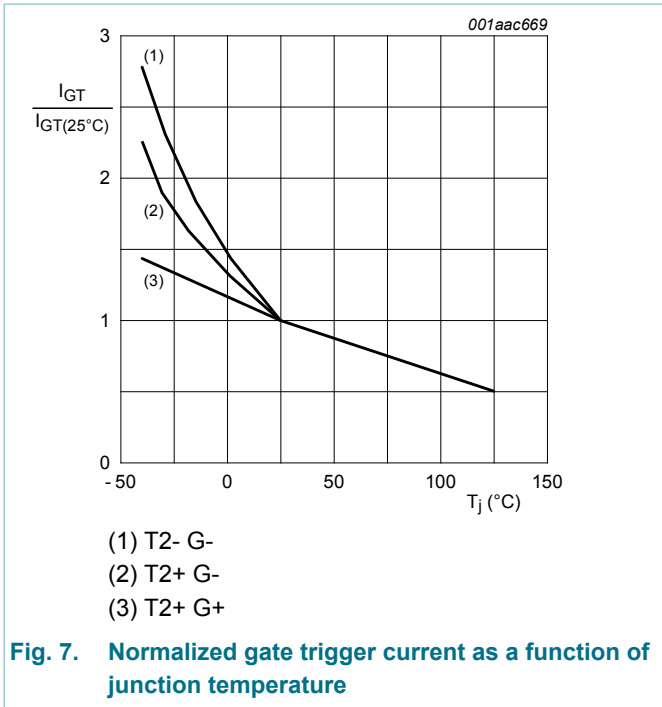
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	full cycle; Fig. 6	-	-	1.2	K/W
		half cycle; Fig. 6	-	-	1.7	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	printed circuit board mounted; minimum footprint	-	55	-	K/W



9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	2	-	35	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	2	-	35	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	2	-	35	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8	-	-	50	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8	-	-	60	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8	-	-	50	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9	-	-	35	mA
V_T	on-state voltage	$I_T = 18\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10	-	1.3	1.5	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 11	-	0.8	1	V
		$V_D = 400\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ }^\circ\text{C}$; Fig. 11	0.25	0.4	-	V
I_D	off-state current	$V_D = 800\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$	-	0.1	0.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit	500	-	-	V/ μs
dI_{com}/dt	rate of change of commutating current	$V_D = 400\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $I_{T(RMS)} = 16\text{ A}$; $dV_{com}/dt = 20\text{ V}/\mu\text{s}$; (snubberless condition); gate open circuit	15	-	-	A/ms



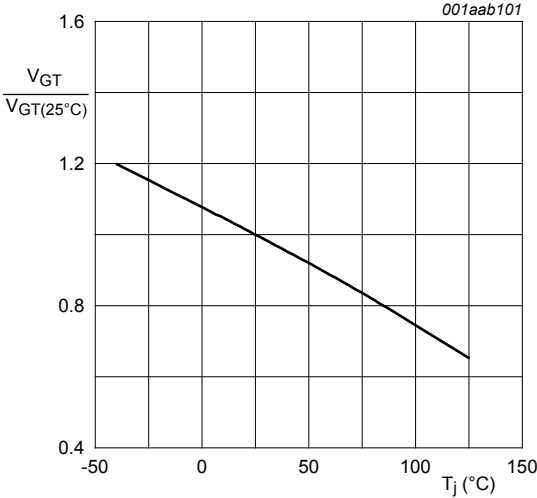
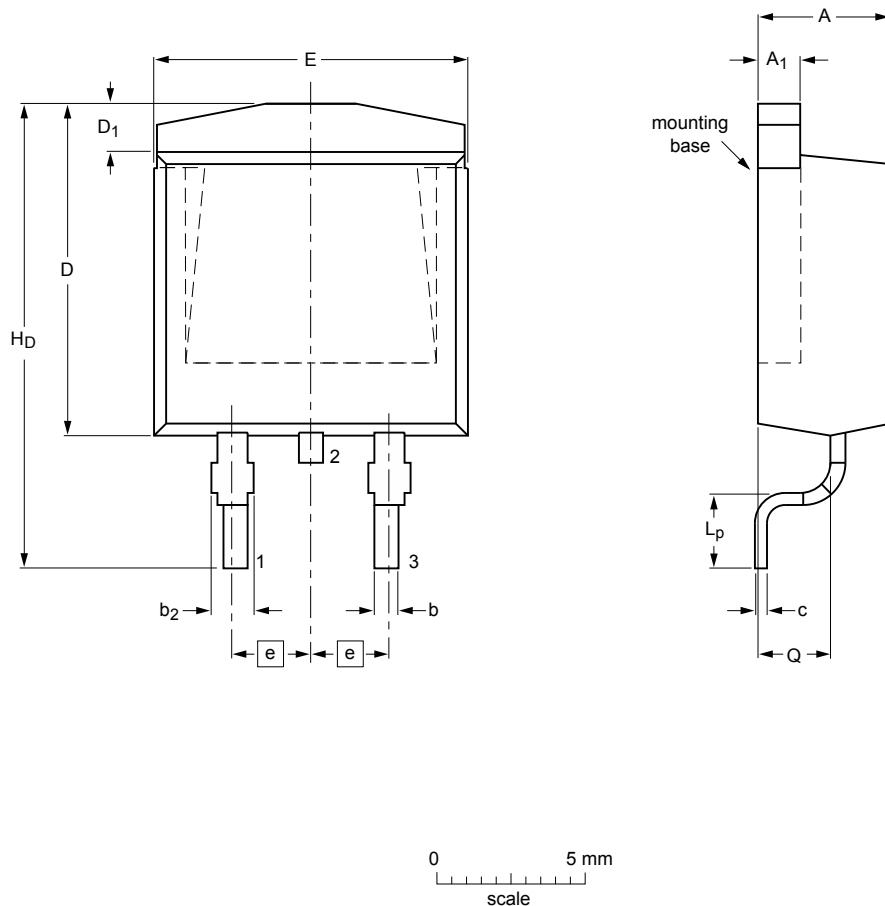


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

10. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) SOT404



Dimensions (mm are the original dimensions)

Unit	A	A ₁	b	b ₂	c	D	D ₁	E	e	H _D	L _p	Q
max	4.5	1.40	0.85	1.45	0.64	11	1.6	10.3		15.8	2.9	2.6
nom									2.54			
min	4.1	1.27	0.60	1.05	0.46		1.2	9.7		14.8	2.1	2.2

sot404_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT404					-06-03-16- 13-02-25

Fig. 12. Package outline D2PAK (SOT404)

11. Soldering

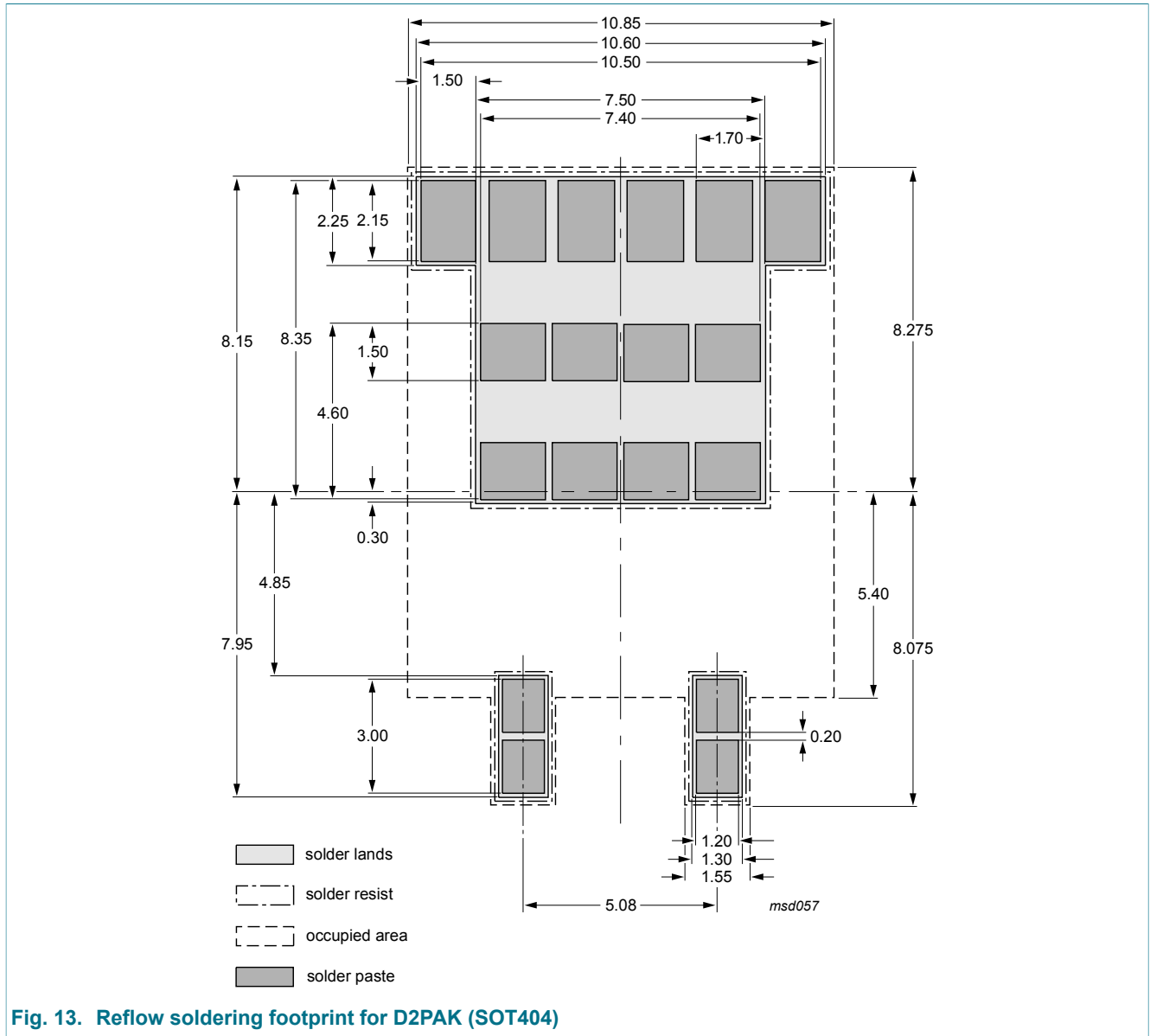


Fig. 13. Reflow soldering footprint for D2PAK (SOT404)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 6 August 2014