XC18V00 Series In-System-Programmable Configuration PROMs

DS026 (v6.0) August 5, 2015 **Product Specification**

Features

- In-System Programmable 3.3V PROMs for Configuration of Xilinx FPGAs
  - Endurance of 20,000 Program/Erase Cycles
  - Program/Erase Over Full Industrial Voltage and Temperature Range (–40°C to +85°C)
- IEEE Std 1149.1 Boundary-Scan (JTAG) Support
- JTAG Command Initiation of Standard FPGA Configuration
- Simple Interface to the FPGA
- Cascadable for Storing Longer or Multiple Bitstreams
- Low-Power Advanced CMOS FLASH Process
- Dual Configuration Modes
  - Serial Slow/Fast Configuration (up to 33 MHz)
  - Parallel (up to 264 Mb/s at 33 MHz)
- 5V-Tolerant I/O Pins Accept 5V, 3.3V and 2.5V Signals
- 3.3V or 2.5V Output Capability
- Design Support Using the Xilinx ISE™ Foundation™ Software Packages
- Available in PC20, SO20, PC44, and VQ44 Packages
- Lead-Free (Pb-Free) Packaging

Description

Xilinx introduces the XC18V00 series of in-system programmable configuration PROMs (Figure 1). Devices in this 3.3V family include a 4-megabit, a 2-megabit, a 1-megabit, and a 512-kilobit PROM that provide an easy-to-use, cost-effective method for reprogramming and storing Xilinx FPGA configuration bitstreams.

When the FPGA is in Master Serial mode, it generates a configuration clock that drives the PROM. A short access time after $\overline{CE}$ and OE are enabled, data is available on the PROM DATA (D0) pin that is connected to the FPGA DIN pin. New data is available a short access time after each rising clock edge. The FPGA generates the appropriate number of clock pulses to complete the configuration. When the FPGA is in Slave Serial mode, the PROM and the FPGA are clocked by an external clock.

When the FPGA is in Master SelectMAP mode, the FPGA generates a configuration clock that drives the PROM. When the FPGA is in Slave Parallel or Slave SelectMAP mode, an external oscillator generates the configuration clock that drives the PROM and the FPGA. After $\overline{CE}$ and OE are enabled, data is available on the PROM's DATA (D0-D7) pins. New data is available a short access time after each rising clock edge. The data is clocked into the FPGA on the following rising edge of the CCLK. A free-running oscillator can be used in the Slave Parallel or Slave SelecMAP modes.

Multiple devices can be cascaded by using the $\overline{CEO}$ output to drive the $\overline{CE}$ input of the following device. The clock inputs and the DATA outputs of all PROMs in this chain are interconnected. All devices are compatible and can be cascaded with other members of the family or with the XC17V00 one-time programmable serial PROM family.

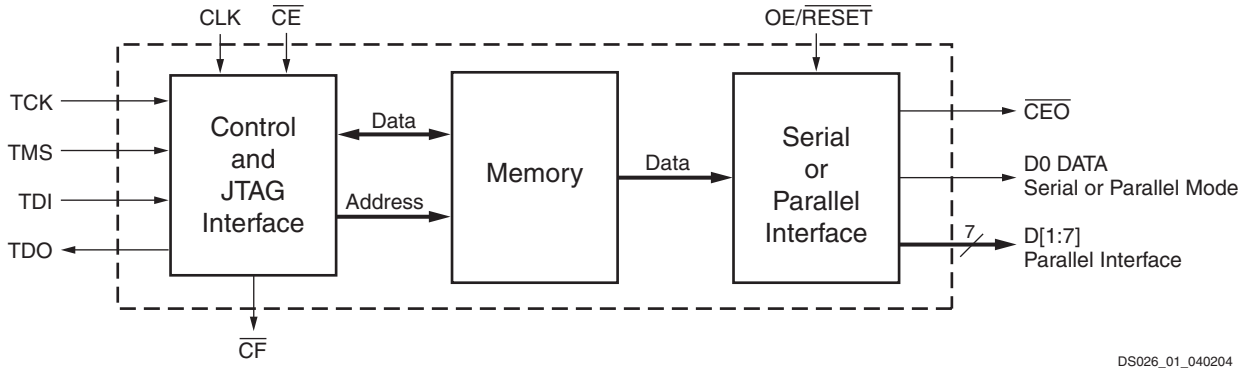


Figure 1: **XC18V00 Series Block Diagram**

Pinout and Pin Description

Table 1 provides a list of the pin names and descriptions for the 44-pin VQFP and PLCC and the 20-pin SOIC and PLCC packages.

Table 1: **Pin Names and Descriptions**

Pin Name	Boundary-Scan Order	Function	Pin Description	44-pin VQFP	44-pin PLCC	20-pin SOIC & PLCC
D0	4	DATA OUT	D0 is the DATA output pin to provide data for configuring an FPGA in serial mode.	40	2	1
	3	OUTPUT ENABLE				
D1	6	DATA OUT	D0-D7 are the output pins to provide parallel data for configuring a Xilinx FPGA in Slave Parallel/SelectMAP mode. D1-D7 remain in high-Z state when the PROM operates in serial mode. D1-D7 can be left unconnected when the PROM is used in serial mode.	29	35	16
	5	OUTPUT ENABLE				
D2	2	DATA OUT		42	4	2
	1	OUTPUT ENABLE				
D3	8	DATA OUT		27	33	15
	7	OUTPUT ENABLE				
D4	24	DATA OUT		9	15	7(1)
	23	OUTPUT ENABLE				
D5	10	DATA OUT		25	31	14
	9	OUTPUT ENABLE				
D6	17	DATA OUT		14	20	9
	16	OUTPUT ENABLE				
D7	14	DATA OUT		19	25	12
	13	OUTPUT ENABLE				
CLK	0	DATA IN	Each rising edge on the CLK input increments the internal address counter if both $\overline{CE}$ is Low and OE/$\overline{RESET}$ is High.	43	5	3
OE/$\overline{RESET}$	20	DATA IN	When Low, this input holds the address counter reset and the DATA output is in a high-Z state. This is a bidirectional open-drain pin that is held Low while the PROM is reset. Polarity is NOT programmable.	13	19	8
	19	DATA OUT				
	18	OUTPUT ENABLE				
CE	15	DATA IN	When $\overline{CE}$ is High, the device is put into low-power standby mode, the address counter is reset, and the DATA pins are put in a high-Z state.	15	21	10
CF	22	DATA OUT	Allows JTAG CONFIG instruction to initiate FPGA configuration without powering down FPGA. This is an open-drain output that is pulsed Low by the JTAG CONFIG command.	10	16	7(1)
	21	OUTPUT ENABLE				

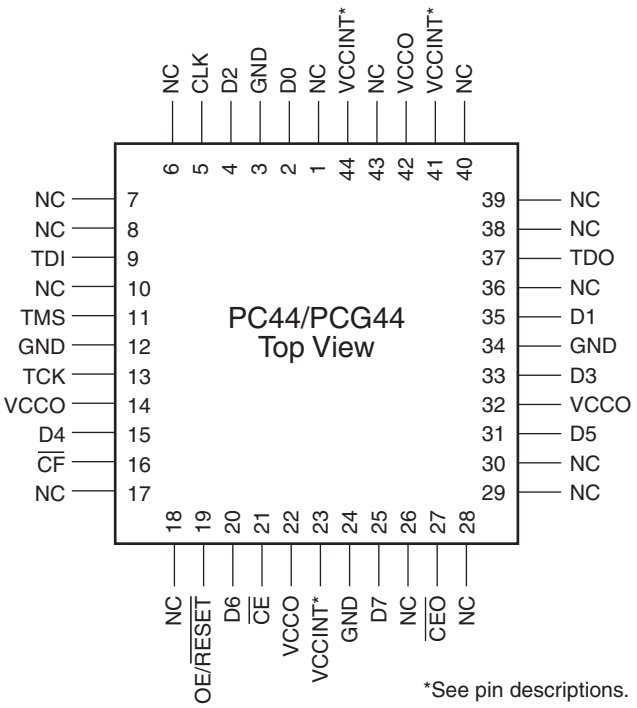
Table 1: **Pin Names and Descriptions *(Cont'd)***

Pin Name	Boundary-Scan Order	Function	Pin Description	44-pin VQFP	44-pin PLCC	20-pin SOIC & PLCC
CEO	12	DATA OUT	Chip Enable Output ($\overline{CEO}$) is connected to the $\overline{CE}$ input of the next PROM in the chain. This output is Low when $\overline{CE}$ is Low and OE/$\overline{RESET}$ input is High, AND the internal address counter has been incremented beyond its Terminal Count (TC) value. $\overline{CEO}$ returns to High when OE/$\overline{RESET}$ goes Low or $\overline{CE}$ goes High.	21	27	13
	11	OUTPUT ENABLE				
GND			GND is the ground connection.	6, 18, 28 & 41	3, 12, 24 & 34	11
TMS		MODE SELECT	The state of TMS on the rising edge of TCK determines the state transitions at the Test Access Port (TAP) controller. TMS has an internal 50 kΩ resistive pull-up to provide a logic 1 to the device if the pin is not driven.	5	11	5
TCK		CLOCK	This pin is the JTAG test clock. It sequences the TAP controller and all the JTAG test and programming electronics.	7	13	6
TDI		DATA IN	This pin is the serial input to all JTAG instruction and data registers. TDI has an internal 50 kΩ resistive pull-up to provide a logic 1 to the device if the pin is not driven.	3	9	4
TDO		DATA OUT	This pin is the serial output for all JTAG instruction and data registers. TDO has an internal 50 kΩ resistive pull-up to provide a logic 1 to the system if the pin is not driven.	31	37	17
V_{CCINT}			Positive 3.3V supply voltage for internal logic.	17, 35 & 38(3)	23, 41 & 44(3)	18 & 20(3)
V_{CCO}			Positive 3.3V or 2.5V supply voltage connected to the input buffers(2) and output voltage drivers.	8, 16, 26 & 36	14, 22, 32 & 42	19
NC			No connects.	1, 2, 4, 11, 12, 20, 22, 23, 24, 30, 32, 33, 34, 37, 39, 44	1, 6, 7, 8, 10, 17, 18, 26, 28, 29, 30, 36, 38, 39, 40, 43	

Notes:

1. By default, pin 7 is the D4 pin in the 20-pin packages. However, CF → D4 programming option can be set to override the default and route the CF function to pin 7 in the Serial mode.
2. For devices with IDCODES `0502x093h`, the input buffers are supplied by V_{CCINT}.
3. For devices with IDCODES `0503x093h`, the following V_{CCINT} pins are no-connects: pin 38 in 44-pin VQFP package, pin 44 in 44-pin PLCC package, and pin 20 in 20-pin SOIC and 20-pin PLCC packages.

Pinout Diagrams



*See pin descriptions.

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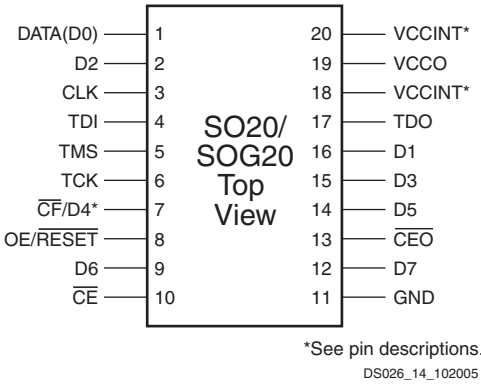

*See pin descriptions.

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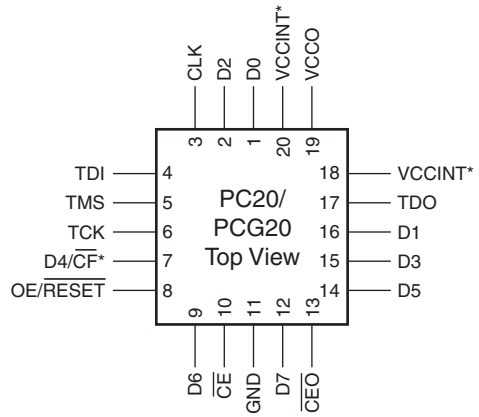

*See pin descriptions.

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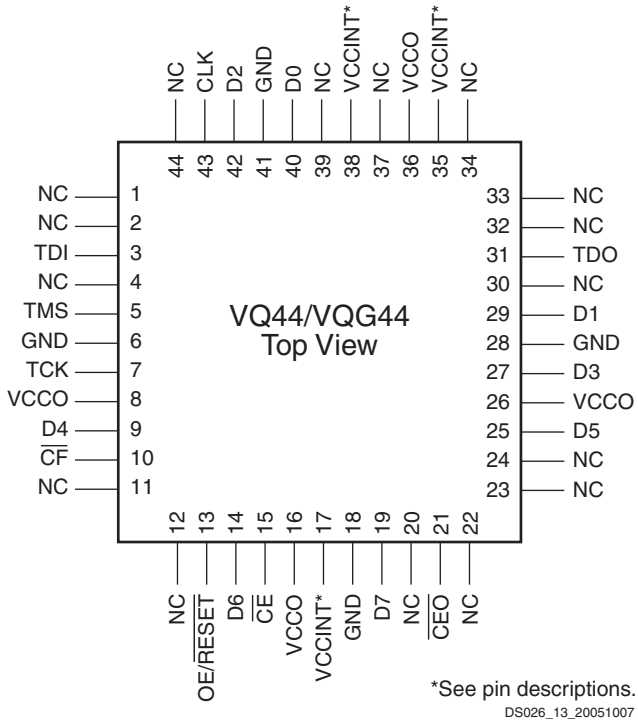

*See pin descriptions.

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Xilinx FPGAs and Compatible PROMs

Table 2 provides a list of Xilinx FPGAs and compatible PROMs.

Table 2: **Xilinx FPGAs and Compatible PROMs**

Device	Configuration Bits	XC18V00 Solution
XC2VP2	1,305,376	XC18V02
XC2VP4	3,006,496	XC18V04
XC2VP7	4,485,408	XC18V04 + XC18V512
XC2VP20	8,214,560	2 of XC18V04
XC2VP30	11,589,920	3 of XC18V04
XC2VP40	15,868,192	4 of XC18V04
XC2VP50	19,021,344	5 of XC18V04
XC2VP70	26,098,976	6 of XC18V04 + XC18V512
XC2VP100	34,292,768	8 of XC18V04 + XC18V512
XC2V40	470,048	XC18V512
XC2V80	732,576	XC18V01
XC2V250	1,726,880	XC18V02
XC2V500	2,767,520	XC18V04
XC2V1000	4,089,504	XC18V04
XC2V1500	5,667,488	XC18V04 + XC18V02
XC2V2000	7,501,472	2 of XC18V04
XC2V3000	10,505,120	3 of XC18V04
XC2V4000	15,673,248	4 of XC18V04
XC2V6000	21,865,376	5 of XC18V04 + XC18V02
XC2V8000	29,081,504	7 of XC18V04
XCV50	559,200	XC18V01
XCV100	781,216	XC18V01
XCV150	1,040,096	XC18V01
XCV200	1,335,840	XC18V02
XCV300	1,751,808	XC18V02
XCV400	2,546,048	XC18V04
XCV600	3,607,968	XC18V04
XCV800	4,715,616	XC18V04 + XC18V512
XCV1000	6,127,744	XC18V04 + XC18V02
XCV50E	630,048	XC18V01
XCV100E	863,840	XC18V01
XCV200E	1,442,016	XC18V02
XCV300E	1,875,648	XC18V02
XCV400E	2,693,440	XC18V04
XCV405E	3,430,400	XC18V04

Table 2: **Xilinx FPGAs and Compatible PROMs *(Cont'd)***

Device	Configuration Bits	XC18V00 Solution
XCV600E	3,961,632	XC18V04
XCV812E	6,519,648	2 of XC18V04
XCV1000E	6,587,520	2 of XC18V04
XCV1600E	8,308,992	2 of XC18V04
XCV2000E	10,159,648	3 of XC18V04
XCV2600E	12,922,336	4 of XC18V04
XCV3200E	16,283,712	4 of XC18V04
XC2S15	197,696	XC18V512
XC2S30	336,768	XC18V512
XC2S50	559,200	XC18V01
XC2S100	781,216	XC18V01
XC2S150	1,040,096	XC18V01
XC2S200	1,335,840	XC18V02
XC2S50E	630,048	XC18V01
XC2S100E	863,840	XC18V01
XC2S150E	1,134,496	XC18V02
XC2S200E	1,442,016	XC18V02
XC2S300E	1,875,648	XC18V02
XC2S400E	2,693,440	XC18V04
XC2S600E	3,961,632	XC18V04
XC3S50	439,264	XC18V512
XC3S200	1,047,616	XC18V01
XC3S400	1,699,136	XC18V02
XC3S1000	3,223,488	XC18V04
XC3S1500	5,214,784	XC18V04 + XC18V01
XC3S2000	7,673,024	2 of XC18V04
XC3S4000	11,316,864	3 of XC18V04
XC3S5000	13,271,936	3 of XC18V04 + XC18V01

Capacity

Devices	Configuration Bits
XC18V04	4,194,304
XC18V02	2,097,152
XC18V01	1,048,576
XC18V512	524,288

In-System Programming

In-System Programmable PROMs can be programmed individually, or two or more can be chained together and programmed in-system via the standard 4-pin JTAG protocol as shown in Figure 2. In-system programming offers quick and efficient design iterations and eliminates unnecessary package handling or socketing of devices. The Xilinx development system provides the programming data sequence using either Xilinx iMPACT software and a download cable, a third-party JTAG development system, a JTAG-compatible board tester, or a simple microprocessor interface that emulates the JTAG instruction sequence. The iMPACT software also outputs serial vector format (SVF) files for use with any tools that accept SVF format and with automatic test equipment.

All outputs are held in a high-Z state or held at clamp levels during in-system programming.

OE/$\overline{\text{RESET}}$

The ISP programming algorithm requires issuance of a reset that causes OE to go Low.

External Programming

Xilinx reprogrammable PROMs can also be programmed by a third-party device programmer, providing the added flexibility of using pre-programmed devices with an in-system programmable option for future enhancements and design changes.

Reliability and Endurance

Xilinx in-system programmable products provide a guaranteed endurance level of 20,000 in-system program/erase cycles and a minimum data retention of 20 years. Each device meets all functional, performance, and data retention specifications within this endurance limit. See the UG116, *Xilinx Device Reliability Report*, for device quality, reliability, and process node information.

Design Security

The Xilinx in-system programmable PROM devices incorporate advanced data security features to fully protect the programming data against unauthorized reading via JTAG. Table 3 shows the security setting available.

The read security bit can be set by the user to prevent the internal programming pattern from being read or copied via JTAG. When set, it allows device erase. Erasing the entire device is the only way to reset the read security bit.

Table 3: **Data Security Options**

Reset	Set
Read Allowed Program/Erase Allowed Verify Allowed	Read Inhibited via JTAG Program/Erase Allowed Verify Inhibited

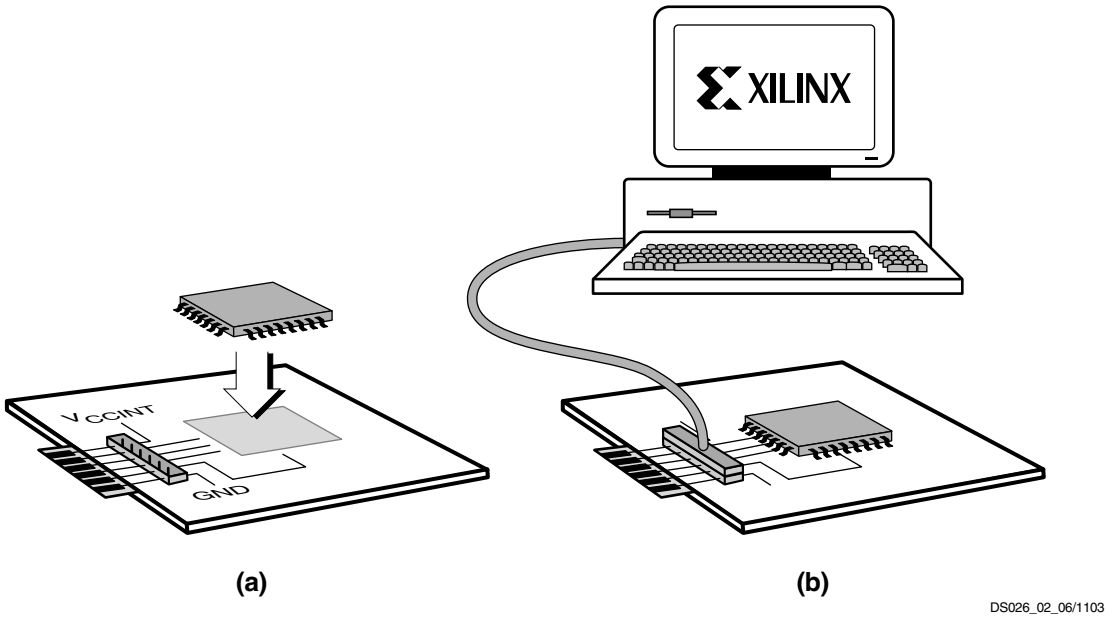


Figure 2: **In-System Programming Operation (a) Solder Device to PCB and (b) Program Using Download Cable**

IEEE 1149.1 Boundary-Scan (JTAG)

The XC18V00 family is fully compliant with the IEEE Std. 1149.1 Boundary-Scan, also known as JTAG. A Test Access Port (TAP) and registers are provided to support all required Boundary-Scan instructions, as well as many of the optional instructions specified by IEEE Std. 1149.1. In addition, the JTAG interface is used to implement in-system programming (ISP) to facilitate configuration, erasure, and verification operations on the XC18V00 device.

Table 4 lists the required and optional Boundary-Scan instructions supported in the XC18V00. Refer to the IEEE Std. 1149.1 specification for a complete description of Boundary-Scan architecture and the required and optional instructions.

Table 4: **Boundary-Scan Instructions**

Boundary-Scan Command	Binary Code [7:0]	Description
Required Instructions:		
BYPASS	11111111	Enables BYPASS
SAMPLE/ PRELOAD	00000001	Enables Boundary-Scan SAMPLE/PRELOAD operation
EXTEST	00000000	Enables Boundary-Scan EXTEST operation
Optional Instructions:		
CLAMP	11111010	Enables Boundary-Scan CLAMP operation
HIGHZ	11111100	All outputs in high-Z state simultaneously
IDCODE	11111110	Enables shifting out 32-bit IDCODE
USERCODE	11111101	Enables shifting out 32-bit USERCODE
XC18V00 Specific Instructions:		
CONFIG	11101110	Initiates FPGA configuration by pulsing $\overline{CF}$ pin Low once

Instruction Register

The Instruction Register (IR) for the XC18V00 is eight bits wide and is connected between TDI and TDO during an instruction scan sequence. In preparation for an instruction scan sequence, the instruction register is parallel loaded with a fixed instruction capture pattern. This pattern is shifted out onto TDO (LSB first), while an instruction is shifted into the instruction register from TDI. The detailed composition of the instruction capture pattern is illustrated in Figure 3.

The ISP Status field, IR(4), contains logic "1" if the device is currently in ISP mode; otherwise, it contains logic "0". The Security field, IR(3), contains logic "1" if the device has been programmed with the security option turned on; otherwise, it contains logic "0".

	IR[7:5]	IR[4]	IR[3]	IR[2]	IR[1:0]	
TDI →	000	ISP Status	Security	0	01(1)	→ TDO

Notes:

1. IR[1:0] = 01 is specified by IEEE Std. 1149.1

Figure 3: **Instruction Register Values Loaded into IR as Part of an Instruction Scan Sequence**

Boundary-Scan Register

The Boundary-Scan register is used to control and observe the state of the device pins during the EXTEST, SAMPLE/PRELOAD, and CLAMP instructions. Each output pin on the XC18V00 has two register stages that contribute to the Boundary-Scan register, while each input pin only has one register stage.

For each output pin, the register stage nearest to TDI controls and observes the output state, and the second stage closest to TDO controls and observes the high-Z enable state of the pin.

For each input pin, the register stage controls and observes the input state of the pin.

Identification Registers

The IDCODE is a fixed, vendor-assigned value that is used to electrically identify the manufacturer and type of the device being addressed. The IDCODE register is 32 bits wide. The IDCODE register can be shifted out for examination by using the IDCODE instruction. The IDCODE is available to any other system component via JTAG.

See Table 5 for the XC18V00 IDCODE values.

The IDCODE register has the following binary format:

```
vvvv:ffff:ffff:aaaa:aaaa:cccc:cccc:ccc1
```

where

v = the die version number

f = the family code (50h for XC18V00 family)

a = the ISP PROM product ID (26h or 36h for the XC18V04)

c = the company code (49h for Xilinx)

Note: *The LSB of the IDCODE register is always read as logic "1" as defined by IEEE Std. 1149.1.*

Table 5 lists the IDCODE register values for XC18V00 devices.

Table 5: **IDCODES Assigned to XC18V00 Devices**

ISP-PROM	IDCODE
XC18V01	05024093h or <v>5034093h
XC18V02	05025093h or <v>5035093h
XC18V04	05026093h or <v>5036093h
XC18V512	05023093h or <v>5033093h

Notes:

1. The <v> in the IDCODE field represents the device's revision code (in hex), and may vary.

The USERCODE instruction gives access to a 32-bit user programmable scratch pad typically used to supply information about the device's programmed contents. By using the USERCODE instruction, a user-programmable identification code can be shifted out for examination. This code is loaded into the USERCODE register during programming of the XC18V00 device. If the device is blank or was not loaded during programming, the USERCODE register contains FFFFFFFFh.

XC18V00 TAP Characteristics

The XC18V00 family performs both in-system programming and IEEE 1149.1 Boundary-Scan (JTAG) testing via a single four-wire Test Access Port (TAP). This simplifies system designs and allows standard Automatic Test Equipment to perform both functions. The AC characteristics of the XC18V00 TAP are described as follows.

TAP Timing

Figure 4 shows the timing relationships of the TAP signals. These TAP timing characteristics are identical for both Boundary-Scan and ISP operations.

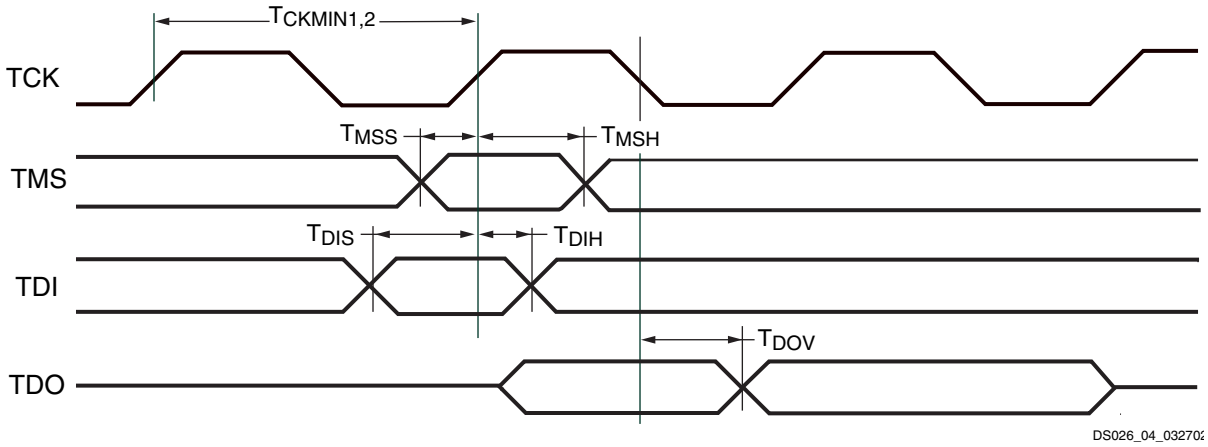


Figure 4: **Test Access Port Timing**

TAP AC Parameters

Table 6 shows the timing parameters for the TAP waveforms shown in Figure 4.

Table 6: **Test Access Port Timing Parameters**

Symbol	Parameter	Min	Max	Units
T_{CKMIN1}	TCK minimum clock period	100	–	ns
T_{CKMIN2}	TCK minimum clock period, Bypass mode	50	–	ns
T_{MSS}	TMS setup time	10	–	ns
T_{MSH}	TMS hold time	25	–	ns
T_{DIS}	TDI setup time	10	–	ns
T_{DIH}	TDI hold time	25	–	ns
T_{DOV}	TDO valid delay	–	25	ns

Connecting Configuration PROMs

Connecting the FPGA device with the configuration PROM (see Figure 5 and Figure 6).

- The DATA output(s) of the PROM(s) drives the DIN input of the lead FPGA device.
- The Master FPGA CCLK output drives the CLK input(s) of the PROM(s) (in Master Serial and Master SelectMAP modes only).
- The $\overline{CEO}$ output of a PROM drives the $\overline{CE}$ input of the next PROM in a daisy chain (if any).
- The OE/$\overline{RESET}$ pins of all PROMs are connected to the $\overline{INIT}$ pins of all FPGA devices. This connection assures that the PROM address counter is reset before the start of any (re)configuration, even when a reconfiguration is initiated by a V_{CCINT} glitch.
- The PROM $\overline{CE}$ input can be driven from the DONE pin. The $\overline{CE}$ input of the first (or only) PROM can be driven by the DONE output of all target FPGA devices, provided that DONE is not permanently grounded. $\overline{CE}$ can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary supply current of 10 mA maximum.
- Slave Parallel/SelectMap mode is similar to slave serial mode. The DATA is clocked out of the PROM one byte per CCLK instead of one bit per CCLK cycle. See FPGA data sheets for special configuration requirements.

Initiating FPGA Configuration

The XC18V00 devices incorporate a pin named $\overline{CF}$ that is controllable through the JTAG CONFIG instruction. Executing the CONFIG instruction through JTAG pulses the $\overline{CF}$ Low once for 300–500 ns, which resets the FPGA and initiates configuration.

The $\overline{CF}$ pin must be connected to the $\overline{PROGRAM}$ pin on the FPGA(s) to use this feature.

The iMPACT software can also issue a JTAG CONFIG command to initiate FPGA configuration through the “Load FPGA” setting.

The 20-pin packages do not have a dedicated $\overline{CF}$ pin. For 20-pin packages, the CF → D4 setting can be used to route the $\overline{CF}$ pin function to pin 7 only if the parallel output mode is *not* used.

Selecting Configuration Modes

The XC18V00 accommodates serial and parallel methods of configuration. The configuration modes are selectable through a user control register in the XC18V00 device. This control register is accessible through JTAG, and is set using the “Parallel mode” setting on the Xilinx iMPACT software. Serial output is the default configuration mode.

Master Serial Mode Summary

The I/O and logic functions of the FPGA’s configurable logic block (CLB) and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the three FPGA mode pins. In Master Serial mode, the FPGA automatically loads the configuration program from an external memory. Xilinx PROMs are designed to accommodate the Master Serial mode.

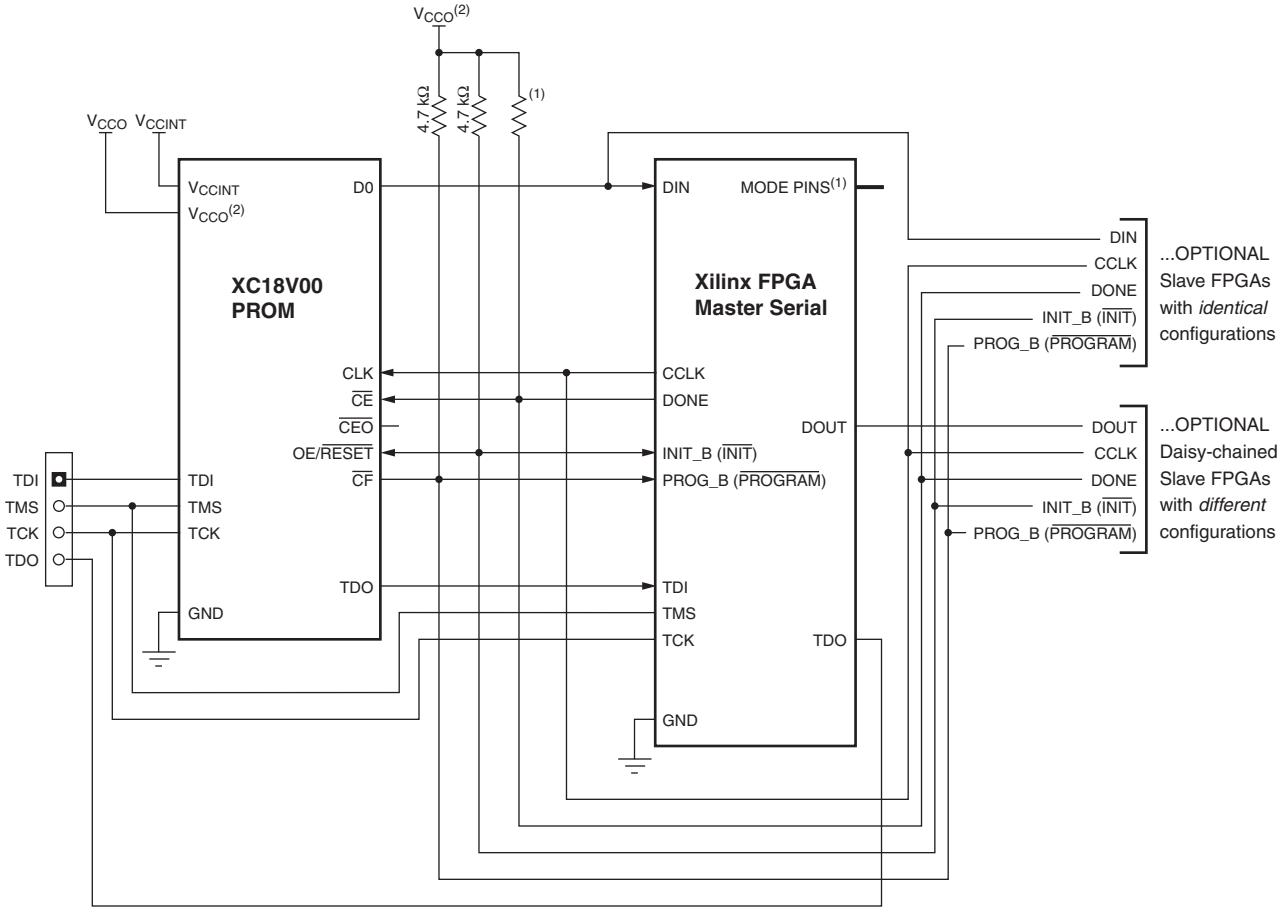
Upon power-up or reconfiguration, an FPGA enters the Master Serial mode whenever all three of the FPGA mode-select pins are Low (M0=0, M1=0, M2=0). Data is read from the PROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated by the FPGA during configuration.

Master Serial mode provides a simple configuration interface. Only a serial data line, a clock line, and two control lines are required to configure an FPGA. Data from the PROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CCLK. If the user-programmable, dual-function DIN pin on the FPGA is used only for configuration, it must still be held at a defined level during normal operation. The Xilinx FPGA families take care of this automatically with an on-chip pull-up resistor.

Cascading Configuration PROMs

For multiple FPGAs configured as a serial daisy-chain, or a single FPGA requiring larger configuration memories in a serial or SelectMAP configuration mode, cascaded PROMs provide additional memory (Figure 7 and Figure 8). Multiple XC18V00 devices can be cascaded by using the $\overline{CEO}$ output to drive the $\overline{CE}$ input of the downstream device. The clock inputs and the data outputs of all XC18V00 devices in the chain are interconnected. After the last data from the first PROM is read, the next clock signal to the PROM asserts its $\overline{CEO}$ output Low and drives its DATA line to a high-Z state. The second PROM recognizes the Low level on its $\overline{CE}$ input and enables its DATA output.

After configuration is complete, address counters of all cascaded PROMs are reset if the PROM OE/$\overline{RESET}$ pin goes Low or $\overline{CE}$ goes High.



Notes:
1 For MODE pin connections and DONE pin pullup value, refer to the appropriate FPGA data sheet or user guide.
2 For compatible voltages, refer to the appropriate data sheet.

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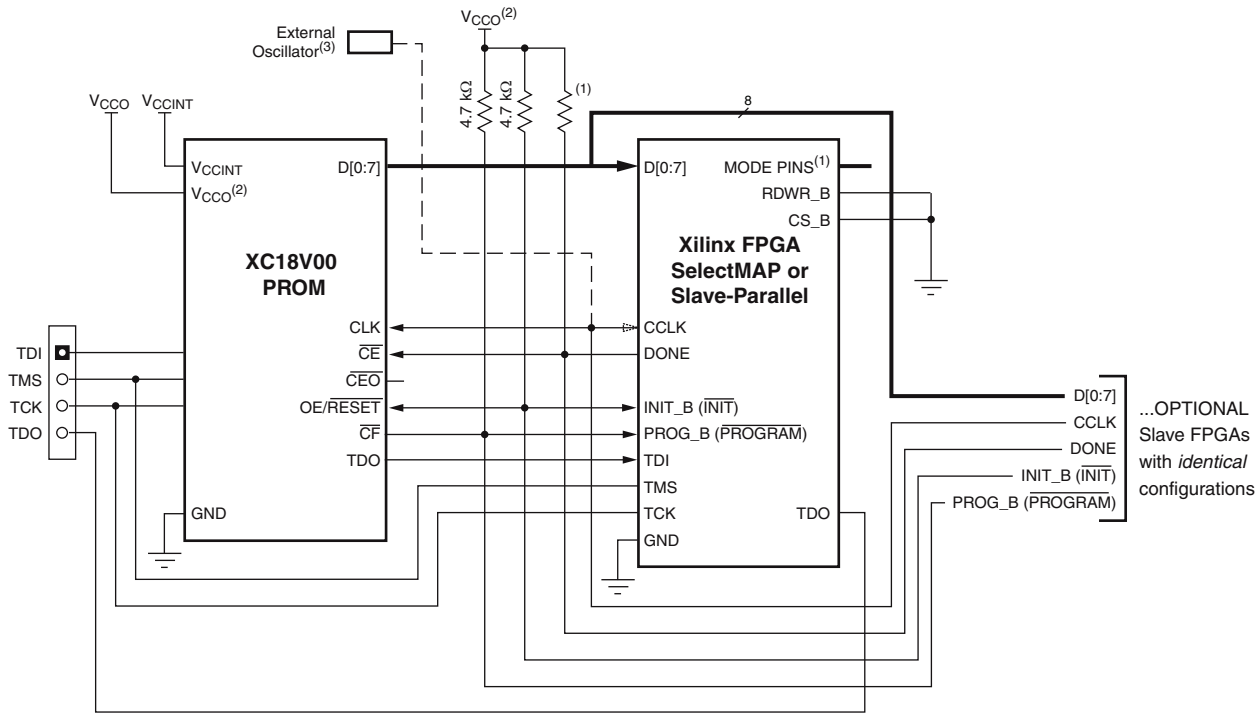
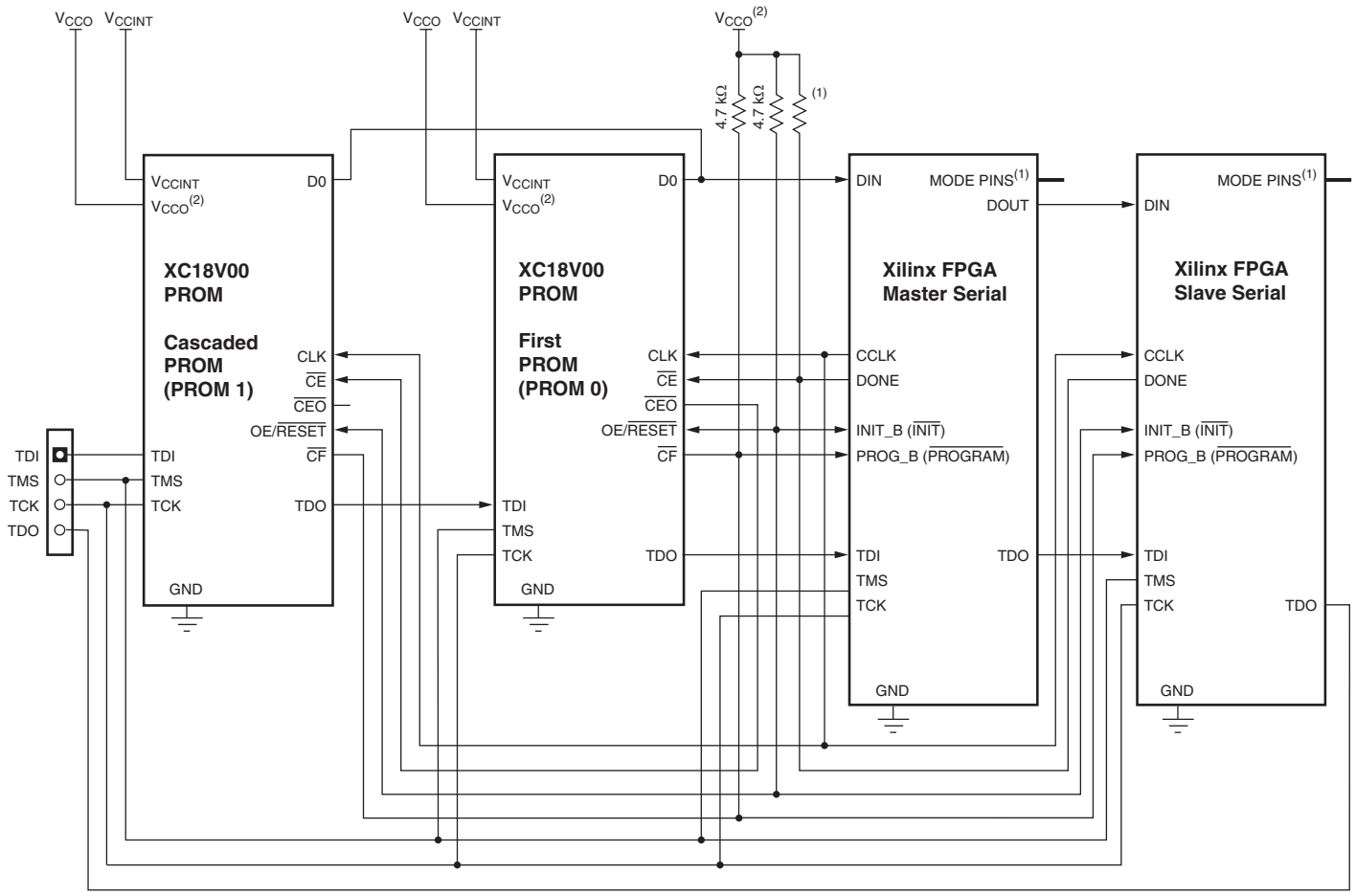
Figure 5: **Master Serial Mode**



Notes:
1 For MODE pin connections and DONE pin pullup value, refer to the appropriate FPGA data sheet or user guide.
2 For compatible voltages, refer to the appropriate data sheet.
3 External oscillator required for Virtex/Virtex-E SelectMAP, for Virtex-II/Virtex-II Pro Slave SelectMAP, and for Spartan-II/Spartan-IIE Slave-Parallel modes.

DS026_19_111207

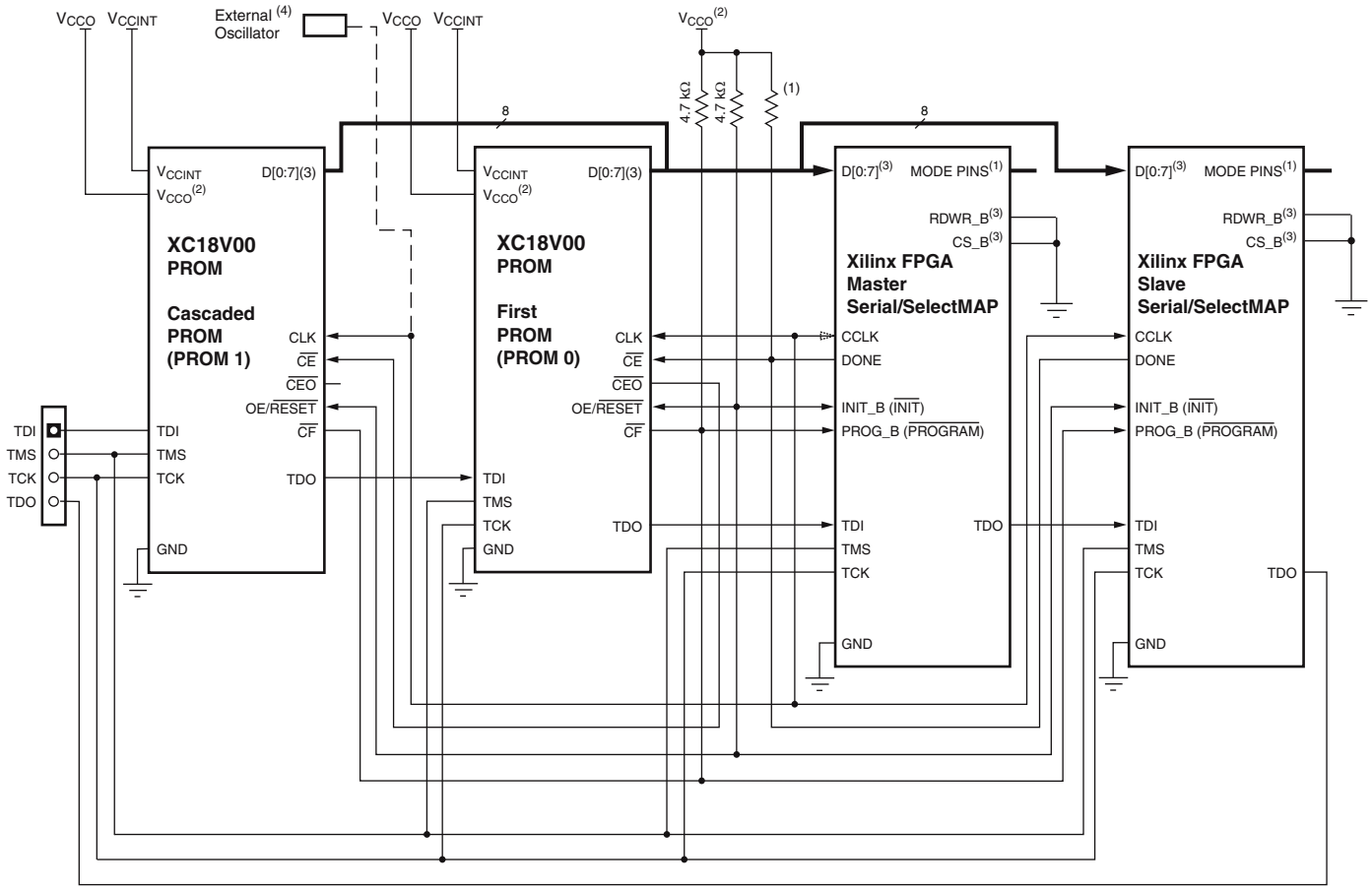
Figure 6: **Master/Slave SelectMAP Mode or Slave Parallel Mode**



Notes:
1 For MODE pin connections and DONE pin pullup value, refer to the appropriate FPGA data sheet or user guide.
2 For compatible voltages, refer to the appropriate data sheet.

ds026_16_20051007

Figure 7: **Configuring Multiple Devices in Master/Slave Serial Mode**



Notes:
1 For MODE pin connections and DONE pin pullup value, refer to the appropriate FPGA data sheet or user guide.
2 For compatible voltages, refer to the appropriate data sheet.
3 Serial modes do not require the D[1:7], RDWR_B, or CS_B pins to be connected.
4 External oscillator required if CLK is not supplied by an FPGA in Master mode. Refer to the appropriate FPGA data sheet.

DS026_17_111207

Figure 8: **Configuring Multiple Devices with Identical Patterns in Master/Slave Serial, Master/Slave SelectMAP, or Master/Slave Parallel Mode**

Reset and Power-On Reset Activation

At power up, the device requires the V_{CCINT} power supply to rise monotonically to the nominal operating voltage within the specified V_{CCINT} rise time. If the power supply cannot meet this requirement, then the device might not perform power-on reset properly. During the power-up sequence, OE/$\overline{\text{RESET}}$ is held Low by the PROM.

Once the required supplies have reached their respective POR (Power On Reset) thresholds, the OE/$\overline{\text{RESET}}$ release is delayed (T_{OER} minimum) to allow more margin for the power supplies to stabilize before initiating configuration. The OE/$\overline{\text{RESET}}$ pin is connected to an external pull-up resistor and also to the target FPGA's INIT_B pin. For systems utilizing slow-rising power supplies, an additional power monitoring circuit can be used to delay the target configuration until the system power reaches minimum operating voltages by holding the OE/$\overline{\text{RESET}}$ pin Low.

When OE/$\overline{\text{RESET}}$ is released, the FPGA's INIT_B pin is pulled High, allowing the FPGA's configuration sequence to begin. If the power drops below the power-down threshold (V_{CCPD}), the PROM resets and OE/$\overline{\text{RESET}}$ is again held Low until the after the POR threshold is reached. OE/$\overline{\text{RESET}}$ polarity is not programmable. These power-up requirements are shown graphically in Figure 9.

For a fully powered Platform Flash PROM, a reset occurs whenever OE/$\overline{\text{RESET}}$ is asserted (Low) or $\overline{\text{CE}}$ is deasserted (High). The address counter is reset, $\overline{\text{CEO}}$ is driven High, and the remaining outputs are placed in a high-Z state.

Standby Mode

The PROM enters a low-power standby mode whenever $\overline{\text{CE}}$ is asserted High. The address is reset. The output remains in a high-Z state regardless of the state of the OE input. JTAG pins TMS, TDI and TDO can be in a high-Z state or High. See Table 7.

When using the FPGA DONE signal to drive the PROM $\overline{\text{CE}}$ pin High to reduce standby power after configuration, an external pull-up resistor should be used. Typically a 330Ω pull-up resistor is used, but refer to the appropriate FPGA data sheet for the recommended DONE pin pull-up value. If the DONE circuit is connected to an LED to indicate FPGA configuration is complete, and also connected to the PROM $\overline{\text{CE}}$ pin to enable low-power standby mode, then an external buffer should be used to drive the LED circuit to ensure valid transitions on the PROMs $\overline{\text{CE}}$ pin. If low-power standby mode is not required for the PROM, then the $\overline{\text{CE}}$ pin should be connected to ground.

5V Tolerant I/Os

The I/Os on each re-programmable PROM are fully 5V tolerant even through the core power supply is 3.3V. This allows 5V CMOS signals to connect directly to the PROM inputs without damage. In addition, the 3.3V V_{CCINT} power supply can be applied before or after 5V signals are applied to the I/Os. In mixed 5V/3.3V/2.5V systems, the user pins, the core power supply (V_{CCINT}), and the output power supply (V_{CCO}) can have power applied in any order. This makes the PROM devices immune to power supply sequencing issues.

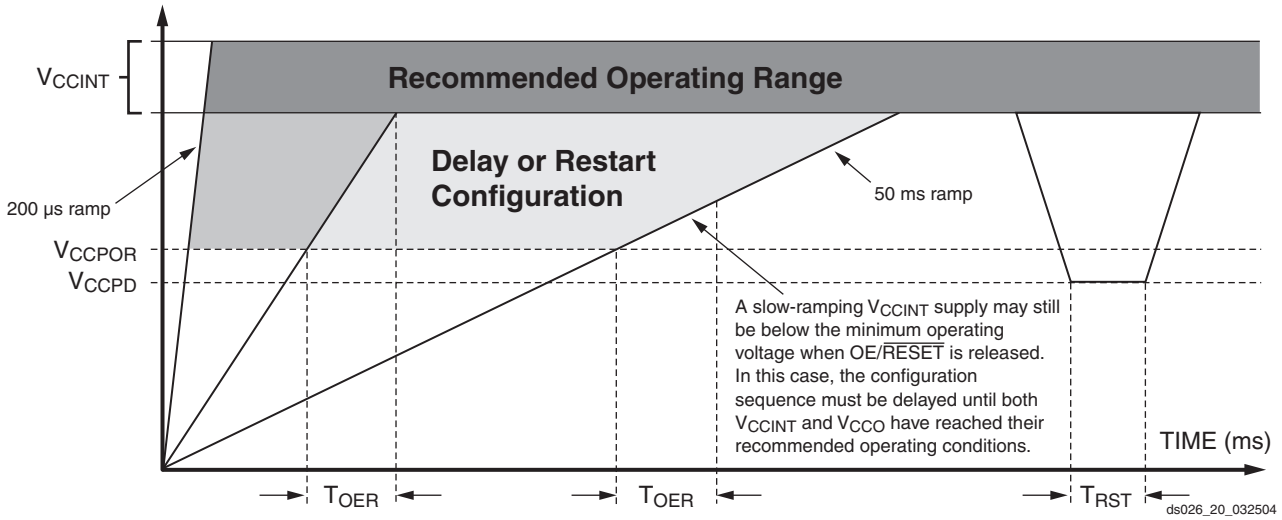


Figure 9: **V_{CCINT} Power-Up Requirements**

Customer Control Bits

The XC18V00 PROMs have various control bits accessible by the customer. These can be set after the array has been programmed using “Skip User Array” in Xilinx iMPACT software. The iMPACT software can set these bits to enable the optional JTAG read security, parallel configuration mode, or CF → D4 pin function. See Table 7.

Table 7: **Truth Table for PROM Control Inputs**

Control Inputs		Internal Address	Outputs		
OE/$\overline{\text{RESET}}$	CE		DATA	CEO	I_{CC}
High	Low	If address ≤ TC(1): increment If address > TC(1): don’t change	Active high-Z	High Low	Active reduced
Low	Low	Held reset	High-Z	High	Active
High	High	Held reset	High-Z	High	Standby
Low	High	Held reset	High-Z	High	Standby

Notes:

1. TC = Terminal Count = highest address value. TC + 1 = address 0.

Absolute Maximum Ratings(1,2)

Symbol	Description	Value	Units
V_{CCINT}/V_{CCO}	Supply voltage relative to GND	–0.5 to +4.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to +5.5	V
V_{TS}	Voltage applied to high-Z output	–0.5 to +5.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_J	Junction temperature	+125	°C

Notes:

1. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins can undershoot to –2.0V or overshoot to +7.0V, provided this over- or undershoot lasts less then 10 ns and with the forcing current being limited to 200 mA.
2. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Supply Voltage Requirements for Power-On Reset and Power-Down

Symbol	Description	Min	Max	Units
T_{VCC}	V_{CCINT} rise time from 0V to nominal voltage(2)	0.2	50	ms
V_{CCPOR}	POR threshold for the V_{CCINT} supply	1	–	V
T_{OER}	OE/$\overline{\text{RESET}}$ release delay following POR(3)	0	1	ms
T_{RST}	Time required to trigger a device reset when the V_{CCINT} supply drops below the maximum V_{CCPD} threshold	10	–	ms
V_{CCPD}	Power-down threshold for V_{CCINT} supply	-	1	V

Notes:

1. V_{CCINT} and V_{CCO} supplies can be applied in any order.
2. At power up, the device requires the V_{CCINT} power supply to rise monotonically to the nominal operating voltage within the specified T_{VCC} rise time. If the power supply cannot meet this requirement, then the device might not perform power-on-reset properly. See Figure 9, page 14.
3. If the V_{CCINT} and V_{CCO} supplies do not reach their respective recommended operating conditions before the OE/$\overline{\text{RESET}}$ pin is released, then the configuration data from the PROM will not be available at the recommended threshold levels. The configuration sequence must be delayed until both V_{CCINT} and V_{CCO} have reached their recommended operating conditions.
4. Typical POR is value is 2.0V.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CCINT}	Internal voltage supply	3.0	3.6	V
V_{CCO}	Supply voltage for output drivers for 3.3V operation	3.0	3.6	V
	Supply voltage for output drivers for 2.5V operation	2.3	2.7	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{IH}	High-level input voltage	2.0	5.5	V
V_O	Output voltage	0	V_{CCO}	V
T_{VCC}	V_{CCINT} rise time from 0V to nominal voltage(1)	1	50	ms
T_A	Operating ambient temperature(2)	–40	85	°C

Notes:

1. At power up, the device requires the V_{CCINT} power supply to rise monotonically from 0V to nominal voltage within the specified V_{CCINT} rise time. If the power supply cannot meet this requirement, then the device might not perform power-on-reset properly. See Figure 9, page 14.
2. Covers the industrial temperature range.

Quality and Reliability Characteristics

Symbol	Description	Min	Max	Units
T_{DR}	Data retention	20	–	Years
N_{PE}	Program/erase cycles (Endurance)	20,000	–	Cycles
V_{ESD}	Electrostatic discharge (ESD)	2,000	–	Volts

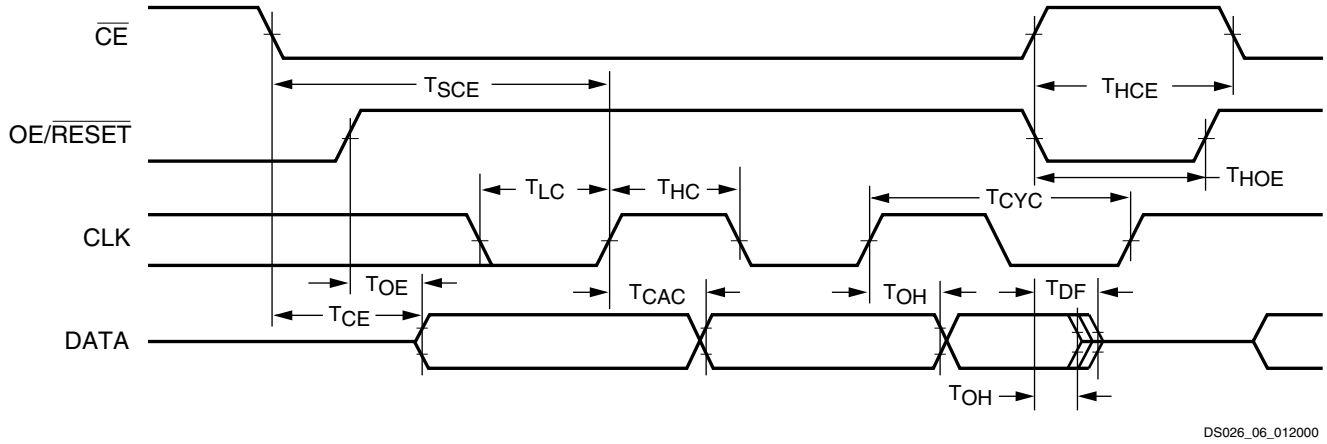
DC Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	High-level output voltage for 3.3V outputs	I_{OH} = –4 mA	2.4	–	V
	High-level output voltage for 2.5V outputs	I_{OH} = –500 µA	90% V_{CCO}	–	V
V_{OL}	Low-level output voltage for 3.3V outputs	I_{OL} = 8 mA	–	0.4	V
	Low-level output voltage for 2.5V outputs	I_{OL} = 500 µA	–	0.4	V
I_{CC}	Supply current, active mode	25 MHz	–	25	mA
I_{CCS}	Supply current, standby mode		–	10	mA
I_{ILJ}	JTAG pins TMS, TDI, and TDO pull-up current (1)	V_{CCINT} = MAX V_{IN} = GND	–	100	µA
I_{IL}	Input leakage current	V_{CCINT} = Max V_{IN} = GND or V_{CCINT}	–10	10	µA
I_{IH}	Input and output high-Z leakage current	V_{CCINT} = Max V_{IN} = GND or V_{CCINT}	–10	10	µA
C_{IN}	Input capacitance	V_{IN} = GND f = 1.0 MHz	–	8	pF
C_{OUT}	Output capacitance	V_{OUT} = GND f = 1.0 MHz	–	14	pF

Notes:

1. Internal pull-up resistors guarantee valid logic levels at unconnected input pins. These pull-up resistors do not guarantee valid logic levels when input pins are connected to other circuits.

AC Characteristics Over Operating Conditions for XC18V04 and XC18V02

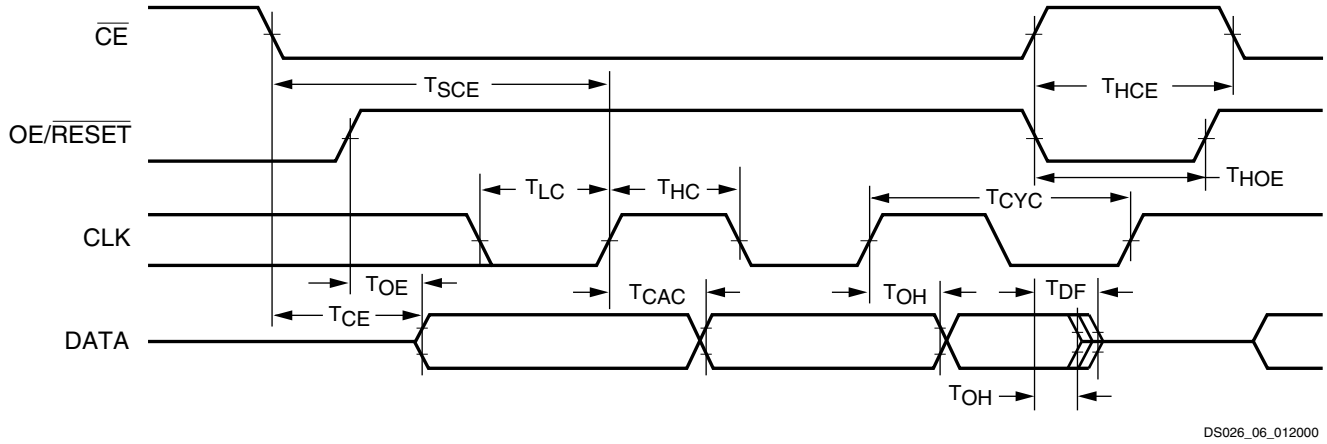


Symbol	Description	Min	Max	Units
T_{OE}	OE/$\overline{\text{RESET}}$ to data delay	–	10	ns
T_{CE}	$\overline{\text{CE}}$ to data delay	–	20	ns
T_{CAC}	CLK to data delay	–	20	ns
T_{OH}	Data hold from $\overline{\text{CE}}$, OE/$\overline{\text{RESET}}$, or CLK	0	-	ns
T_{DF}	$\overline{\text{CE}}$ or OE/$\overline{\text{RESET}}$ to data float delay(2)	–	25	ns
T_{CYC}	Clock periods	50	–	ns
T_{LC}	CLK Low time(3)	10	–	ns
T_{HC}	CLK High time(3)	10	–	ns
T_{SCE}	$\overline{\text{CE}}$ setup time to CLK (guarantees proper counting)(3)	25	–	ns
T_{HCE}	$\overline{\text{CE}}$ High time (guarantees counters are reset)	250	–	ns
T_{HOE}	OE/$\overline{\text{RESET}}$ hold time (guarantees counters are reset)	250	–	ns

Notes:

1. AC test load = 50 pF.
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
5. If T_{HCE} High < 2 µs, T_{CE} = 2 µs.
6. If T_{HOE} Low < 2 µs, T_{OE} = 2 µs.

AC Characteristics Over Operating Conditions for XC18V01 and XC18V512

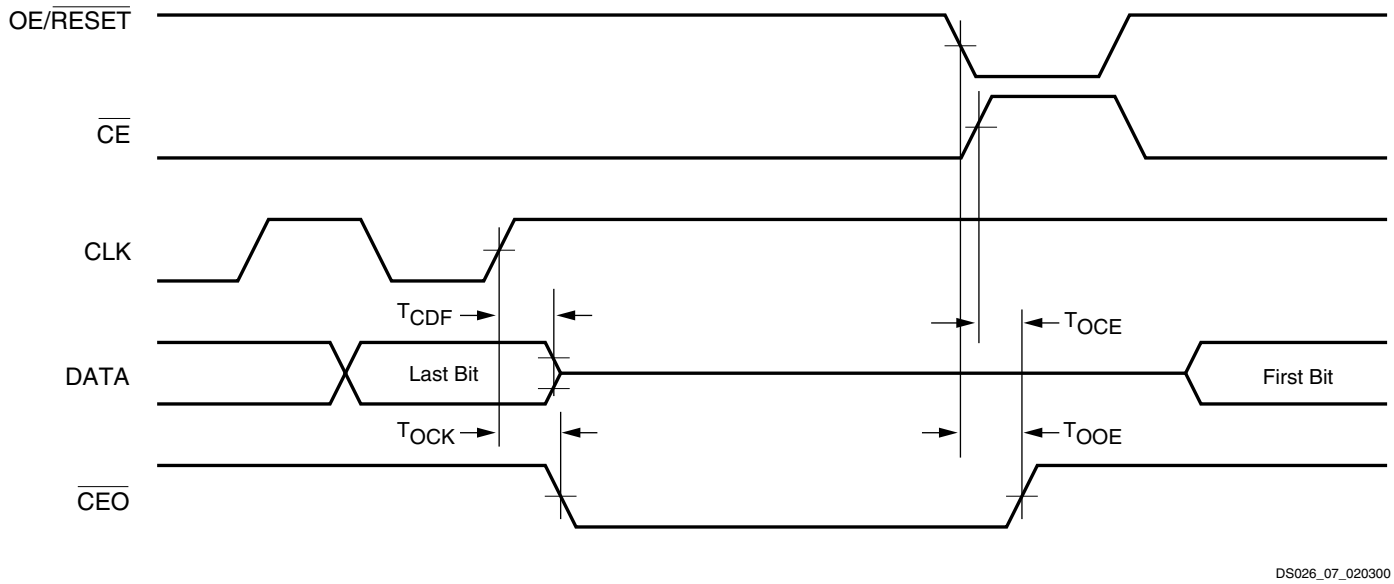


Symbol	Description	Min	Max	Units
T_{OE}	OE/$\overline{\text{RESET}}$ to data delay	–	10	ns
T_{CE}	$\overline{\text{CE}}$ to data delay	–	15	ns
T_{CAC}	CLK to data delay	–	15	ns
T_{OH}	Data hold from $\overline{\text{CE}}$, OE/$\overline{\text{RESET}}$, or CLK	0	–	ns
T_{DF}	$\overline{\text{CE}}$ or OE/$\overline{\text{RESET}}$ to data float delay(2)	–	25	ns
T_{CYC}	Clock periods	30	–	ns
T_{LC}	CLK Low time(3)	10	–	ns
T_{HC}	CLK High time(3)	10	–	ns
T_{SCE}	$\overline{\text{CE}}$ setup time to CLK (guarantees proper counting)(3)	20	–	ns
T_{HCE}	$\overline{\text{CE}}$ High time (guarantees counters are reset)	250	–	ns
T_{HOE}	OE/$\overline{\text{RESET}}$ hold time (guarantees counters are reset)	250	–	ns

Notes:

1. AC test load = 50 pF.
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
5. If T_{HCE} High < 2 µs, T_{CE} = 2 µs.
6. If T_{HOE} Low < 2 µs, T_{OE} = 2 µs.

AC Characteristics Over Operating Conditions When Cascading for XC18V04 and XC18V02

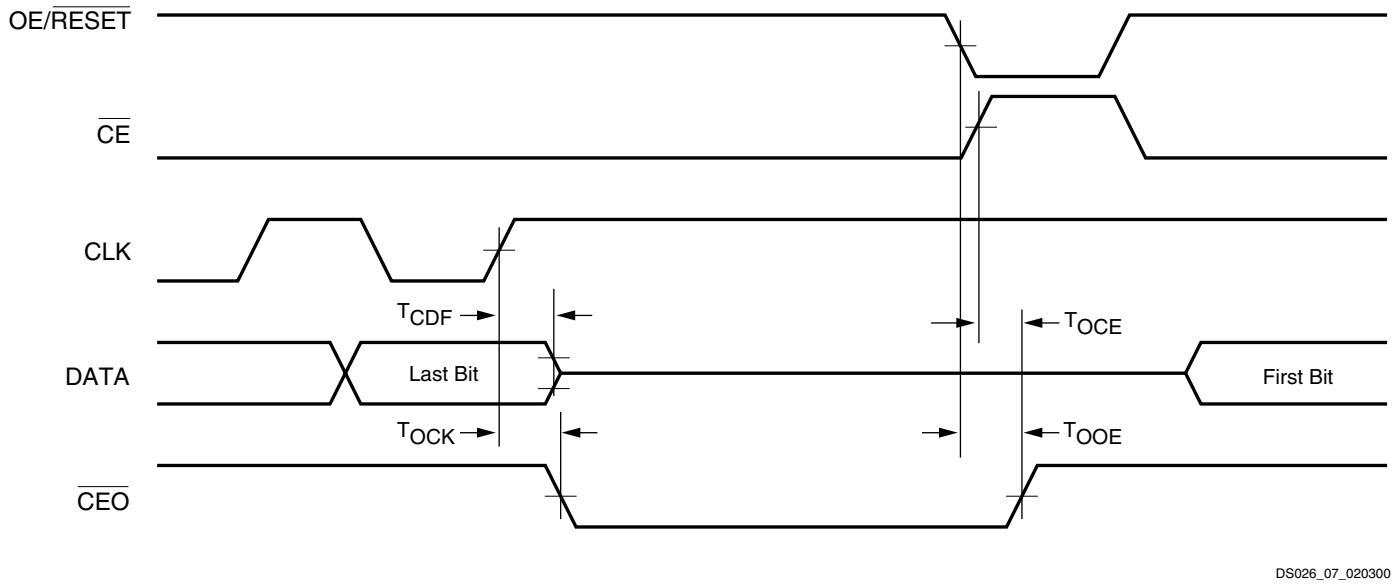


Symbol	Description	Min	Max	Units
T_{CDF}	CLK to data float delay(2,3)	–	25	ns
T_{OCK}	CLK to $\overline{CEO}$ delay(3)	–	20	ns
T_{OCE}	CE to $\overline{CEO}$ delay(3)	–	20	ns
T_{OOE}	OE/$\overline{RESET}$ to $\overline{CEO}$ delay(3)	–	20	ns

Notes:

1. AC test load = 50 pF.
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
5. For cascade mode:
   - T_{CYC} min = T_{OCK} + T_{CE} + FPGA DIN-to-CCLK setup time
   - T_{CAC} min = T_{OCK} + T_{CE}

AC Characteristics Over Operating Conditions When Cascading for XC18V01 and XC18V512



Symbol	Description	Min	Max	Units
T_{CDF}	CLK to data float delay(2,3)	–	25	ns
T_{OCK}	CLK to $\overline{CEO}$ delay(3)	–	20	ns
T_{OCE}	CE to $\overline{CEO}$ delay(3)	–	20	ns
T_{OOE}	OE/$\overline{RESET}$ to $\overline{CEO}$ delay(3)	–	20	ns

Notes:

1. AC test load = 50 pF.
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
5. For cascade mode:
   - T_{CYC} min = T_{OCK} + T_{CE} + FPGA DIN-to-CCLK setup time
   - T_{CAC} min = T_{OCK} + T_{CE}

Ordering Information

XC18V04 VQ44 C

Device Number

XC18V04
XC18V02
XC18V01
XC18V512

Package Type

VQ44 = 44-pin Plastic Quad Flat Package
VQG44 = 44-pin Plastic Quad Flat Package, Pb-free
PC44 = 44-pin Plastic Chip Carrier(1)
PCG44 = 44-pin Plastic Chip Carrier, Pb-free(1)
SO20 = 20-pin Small-Outline Package(2)
SOG20 = 20-pin Small-Outline Package, Pb-free(2)
PC20 = 20-pin Plastic Leaded Chip Carrier(2)
PCG20 = 20-pin Plastic Leaded Chip Carrier, Pb-free(2)

Operating Range

C = Industrial (T_A = –40°C to +85°C)

Notes:

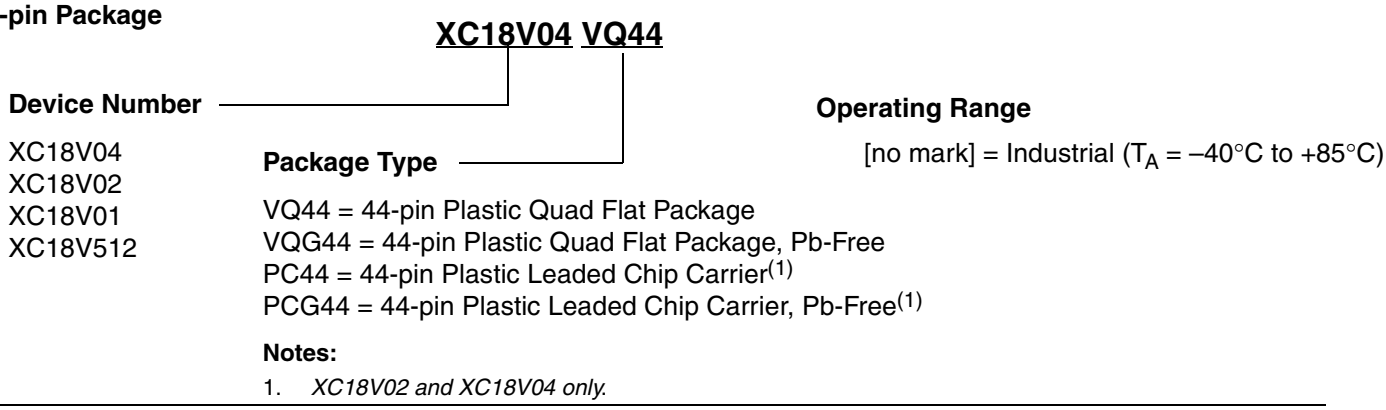
1. XC18V04 and XC18V02 only.
2. XC18V01 and XC18V512 only.

Valid Ordering Combinations

XC18V04VQ44C	XC18V02VQ44C	XC18V01VQ44C	XC18V512VQ44C
XC18V04PC44C	XC18V02PC44C	XC18V01PC20C	XC18V512PC20C
XC18V04VQG44C	XC18V02VQG44C	XC18V01SO20C	XC18V512SO20C
XC18V04PCG44C	XC18V02PCG44C	XC18V01VQG44C	XC18V512VQG44C
		XC18V01PCG20C	XC18V512PCG20C
		XC18V01SOG20C	XC18V512SOG20C

Marking Information

44-pin Package

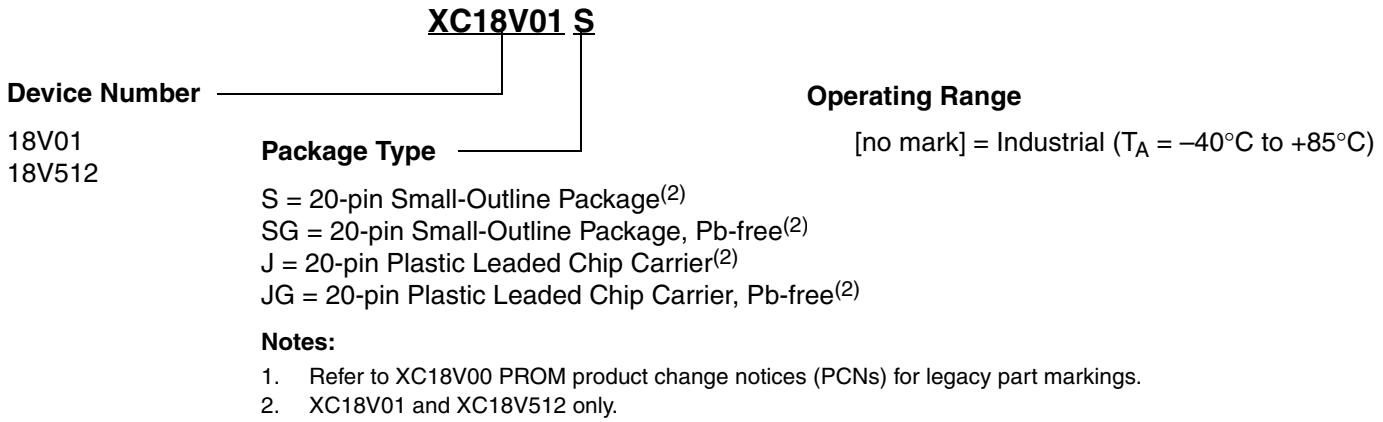


Notes:

1. *XC18V02 and XC18V04 only.*

20-pin Package(1)

Due to the small size of the serial PROM packages, the complete ordering part number cannot be marked on the package. The package code is simplified. Device marking is as follows:



Notes:

1. Refer to XC18V00 PROM product change notices (PCNs) for legacy part markings.
2. XC18V01 and XC18V512 only.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/09/1999	1.0	First publication of this early access specification
08/23/1999	1.1	Edited text, changed marking, added $\overline{CF}$ and parallel load
09/01/1999	1.2	Corrected JTAG order, Security and Endurance data.
09/16/1999	1.3	Corrected SelectMAP diagram, control inputs, reset polarity. Added JTAG and $\overline{CF}$ description, 256 Kbit and 128 Kbit devices.
01/20/2000	2.0	Added Q44 Package, changed XC18xx to XC18Vxx
02/18/2000	2.1	Updated JTAG configuration, AC and DC characteristics
04/04/2000	2.2	Removed stand alone resistor on INIT pin in Figure 5. Added Virtex-E and EM parts to FPGA table.
06/29/2000	2.3	Removed XC18V128 and updated format. Added AC characteristics for XC18V01, XC18V512, and XC18V256 densities.
11/13/2000	2.4	Features: changed 264 MHz to 264 Mb/s at 33 MHz; AC Spec.: T_{SCE} units to ns, T_{HCE} CE High time units to µs. Removed Standby mode statement: “The lower power standby modes available on some XC18V00 devices are set by the user in the programming software”. Changed 10,000 cycles endurance to 20,000 cycles.
01/15/2001	2.5	Updated Figures 5 and 6, added 4.7 resistors. Identification registers: changes ISP PROM product ID from 06h to 26h.
04/04/2001	2.6	Updated Figure 8, Virtex SelectMAP mode; added XC2V products to Compatible PROM table; changed Endurance from 10,000 cycles, 10 years to 20,000, 20 years;
04/30/2001	2.7	Updated Figure 8: removed Virtex-E in Note 2, fixed SelectMAP mode connections. Under "AC Characteristics Over Operating Conditions for XC18V04 and XC18V02", changed T_{SCE} from 25 ms to 25 ns.
06/11/2001	2.8	"AC Characteristics Over Operating Conditions for XC18V01 and XC18V512". Changed Min values for T_{SCE} from 20 ms to 20 ns and for T_{HCE} from 2 ms to 2 µs.
09/28/2001	2.9	Changed the Boundary-Scan order for the CEO pin in Table 1, updated the configuration bits values in the table under "Xilinx FPGAs and Compatible PROMs", and added information to the "Recommended Operating Conditions" table.
11/12/2001	3.0	Updated for Spartan-IIE FPGA family.
12/06/2001	3.1	Changed Figure 5(c).
02/27/2002	3.2	Updated Table 2 and Figure 8 for the Virtex-II Pro family of devices.
03/15/2002	3.3	Updated Xilinx software and modified Figure 8 and Figure 5.
03/27/2002	3.4	Made changes to pages 1-3, 5, 7-11, 13, 14, and 18. Added new Figure 9 and Figure 9.
06/14/2002	3.5	Made additions and changes to Table 2.
07/24/2002	3.6	Changed last bullet under Connecting Configuration PROMs, page 9.
09/06/2002	3.7	Multiple minor changes throughout, plus the addition of Pinout Diagrams, page 4 and the deletion of Figure 9.
10/31/2002	3.8	Made minor change on Figure 5 (b) and changed orientation of SO20 diagram on page 5.
11/18/2002	3.9	Added XC2S400E and XC2S600E to Table 2.
04/17/2003	3.10	Changes to "Description", "External Programming", and Table 2.

06/11/2003	4.0	Major revision. • Added alternate **IDCODES** to Table 5. • Discontinued XC18V256 density. • Eliminated industrial ordering combinations. • Extended commercial temperature range. • Added MultiPRO Desktop Tool support. • Changed T_{HOE} and T_{HCE} to 250 ns in the tables on <RD Red>page 17 and <RD Red>page 18. • Made change in capacitance values "DC Characteristics Over Operating Conditions". • Added Note (3) to Table 1. • Other minor edits.
12/15/2003	4.1	Added specification (4.7 kΩ) for recommended pull-up resistor on OE/$\overline{\text{RESET}}$ pin to section Reset and Power-On Reset Activation, page 14. Added paragraph to section Standby Mode, page 14, concerning use of a pull-up resistor and/or buffer on the DONE pin.
04/05/2004	5.0	Major revision. • Figure 2: Revised configuration bitstream lengths for most Virtex-II FPGAs. • Replaced previous schematics in Figures 5, 6, 7(a), 7(b), and 7(c) with new Figure 5, Figure 6, Figure 7, and Figure 8. • Replaced previous Figure 8 with new Figure 9. • Replaced previous power-on text section with new Reset and Power-On Reset Activation, page 14. • Added specification table Supply Voltage Requirements for Power-On Reset and Power-Down, page 15. • Added Footnote (5) to: ♦ Specification table AC Characteristics Over Operating Conditions When Cascading for XC18V04 and XC18V02, page 19. ♦ Specification table AC Characteristics Over Operating Conditions When Cascading for XC18V01 and XC18V512, page 20. • Numerous copyedits and wording changes/clarifications throughout.
07/20/2004	5.0.1	Table 2: Removed reference to XC2VP125 FPGA.
03/06/2006	5.1	• Added Pb-free packages to Features, page 1, Pinout Diagrams, page 4,"Ordering Information", Valid Ordering Combinations, page 21and Marking Information, page 22. • Removed maximum soldering temperature (T_{SOL}) from Absolute Maximum Ratings(1,2), page 15. Refer to Xilinx Device Package User Guide for package soldering guidelines. • Added information to Table 5 regarding variable JTAG IDCODE revision field.
01/11/2008	5.2	• Updated document template. • Updated URLs. • Tied RDWR_B and CS_B to GND to ensure valid logic-level Low in FPGA SelectMAP mode in Figure 6, page 11 and Figure 8, page 13. • Updated "Marking Information," page 22 for 20-pin packaging.
08/05/2015	6.0	This product is obsolete/discontinued per XCN15008. Updated Notice of Disclaimer.

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