# 74LV08 Quad 2-input AND gate Rev. 4 — 8 December 2015

Product data sheet

### 1. **General description**

The 74LV08 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC08 and 74HCT08.

The 74LV08 provides a quad 2-input AND function.

### **Features and benefits** 2.

- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between V<sub>CC</sub> = 2.7 V and V<sub>CC</sub> = 3.6 V
- Typical output ground bounce < 0.8 V at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C
- Typical HIGH-level output voltage (V<sub>OH</sub>) undershoot: > 2 V at V<sub>CC</sub> = 3.3 V and  $T_{amb} = 25 \, ^{\circ}C$
- ESD protection:
  - ♦ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

# **Ordering information**

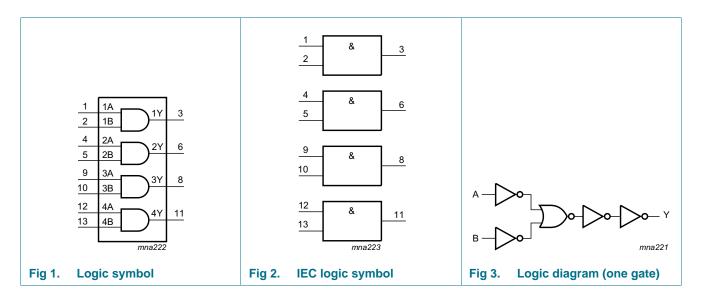
Table 1. **Ordering information** 

Type number	Package											
	Temperature range	Name	Description	Version								
74LV08D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1								
74LV08DB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1								
74LV08PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1								



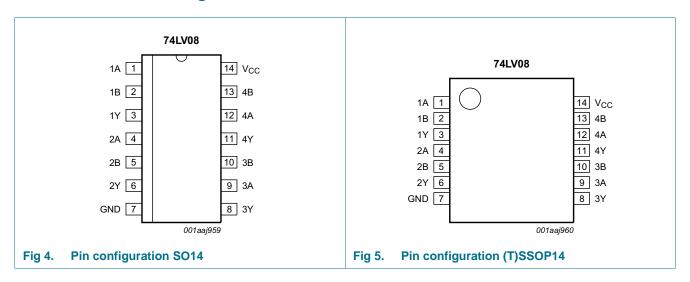
**Quad 2-input AND gate** 

# 4. Functional diagram



# 5. Pinning information

## 5.1 Pinning



**Quad 2-input AND gate** 

# 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A	1, 4, 9, 12	data input
1B, 2B, 3B, 4B	2, 5, 10, 13	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

# 6. Functional description

Table 3. Function selection[1]

Input							
nA	nB	nY					
L	X	L					
X	L	L					
Н	Н	Н					

<sup>[1]</sup> H = HIGH voltage level; L = LOW voltage level; X = don't care

# 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>CC</sub>	supply voltage			-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{CC} + 0.5 \text{ V}$	<u>[1]</u>	-	±20	mA
I <sub>OK</sub>	output clamping current	$V_{O} < -0.5 \text{ V or } V_{O} > V_{CC} + 0.5 \text{ V}$	<u>[1]</u>	-	±50	mA
Io	output current	$V_{O} = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$		-	±25	mA
I <sub>CC</sub>	supply current			-	50	mA
I <sub>GND</sub>	ground current			-50	-	mA
T <sub>stg</sub>	storage temperature			-65	+150	°C
P <sub>tot</sub>	total power dissipation	$T_{amb} = -40  ^{\circ}\text{C} \text{ to } +125  ^{\circ}\text{C}$	[2]			
		SO14, SSOP14, TSSOP14		-	500	mW

<sup>[1]</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>[2]</sup> For SO14 packages: above 70 °C the value of  $P_{tot}$  derates linearly with 8 mW/K. For (T)SSOP14 packages: above 60 °C the value of  $P_{tot}$  derates linearly with 5.5 mW/K.

**Quad 2-input AND gate** 

# 8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>CC</sub>	supply voltage[1]		1.0	3.3	5.5	V
VI	input voltage		0	-	V <sub>CC</sub>	V
Vo	output voltage		0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 1.0 V to 2.0 V	-	-	500	ns/V
		$V_{CC} = 2.0 \text{ V to } 2.7 \text{ V}$	-	-	200	ns/V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	-	-	100	ns/V
		$V_{CC} = 3.6 \text{ V to } 5.5 \text{ V}$	-	-	50	ns/V

<sup>[1]</sup> The static characteristics are guaranteed from  $V_{CC}$  = 1.2 V to  $V_{CC}$  = 5.5 V, but LV devices are guaranteed to function down to  $V_{CC}$  = 1.0 V (with input levels GND or  $V_{CC}$ ).

# 9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

V <sub>IH</sub> II	Parameter	Conditions	-40	°C to +8	5 °C	-40 °C to	+125 °C	Unit
			Min	Typ[1]	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input	V <sub>CC</sub> = 1.2 V	0.9	-	-	0.9	-	V
	voltage	V <sub>CC</sub> = 2.0 V	1.4	-	-	1.4	-	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2.0	-	-	2.0	-	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7V <sub>CC</sub>	-	-	0.7V <sub>CC</sub>	-	V
V <sub>IL</sub> LOW-level in voltage	LOW-level input	V <sub>CC</sub> = 1.2 V	-	-	0.3	-	0.3	V
	voltage	V <sub>CC</sub> = 2.0 V	-	-	0.6	-	0.6	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.3V <sub>CC</sub>	-	0.3V <sub>CC</sub>	V
V <sub>OH</sub>	HIGH-level output	$V_I = V_{IH}$ or $V_{IL}$						
	voltage	$I_{O} = -100 \mu A; V_{CC} = 1.2 V$	-	1.2	-	-	-	V
		$I_{O} = -100 \mu A; V_{CC} = 2.0 V$	1.8	2.0	-	1.8	Max	V
	LOW-level input voltage  HIGH-level output	$I_O = -100 \mu A; V_{CC} = 2.7 V$	2.5	2.7	-	2.5	-	V
		$I_O = -100 \mu A; V_{CC} = 3.0 \text{ V}$	2.8	3.0	-	2.8	-	V
		$I_O = -100 \mu A$ ; $V_{CC} = 4.5 V$	4.3	4.5	-	4.3	-	V
		$I_{O} = -6 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.4	2.82	-	2.2	-	V
V <sub>OH</sub> H		$I_{O} = -12 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.6	4.2	-	3.5	-	V

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**Table 6. Static characteristics** ...continued Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40	°C to +8	5 °C	–40 °C to	+125 °C	Unit
			Min	Typ[1]	Max	Min	Max	
V <sub>OL</sub>	LOW-level output	$V_I = V_{IH}$ or $V_{IL}$						
	voltage	$I_O = 100 \mu A; V_{CC} = 1.2 V$	-	0	-	-	-	V
		$I_O = 100 \mu A; V_{CC} = 2.0 V$	-	0	0.2	-	0.2	V
		$I_O = 100 \mu A; V_{CC} = 2.7 V$	-	0	0.2	-	0.2	V
		$I_O = 100 \mu A; V_{CC} = 3.0 \text{ V}$	-	0	0.2	-	0.2	V
		$I_O = 100 \mu A; V_{CC} = 4.5 V$	-	0	0.2	-	0.2	V
		$I_O = 6 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	0.25	0.40	-	0.50	V
		$I_O = 12 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	0.35	0.55	-	0.65	V
I <sub>I</sub>	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	1.0	-	1.0	μΑ
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	20.0	-	40	μА
Δl <sub>CC</sub>	additional supply current	per input; $V_I = V_{CC} - 0.6 \text{ V}$ ; $V_{CC} = 2.7 \text{ V}$ to 3.6 V	-	-	500	-	850	μА
Cı	input capacitance		-	3.5	-	-	-	pF

<sup>[1]</sup> Typical values are measured at  $T_{amb}$  = 25 °C.

# 10. Dynamic characteristics

**Table 7. Dynamic characteristics** GND = 0 V; For test circuit see Figure 7.

Symbol	Parameter	Conditions		<b>-40</b>	°C to +85	S °C	–40 °C t	o +125 °C	Unit
				Min	Typ[1]	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nA, nB to nY; see Figure 6	[2]						
		V <sub>CC</sub> = 1.2 V		-	45	-	-	-	ns
		V <sub>CC</sub> = 2.0 V		-	15	26	-	33	ns
		V <sub>CC</sub> = 2.7 V		-	11	17	-	21	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V; } C_L = 15 \text{ pF}$	[3]	-	7	-	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	[3]	-	9.0	15	-	19	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V		-	-	11	-	14	ns
C <sub>PD</sub>	power dissipation capacitance	$C_L$ = 50 pF; $f_i$ = 1 MHz; $V_I$ = GND to $V_{CC}$	[4]	-	10	-	-	-	pF

- [1] All typical values are measured at  $T_{amb}$  = 25 °C.
- [2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .
- [3] Typical values are measured at nominal supply voltage ( $V_{CC} = 3.3 \text{ V}$ ).
- [4]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

 $P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}{}^2 \times f_o) \text{ where:}$ 

 $f_i$  = input frequency in MHz,  $f_o$  = output frequency in MHz

C<sub>L</sub> = output load capacitance in pF

 $V_{CC}$  = supply voltage in Volts

N = number of inputs switching

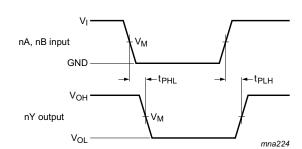
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

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## 11. Waveforms



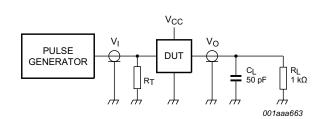
Measurement points are given in Table 8.

V<sub>OL</sub> and V<sub>OH</sub> are typical voltage output levels that occur with the output load.

Fig 6. The input (nA, nB) to output (nY) propagation delays

Table 8. Measurement points

Supply voltage	Input	Output
V <sub>CC</sub>	V <sub>M</sub>	V <sub>M</sub>
< 2.7 V	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>
2.7 V to 3.6 V	1.5 V	1.5 V
≥ 4.5 V	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>



Test data is given in Table 9.

Definitions test circuit:

 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

 $R_L$  = Load resistance.

 $C_L$  = Load capacitance including jig and probe capacitance.

Fig 7. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input				
Vcc	V <sub>I</sub>	$t_r, t_f$			
< 2.7 V	Vcc	≤ 2.5 ns			
2.7 V to 3.6 V	2.7 V	≤ 2.5 ns			
≥ 4.5 V	Vcc	≤ 2.5 ns			

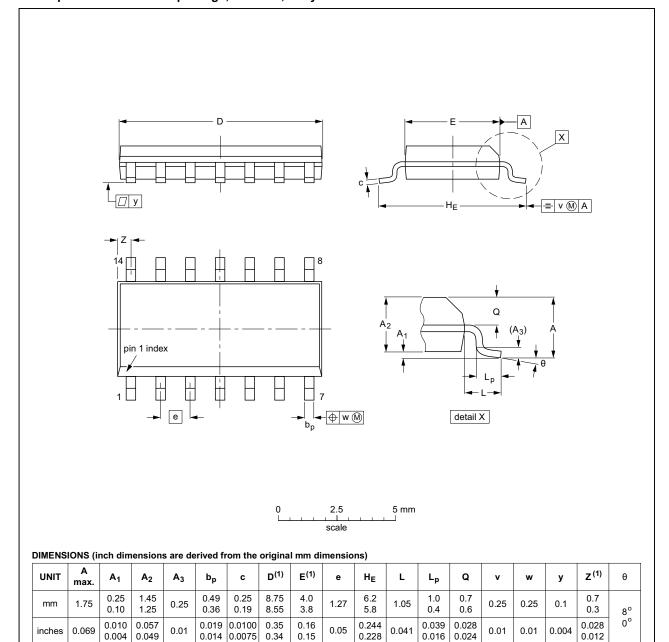
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# 12. Package outline

### SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



### Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE	
SOT108-1	076E06	MS-012			<del>99-12-27</del> 03-02-19	

Fig 8. Package outline SOT108-1 (SO14)

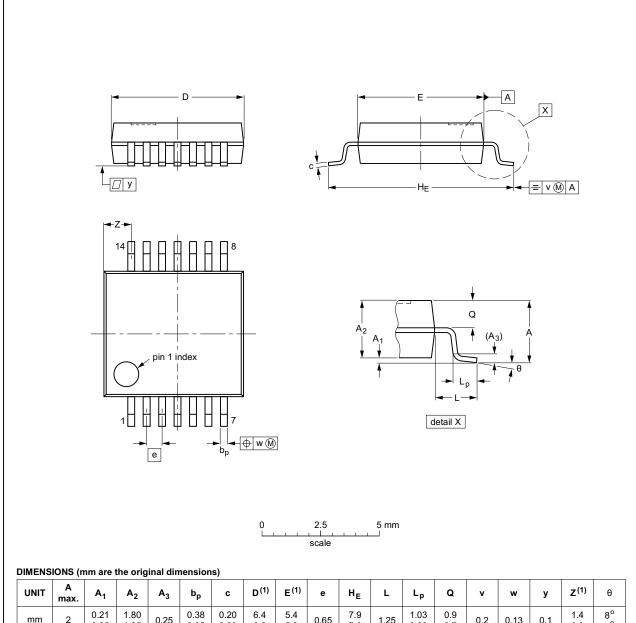
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SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	<b>A</b> <sub>3</sub>	b <sub>p</sub>	C	D <sup>(1)</sup>	E <sup>(1)</sup>	е	HE	L	Lp	Q	v	w	у	Z <sup>(1)</sup>	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

### Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

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MO-150				<del>99-12-27</del> 03-02-19	
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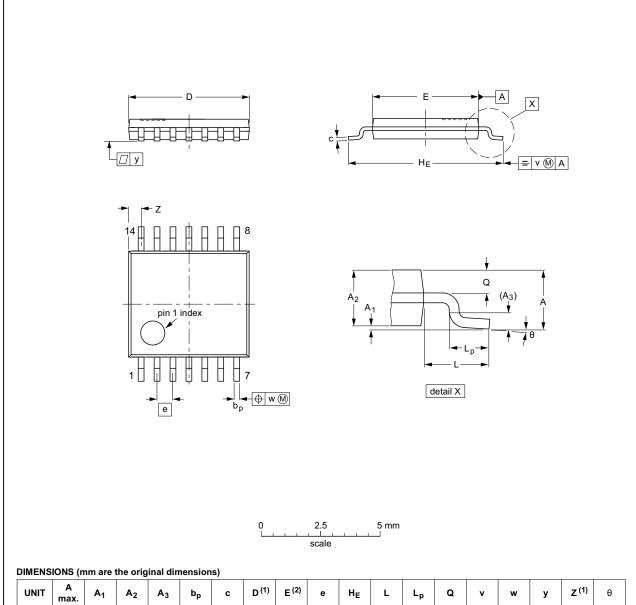
Package outline SOT337-1 (SSOP14) Fig 9.

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	<b>A</b> <sub>3</sub>	bp	С	D <sup>(1)</sup>	E (2)	е	HE	L	Lp	Q	٧	w	у	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

### Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

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			-	
MO-153			∃⊕	<del>99-12-27</del> 03-02-18
	MO-153	MO-153	MO-153	MO-153

Fig 10. Package outline SOT402-1 (TSSOP14)

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# 13. Abbreviations

### Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

# 14. Revision history

### Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes					
74LV08 v.4	20151208	20151208 Product data sheet - 74LV08 v.3							
Modifications:	Type numbe	r 74LV08N (SOT27-1) remove	d.						
74LV08 v.3	20090406 Product data sheet - 74LV08 v.2								
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> </ul>								
	<ul> <li>Legal texts have been adapted to the new company name when appropriate.</li> </ul>								
74LV08 v.2	19980420	Product specification	-	74LV08 v.1					
74LV08 v.1	19970203	Product specification	-	-					

**Quad 2-input AND gate** 

# 15. Legal information

### 15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition						
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.						
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- [2] The term 'short data sheet' is explained in section "Definitions"
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# **Quad 2-input AND gate**

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