

# **BUK763R4-30B**

# N-channel TrenchMOS standard level FET Rev. 2 — 21 April 2011

**Product data sheet** 

#### 1. **Product profile**

## 1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

## 1.2 Features and benefits

- AEC Q101 compliant
- Suitable for standard level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

## 1.3 Applications

- 12 V loads
- Automotive systems

- General purpose power switching
- Motors, lamps and solenoids

## 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \ge 25 \text{ °C}; T_j \le 175 \text{ °C}$		-	-	30	V
I <sub>D</sub>	drain current	$V_{GS} = 10 \text{ V}; T_{mb} = 25 \text{ °C};$ see <u>Figure 1</u> ; see <u>Figure 4</u>	<u>[1]</u>	-	-	75	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>		-	-	255	W
Static cha	racteristics						
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A};$ $T_j = 25 \text{ °C};$ see <u>Figure 12</u> ; see <u>Figure 13</u>		-	2.9	3.4	mΩ
Avalanch	e ruggedness						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$I_D$ = 75 A; $V_{sup} \le 30$ V; $R_{GS}$ = 50 $\Omega$ ; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped		-	-	1.3	J

<sup>[1]</sup> Continuous current is limited by package.



# 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain	mb	D
3	S	source		
mb	D	mounting base; connected to drain	1 3	mbb076 S
			SOT404 (D2PAK)	

# 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK763R4-30B	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C		-	30	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$		-	30	V
V <sub>GS</sub>	gate-source voltage			-20	20	V
I <sub>D</sub>	drain current	$T_{mb}$ = 25 °C; $V_{GS}$ = 10 V; see <u>Figure 1</u> ; see <u>Figure 4</u>	<u>[1]</u>	-	75	Α
		$T_{mb} = 100  ^{\circ}\text{C};  V_{GS} = 10  \text{V};  \text{see}  \frac{\text{Figure 1}}{}$	<u>[1]</u>	-	75	Α
		$T_{mb}$ = 25 °C; $V_{GS}$ = 10 V; see <u>Figure 1</u> ; see <u>Figure 4</u>	[2][3]	-	198	Α
I <sub>DM</sub>	peak drain current	$T_{mb}$ = 25 °C; pulsed; $t_p \le 10 \mu s$ ; see Figure 4		-	794	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>		-	255	W
T <sub>stg</sub>	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
Source-drain	diode					
Is	source current	T <sub>mb</sub> = 25 °C	[2][3]	-	198	Α
			<u>[1]</u>	-	75	Α
I <sub>SM</sub>	peak source current	pulsed; $t_p \le 10 \ \mu s$ ; $T_{mb} = 25 \ ^{\circ}C$		-	794	Α
Avalanche rug	gedness					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$I_D$ = 75 A; $V_{sup}$ ≤ 30 V; $R_{GS}$ = 50 $\Omega$ ; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped		-	1.3	J
E <sub>DS(AL)R</sub>	repetitive drain-source avalanche energy	see Figure 3	[4][5][6][ <u>7]</u>	-	-	J

<sup>[1]</sup> Continuous current is limited by package.

<sup>[2]</sup> Current is limited by power dissipation chip rating.

<sup>[3]</sup> Refer to document 9397 750 12572 for further information.

<sup>[4]</sup> Maximum value not quoted. Repetitive rating defined in avalanche rating figure.

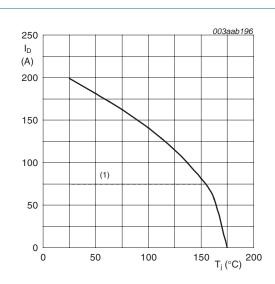
<sup>[5]</sup> Single-shot avalanche rating limited by maximum junction temperature of 175 °C.

<sup>[6]</sup> Repetitive avalanche rating limited by an average junction temperature of 170 °C.

<sup>[7]</sup> Refer to application note AN10273 for further information.

Fig 1.

## N-channel TrenchMOS standard level FET

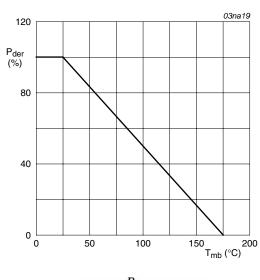


 $V_{\rm GS} \geq$  5 V

Continuous drain current as a function of

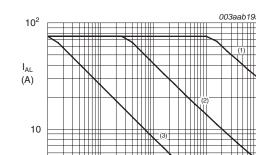
mounting base temperature

(1) Capped at 75 A due to package.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Normalized total power dissipation as a Fig 2. function of mounting base temperature

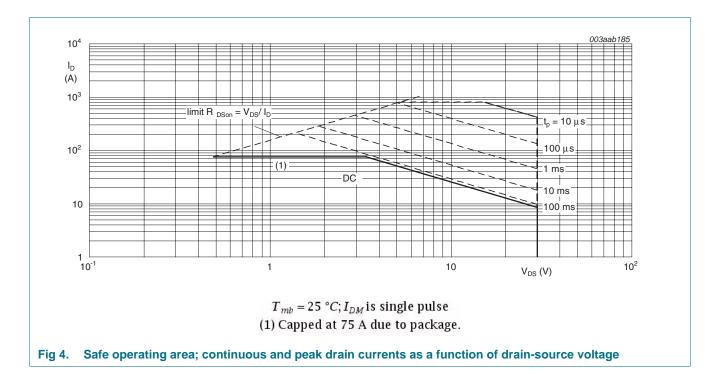


Single shot and repetitive avalanche rating; avalanche current as a function of avalanche time Fig 3.

10<sup>-1</sup>

t<sub>AL</sub> (ms) 10

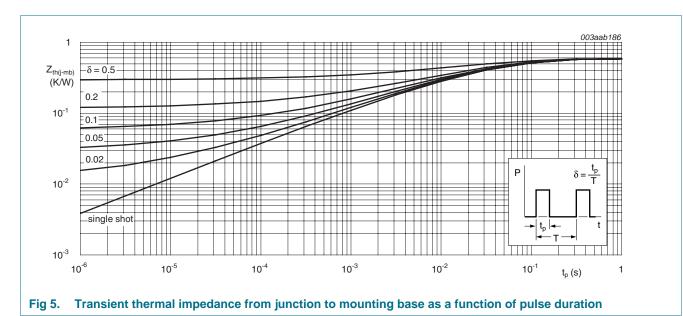
10<sup>-2</sup>



## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	-	0.59	K/W
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint; vertical in still air	-	50	-	K/W



BUK763R4-30B All information provided in this document is subject to leg

## 6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	aracteristics					
V <sub>(BR)DSS</sub>	drain-source	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	30	-	-	V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 ^{\circ}C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ °C}$ ; see <u>Figure 10</u> ; see <u>Figure 11</u>	2	3	4	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 1$ mA; $V_{DS} = V_{GS}$ ; $T_j = -55$ °C; see <u>Figure 10</u> ; see <u>Figure 11</u>	-	-	4.4	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$ ; $T_j = 175$ °C; see <u>Figure 10</u> ; see <u>Figure 11</u>	1	-	-	V
DSS	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.05	10	μA
GSS	gate leakage current	V <sub>GS</sub> = 20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 °C;$ see <u>Figure 12</u> ; see <u>Figure 13</u>	-	-	6.5	mΩ
		$V_{GS} = 10 \text{ V}$ ; $I_D = 25 \text{ A}$ ; $T_j = 25 \text{ °C}$ ; see Figure 12; see Figure 13	-	2.9	3.4	mΩ
I <sub>DSS</sub>	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ °C}$	-	-	500	μΑ
Dynamic	characteristics					
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 24 \text{ V}; V_{GS} = 10 \text{ V};$	-	75	-	nC
$Q_{GS}$	gate-source charge	see Figure 14	-	19	-	nC
$Q_{GD}$	gate-drain charge		-	23	-	nC
C <sub>iss</sub>	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$	-	3713	4951	pF
Coss	output capacitance	T <sub>j</sub> = 25 °C; see <u>Figure 15</u>	-	1249	1499	pF
C <sub>rss</sub>	reverse transfer capacitance		-	460	630	pF
d(on)	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \Omega; V_{GS} = 10 \text{ V};$	-	32	-	ns
r	rise time	$R_{G(ext)} = 10 \Omega$	-	64	-	ns
d(off)	turn-off delay time		-	89	-	ns
f	fall time		-	71	-	ns
-D	internal drain inductance	from contact screw on mounting base to centre of die	-	3.5	-	nΗ
		from upper edge of drain mounting base to centre of die	-	2.5	-	nΗ
		from drain lead 6 mm from package to centre of die	-	4.5	-	nΗ
-S	internal source inductance	from source lead to source bonding pad	-	7.5	-	nΗ
Source-d	rain diode					
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C};$ see <u>Figure 16</u>	-	0.85	1.2	V
rr	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$	-	70	-	ns
**		$V_{DS} = 30 \text{ V}$				

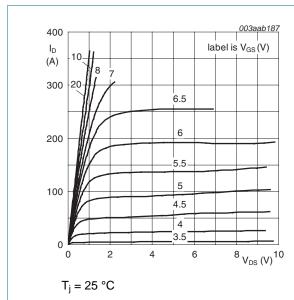


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values

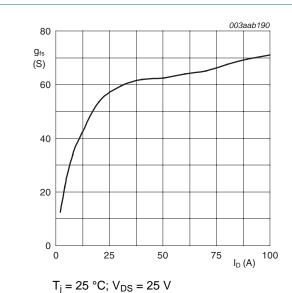


Fig 8. Forward transconductance as a function of drain current; typical values

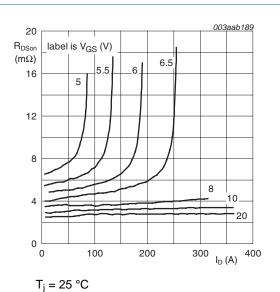


Fig 7. Drain-source on-state resistance as a function of drain current; typical values

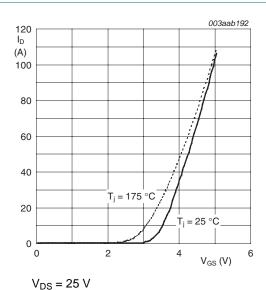
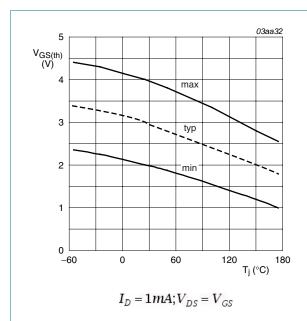
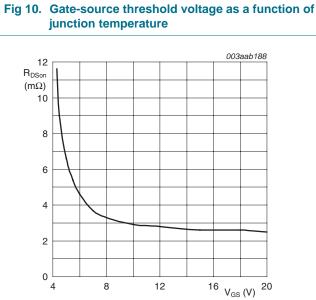


Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

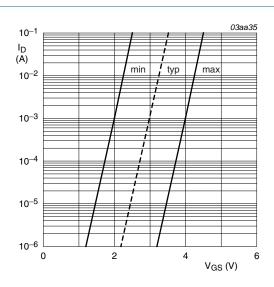


junction temperature



 $T_j = 25 \, ^{\circ}C; I_D = 10 \, A$ 

Fig 12. Drain-source on-state resistance as a function of gate-source voltage; typical values



 $T_j = 25 \,^{\circ}C; V_{DS} = 5V$ 

Fig 11. Sub-threshold drain current as a function of gate-source voltage

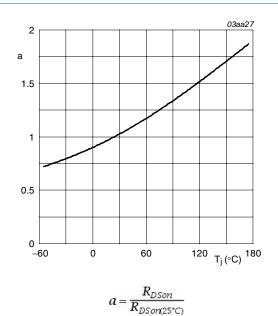


Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

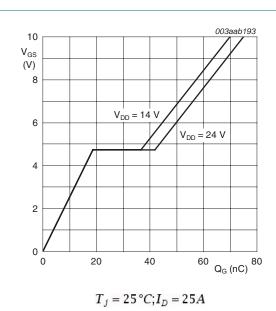
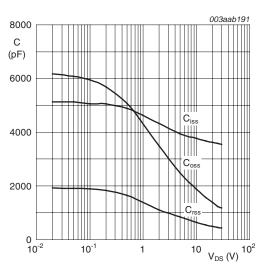
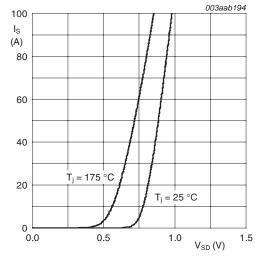


Fig 14. Gate-source voltage as a function of gate charge; typical values



 $V_{GS} = 0V; f = 1MHz$ 

Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



 $V_{GS} = 0 V$ 

Fig 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

## 7. Package outline

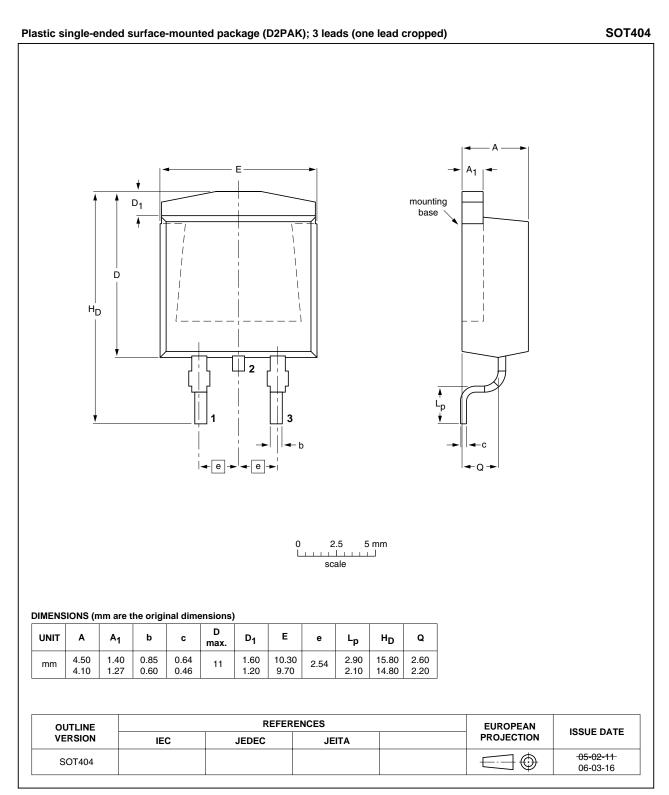


Fig 17. Package outline SOT404 (D2PAK)

## 8. Revision history

## Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK763R4-30B v.2	20110421	Product data sheet	-	BUK75_763R4-30B_1
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the new identity guide of NXP Semiconductors.</li> </ul>			
	<ul> <li>Legal texts have be</li> </ul>	een adapted to the new c	ompany name where app	oropriate.
	<ul> <li>Type number BUK</li> </ul>	763R4-30B separated from	m data sheet BUK75_76	3R4-30B_1.
BUK75_763R4-30B_1	20060105	Product specification	-	-

## 9. Legal information

#### 9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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## **Nexperia**

N-channel TrenchMOS standard level FET

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