

# HEF4014B

## 8-bit static shift register

Rev. 9 — 21 March 2016

Product data sheet

### 1. General description

The HEF4014B is a fully synchronous edge-triggered 8-bit static shift register with eight synchronous parallel inputs (D0 to D7), a synchronous serial data input (DS), a synchronous parallel enable input (PE), a LOW-to-HIGH edge-triggered clock input (CP) and buffered parallel outputs from the last three stages (Q5 to Q7).

Operation is synchronous and the device is edge-triggered on the LOW-to-HIGH transition of CP. Each register stage is of a D-type master-slave flip-flop type. When PE is HIGH, data is loaded into the register from D0 to D7 on the LOW-to-HIGH transition of CP. When PE is LOW, data is shifted to the first position from DS, and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of CP. The clock input's Schmitt trigger action makes it highly tolerant of slower clock rise and fall times.

It operates over a recommended  $V_{DD}$  power supply range of 3 V to 15 V referenced to  $V_{SS}$  (usually ground). Unused inputs must be connected to  $V_{DD}$ ,  $V_{SS}$ , or another input.

### 2. Features and benefits

- Tolerant of slow clock rise and fall times
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

### 3. Applications

- Parallel-to-serial converter
- Serial data queueing
- General purpose register

### 4. Ordering information

Table 1. Ordering information

All types operate from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$

Type number	Package		Version
	Name	Description	
HEF4014BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

5. Functional diagram

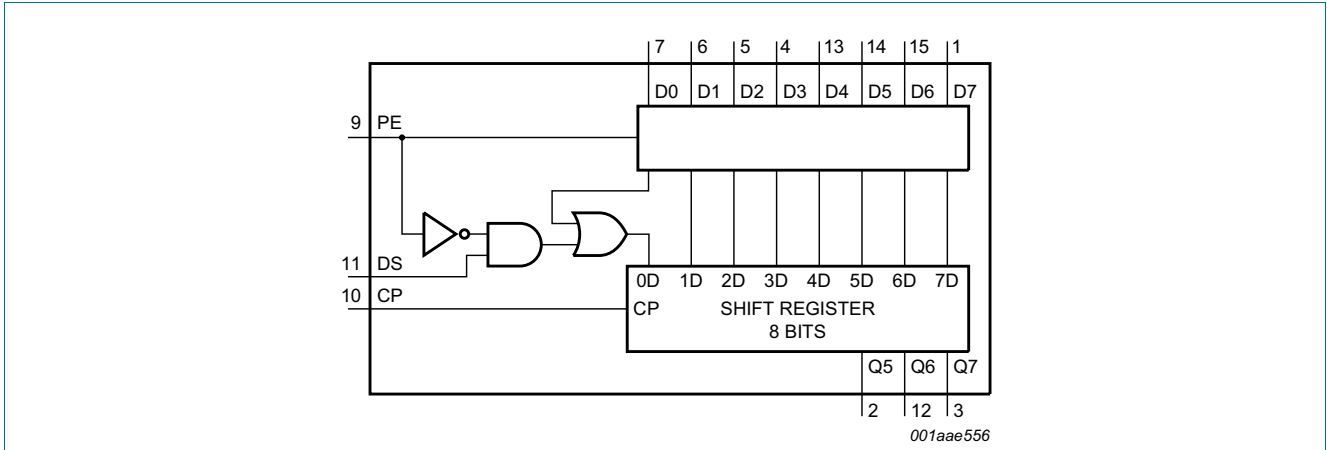


Fig 1. Functional diagram

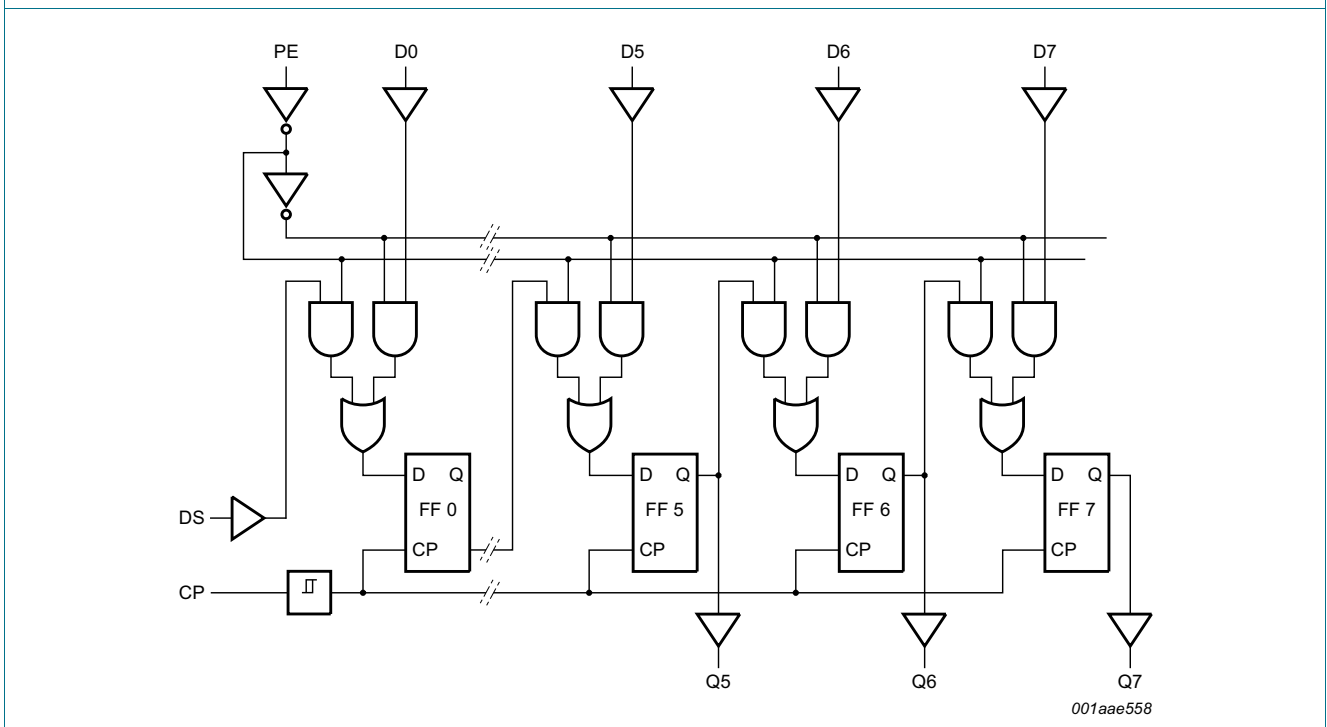
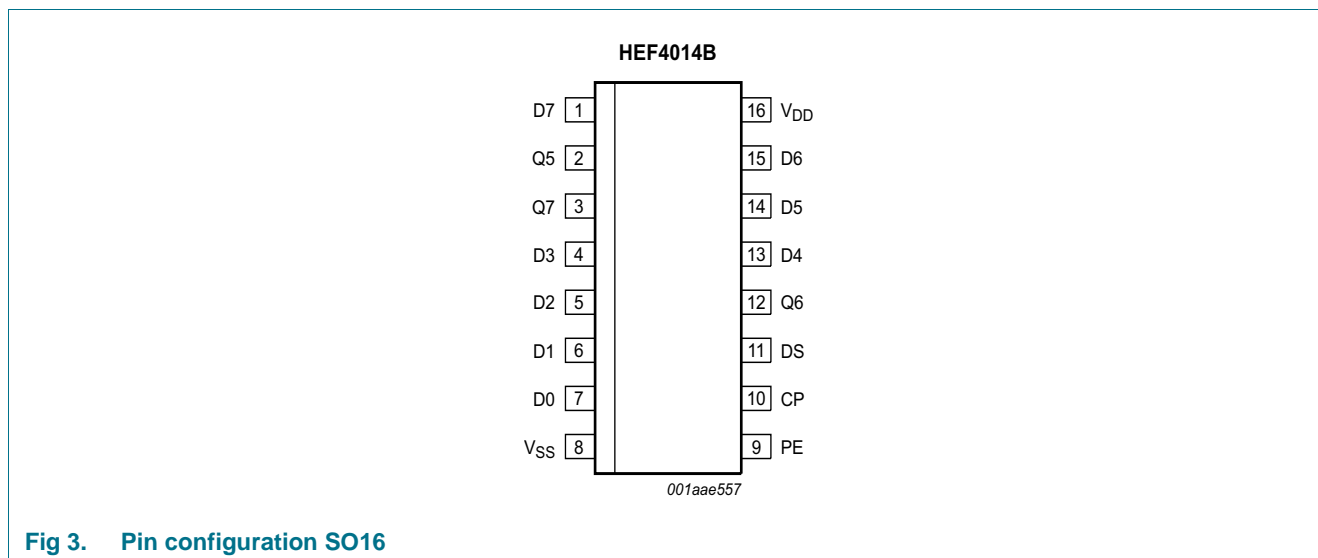


Fig 2. Logic diagram

## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

**Table 2. Pin description**

Symbol	Pin	Description
Q5 to Q7	2, 12, 3	output
D0 to D7	7, 6, 5, 4, 13, 14, 15, 1	parallel data input
V <sub>SS</sub>	8	ground supply voltage
PE	9	parallel enable input
CP	10	clock input (LOW-to-HIGH edge-triggered)
DS	11	serial data input
V <sub>DD</sub>	16	supply voltage

## 7. Functional description

Table 3. Function table<sup>[1]</sup>

Number of clock transitions	Inputs			Outputs		
	CP	DS	PE	Q5	Q6	Q7
<b>Serial operation</b>						
1	↑	1D	L	X	X	X
2	↑	2D	L	X	X	X
3	↑	3D	L	X	X	X
6	↑	X	L	1D	X	X
7	↑	X	L	2D	1D	X
8	↑	X	L	3D	2D	1D
	↓	X	X	no change	no change	no change
<b>Parallel operation</b>						
1	↑	X	H	D5	D6	D7
	↓	X	X	no change	no change	no change

- [1] H = HIGH voltage level; L = LOW voltage level; X = don't care; nD = HIGH or LOW;  
 ↑ = LOW-to-HIGH clock transition; ↓ = HIGH-to-LOW clock transition;

## 8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+18	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{DD} + 0.5\text{ V}$	-	±10	mA
$V_I$	input voltage		-0.5	$V_{DD} + 0.5$	V
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{DD} + 0.5\text{ V}$	-	±10	mA
$I_{IO}$	input/output current		-	±10	mA
$I_{DD}$	supply current		-	50	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_{amb}$	ambient temperature		-40	+85	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+85\text{ °C}$			
		SO16 package <sup>[1]</sup>	-	500	mW
P	power dissipation	per output	-	100	mW

- [1] For SO16 package:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.

## 9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD}$	supply voltage		3	-	15	V
$V_I$	input voltage		0	-	$V_{DD}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	-	0.08	$\mu\text{s/V}$

## 10. Static characteristics

Table 6. Static characteristics

$V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ °C}$		$T_{amb} = +25\text{ °C}$		$T_{amb} = +85\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$ I_O  < 1\ \mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
$V_{IL}$	LOW-level input voltage	$ I_O  < 1\ \mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
$V_{OH}$	HIGH-level output voltage	$ I_O  < 1\ \mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
$V_{OL}$	LOW-level output voltage	$ I_O  < 1\ \mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
$I_{OH}$	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		$V_O = 4.6\text{ V}$	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		$V_O = 9.5\text{ V}$	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		$V_O = 13.5\text{ V}$	15 V	-	-3.6	-	-3.0	-	-2.4	mA
$I_{OL}$	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.52	-	0.44	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.3	-	1.1	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	3.6	-	3.0	-	2.4	-	mA
$I_I$	input leakage current		15 V	-	$\pm 0.3$	-	$\pm 0.3$	-	$\pm 1.0$	$\mu\text{A}$
$I_{DD}$	supply current	$I_O = 0\text{ A}$	5 V	-	20	-	20	-	150	$\mu\text{A}$
			10 V	-	40	-	40	-	300	$\mu\text{A}$
			15 V	-	80	-	80	-	600	$\mu\text{A}$
$C_I$	input capacitance		-	-	-	7.5	-	-	pF	

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $V_{SS} = 0\text{ V}$ .

Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula <sup>[1]</sup>	Min	Typ	Max	Unit
$t_{PHL}$	HIGH to LOW propagation delay	CP to Qn; see <a href="#">Figure 4</a>	5 V	$103\text{ ns} + (0.55\text{ ns/pF})C_L$	-	130	260	ns
			10 V	$44\text{ ns} + (0.23\text{ ns/pF})C_L$	-	55	110	ns
			15 V	$32\text{ ns} + (0.16\text{ ns/pF})C_L$	-	40	80	ns
$t_{PLH}$	LOW to HIGH propagation delay	CP to Qn; see <a href="#">Figure 4</a>	5 V	$88\text{ ns} + (0.55\text{ ns/pF})C_L$	-	115	230	ns
			10 V	$39\text{ ns} + (0.23\text{ ns/pF})C_L$	-	50	100	ns
			15 V	$32\text{ ns} + (0.16\text{ ns/pF})C_L$	-	40	80	ns
$t_t$	transition time	Qn output; see <a href="#">Figure 4</a>	5 V <sup>[2]</sup>	$10\text{ ns} + (1.00\text{ ns/pF})C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF})C_L$	-	20	40	ns
$t_W$	pulse width	CP input; minimum width; see <a href="#">Figure 5</a>	5 V		70	35	-	ns
			10 V		30	15	-	ns
			15 V		24	12	-	ns
$t_{su}$	set-up time	PE → CP; see <a href="#">Figure 5</a>	5 V		40	10	-	ns
			10 V		25	5	-	ns
			15 V		15	0	-	ns
		DS → CP; see <a href="#">Figure 5</a>	5 V		+35	-5	-	ns
			10 V		+25	-5	-	ns
			15 V		25	0	-	ns
		Dn → CP; see <a href="#">Figure 5</a>	5 V		+35	-5	-	ns
			10 V		+25	-5	-	ns
			15 V		25	0	-	ns
$t_h$	hold time	PE → CP; see <a href="#">Figure 5</a>	5 V		+25	-5	-	ns
			10 V		20	0	-	ns
			15 V		15	0	-	ns
		DS → CP; see <a href="#">Figure 5</a>	5 V		30	15	-	ns
			10 V		20	10	-	ns
			15 V		15	7	-	ns
		Dn → CP; see <a href="#">Figure 5</a>	5 V		30	15	-	ns
			10 V		20	10	-	ns
			15 V		15	7	-	ns
$f_{clk(max)}$	maximum clock frequency	see <a href="#">Figure 5</a>	5 V		6	13	-	MHz
			10 V		15	30	-	MHz
			15 V		20	40	-	MHz

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown ( $C_L$  in pF).

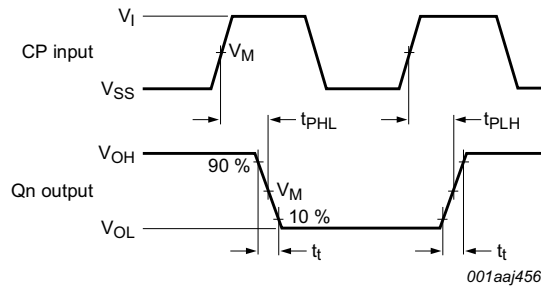
[2]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .

**Table 8. Dynamic power dissipation  $P_D$**

$P_D$  can be calculated from the formulas shown.  $V_{SS} = 0\text{ V}$ ;  $t_r = t_f \leq 20\text{ ns}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ .

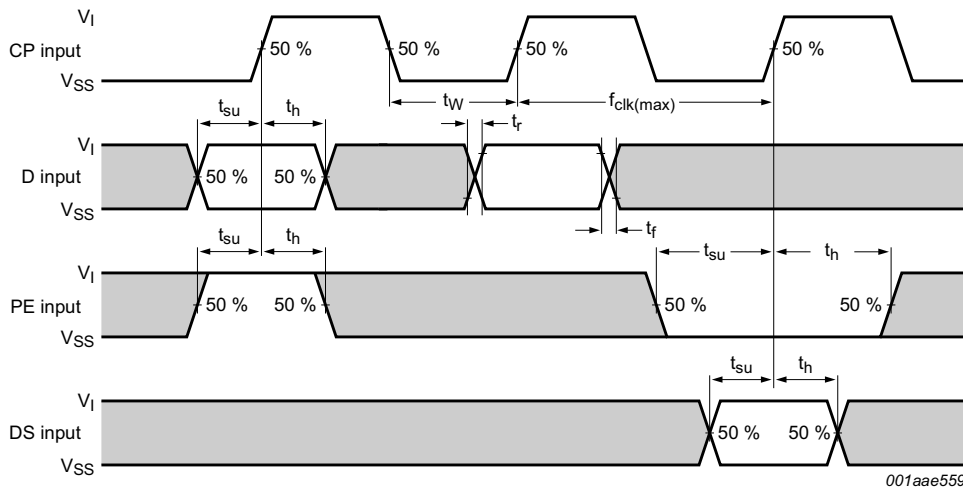
Symbol	Parameter	$V_{DD}$	Typical formula for $P_D$ ( $\mu\text{W}$ )	Where:
$P_D$	dynamic power dissipation	5 V	$P_D = 900 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$f_i$ = input frequency in MHz; $f_o$ = output frequency in MHz; $C_L$ = output load capacitance in pF; $V_{DD}$ = supply voltage in V; $\Sigma(C_L \times f_o)$ = sum of the outputs.
		10 V	$P_D = 4300 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 12000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	

## 12. Waveforms



Measurement points are given in [Table 9](#).

**Fig 4. CP to Qn propagation delays and output transition times**



The shaded areas indicate where change is permitted for predictable output performance.

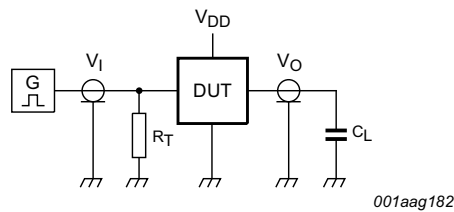
Set-up and hold times are shown as positive values but may be specified as negative values.

Measurement points are given in [Table 9](#).

**Fig 5. Minimum clock pulse width, and set-up and hold times for PE to CP, DS to CP, and D to CP**

Table 9. Measurement points

Supply voltage	Input	Output
$V_{DD}$	$V_M$	$V_M$
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



Test data is given in [Table 10](#);

Definitions for test circuit:

DUT = Device Under Test.

$C_L$  = load capacitance including jig and probe capacitance.

$R_T$  = termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

Fig 6. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input	Load
$V_{DD}$	$V_I$	$C_L$
5 V to 15 V	$V_{SS}$ or $V_{DD}$	50 pF
		$t_r, t_f$
		$\leq 20$ ns



13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



Fig 7. Package outline SOT109-1 (SO16)

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4014B v.9	20160321	Product data sheet	-	HEF4014B v.8
Modifications:	<ul style="list-style-type: none"> <li>Type number HEF4014BP (SOT38-4) removed.</li> </ul>			
HEF4014B v.8	20111121	Product data sheet	-	HEF4014B v.7
Modifications:	<ul style="list-style-type: none"> <li>Legal pages updated.</li> <li>Changes in “General description” and “Features and benefits”.</li> </ul>			
HEF4014B v.7	20110914	Product data sheet	-	HEF4014B v.6
HEF4014B v.6	20091102	Product data sheet	-	HEF4014B v.5
HEF4014B v.5	20090624	Product data sheet	-	HEF4014B v.4
HEF4014B v.4	20090122	Product data sheet	-	HEF4014B_CNV v.3
HEF4014B_CNV v.3	19950101	Product specification	-	HEF4014B_CNV v.2
HEF4014B_CNV v.2	19950101	Product specification	-	-

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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