



# PMDXB950UPE

20 V, dual P-channel Trench MOSFET

30 June 2015

Product data sheet

## 1. General description

Dual P-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1010B-6 (SOT1216) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Trench MOSFET technology
- Leadless ultra small and ultra thin SMD plastic package: 1.1 × 1.0 × 0.37 mm
- Exposed drain pad for excellent thermal conduction
- ElectroStatic Discharge (ESD) protection > 1 kV HBM
- Drain-source on-state resistance  $R_{DSon} = 1.02 \Omega$

## 3. Applications

- Relay driver
- High-speed line driver
- High-side load switch
- Switching circuits

## 4. Quick reference data

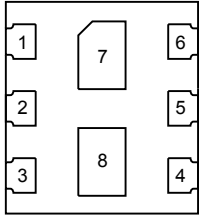
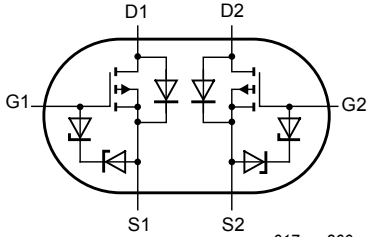
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
$V_{DS}$	drain-source voltage	$T_j = 25 \text{ }^\circ\text{C}$	-	-	-20	V
$V_{GS}$	gate-source voltage		-8	-	8	V
$I_D$	drain current	$V_{GS} = -4.5 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$	[1]	-	-500	mA
<b>Static characteristics (per transistor)</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}; I_D = -500 \text{ mA}; T_j = 25 \text{ }^\circ\text{C}$	-	1.02	1.4	$\Omega$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 <p>Transparent top view <b>DFN1010B-6 (SOT1216)</b></p>	 <p>017aaa260</p>
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		
7	D1	drain TR1		
8	D2	drain TR2		

## 6. Ordering information

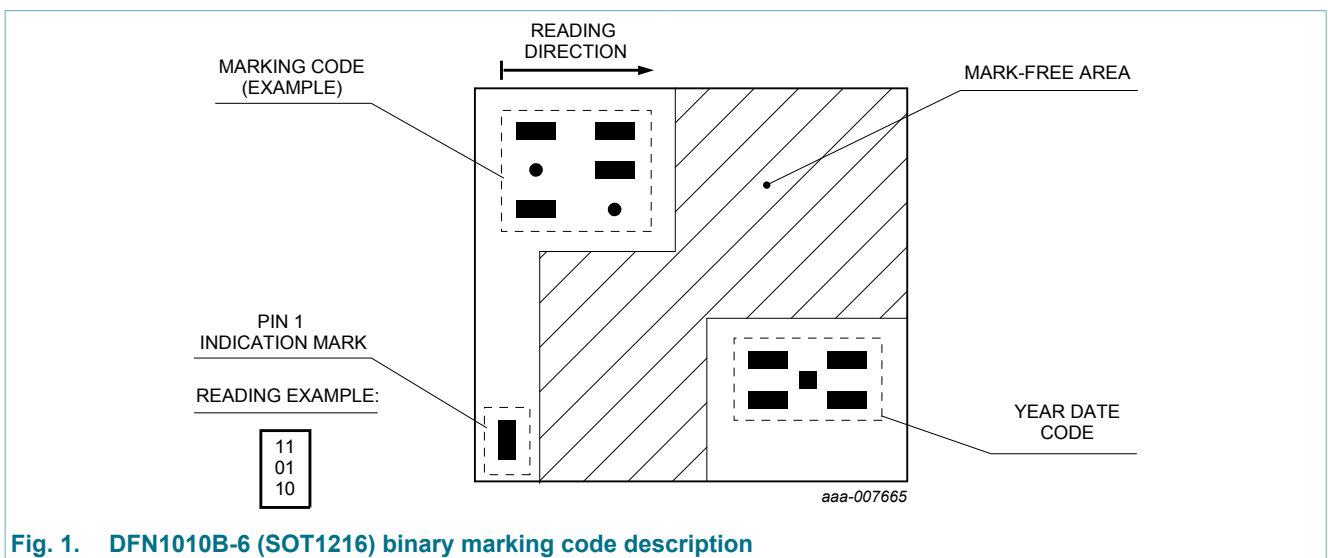
Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMDXB950UPE	DFN1010B-6	DFN1010B-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1216

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PMDXB950UPE	10 10 00



## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
<b>Per transistor</b>						
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$		-	-20	V
$V_{GS}$	gate-source voltage			-8	8	V
$I_D$	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-500	mA
		$V_{GS} = -4.5\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	-300	mA
$I_{DM}$	peak drain current	$T_{amb} = 25\text{ °C}; \text{single pulse}; t_p \leq 10\text{ }\mu\text{s}$		-	-2	A
$P_{tot}$	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	265	mW
			[1]	-	380	mW
		$T_{sp} = 25\text{ °C}$		-	4025	mW
<b>Source-drain diode</b>						
$I_S$	source current	$T_{amb} = 25\text{ °C}$	[1]	-	-350	mA
<b>Per device</b>						
$T_j$	junction temperature			-55	150	°C
$T_{amb}$	ambient temperature			-55	150	°C
$T_{stg}$	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain  $1\text{ cm}^2$ .

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

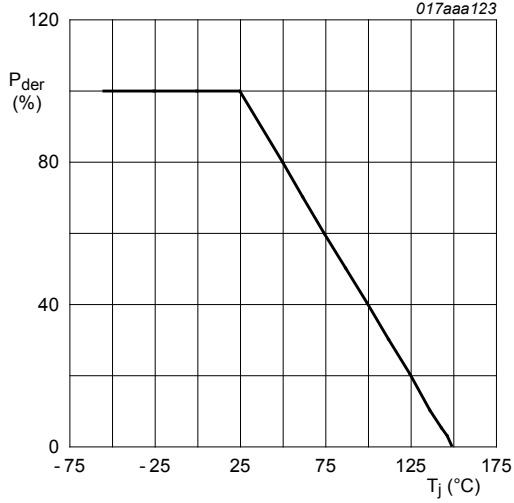


Fig. 2. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100 \%$$

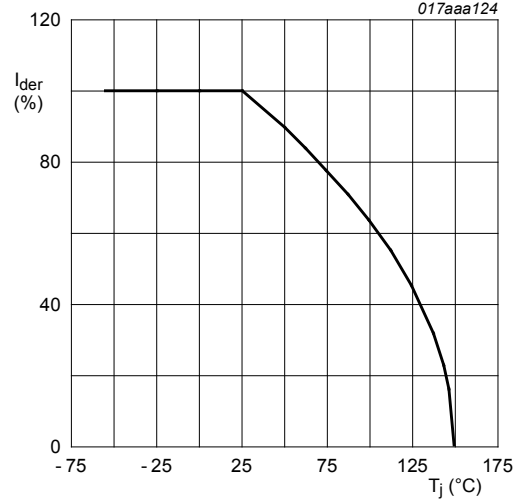
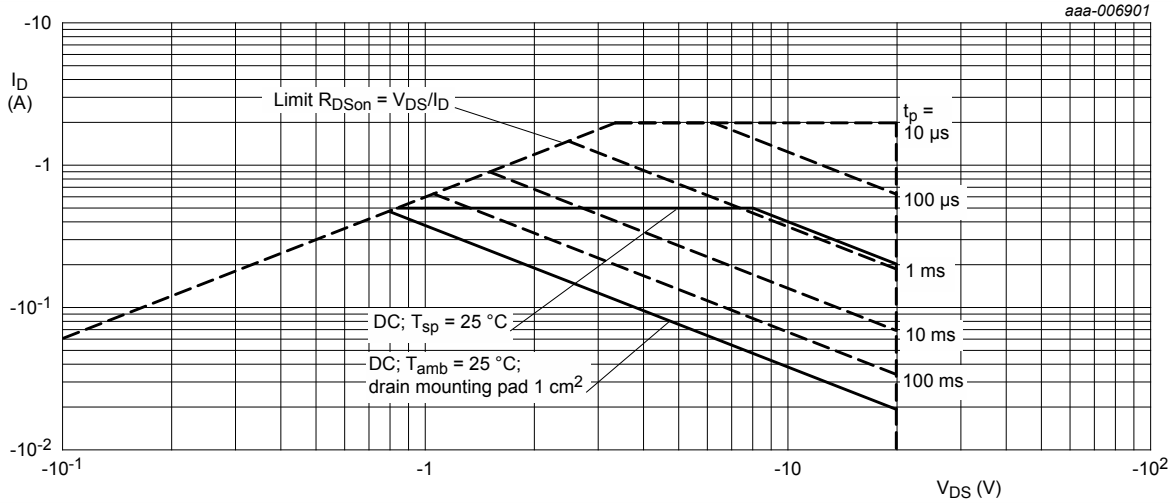


Fig. 3. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100 \%$$



$I_{DM}$  = single pulse

Fig. 4. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	410	475 K/W
			[2]	-	285	330 K/W

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	27	31	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.

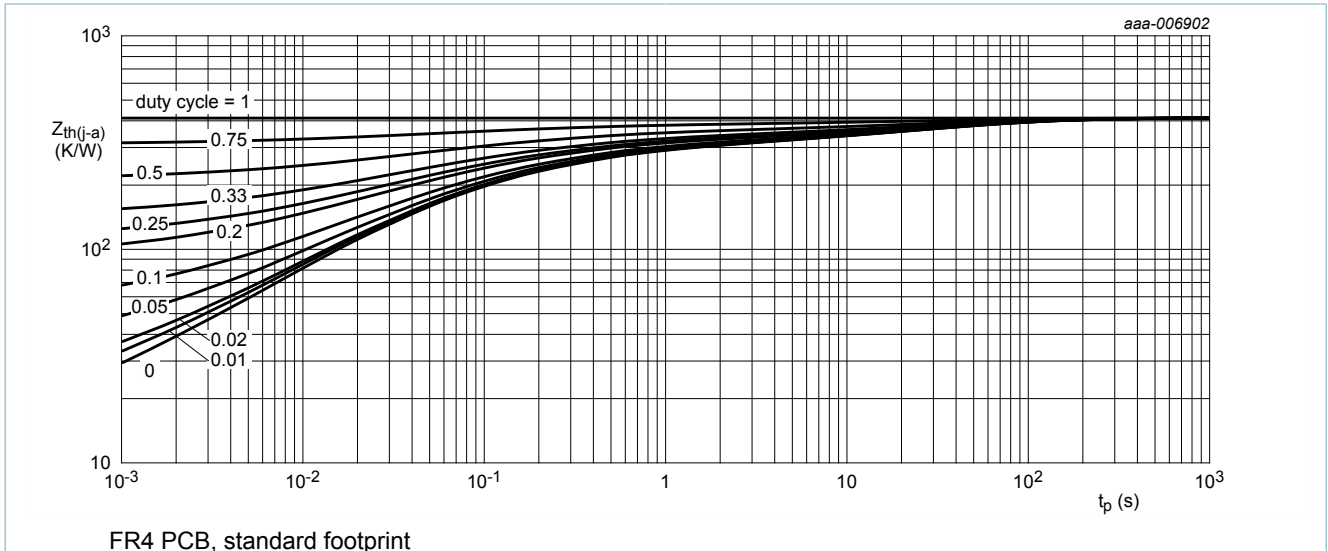


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

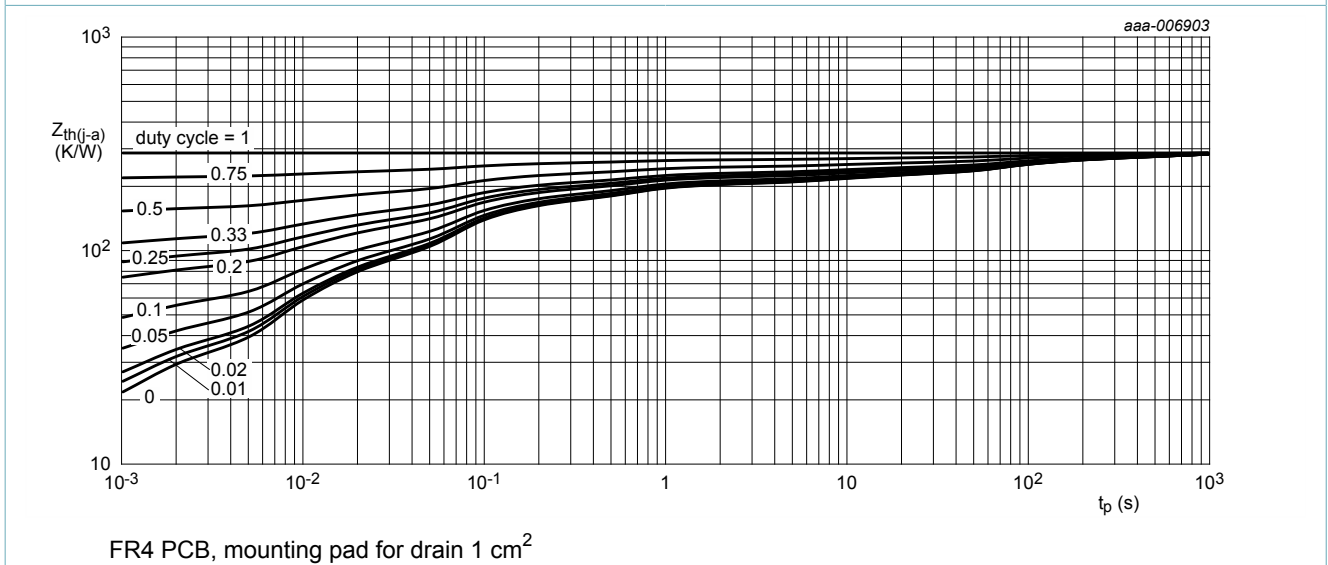
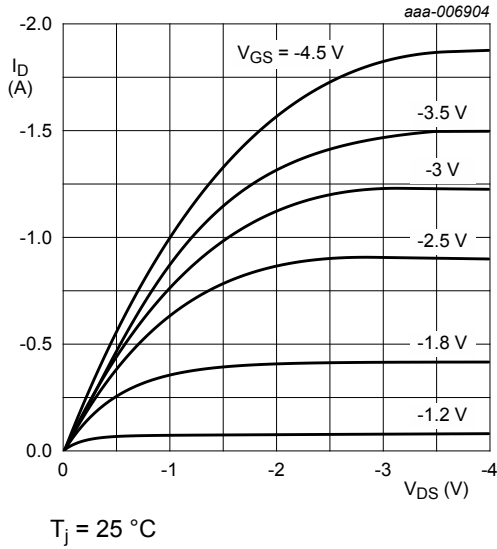


Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

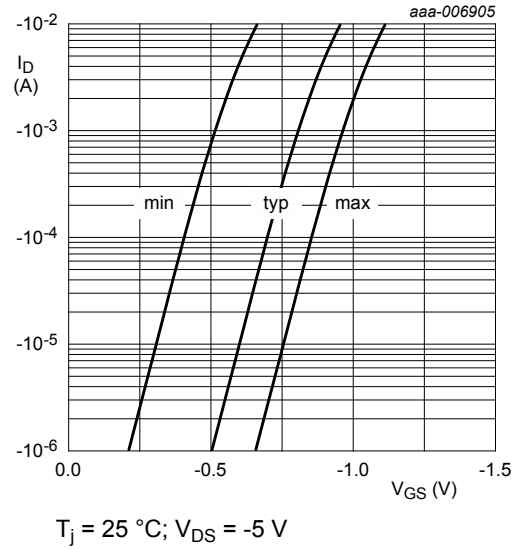
## 10. Characteristics

Table 7. Characteristics

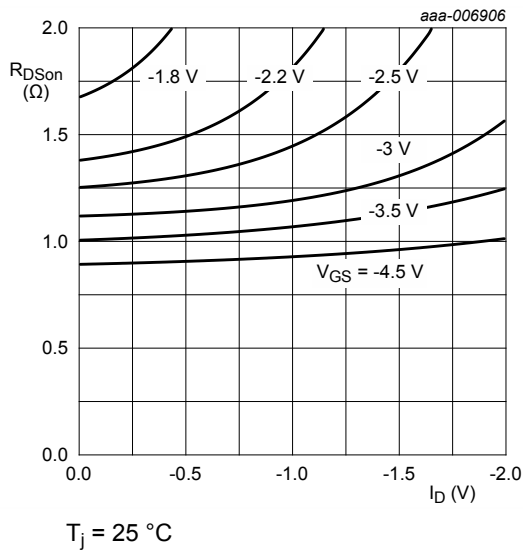
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics (per transistor)</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-20	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = -250 \mu A$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ C$	-0.45	-0.7	-0.95	V
$I_{DSS}$	drain leakage current	$V_{DS} = -20 V$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	-1	$\mu A$
		$V_{DS} = -20 V$ ; $V_{GS} = 0 V$ ; $T_j = 150 \text{ }^\circ C$	-	-	-10	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 8 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	10	$\mu A$
		$V_{GS} = -8 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	-10	$\mu A$
		$V_{GS} = 4.5 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	1	$\mu A$
		$V_{GS} = -4.5 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	-1	$\mu A$
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5 V$ ; $I_D = -500 \text{ mA}$ ; $T_j = 25 \text{ }^\circ C$	-	1.02	1.4	$\Omega$
		$V_{GS} = -4.5 V$ ; $I_D = -500 \text{ mA}$ ; $T_j = 150 \text{ }^\circ C$	-	1.54	2.1	$\Omega$
		$V_{GS} = -2.5 V$ ; $I_D = -200 \text{ mA}$ ; $T_j = 25 \text{ }^\circ C$	-	1.27	2.2	$\Omega$
		$V_{GS} = -1.8 V$ ; $I_D = -40 \text{ mA}$ ; $T_j = 25 \text{ }^\circ C$	-	1.7	3.3	$\Omega$
		$V_{GS} = -1.5 V$ ; $I_D = -10 \text{ mA}$ ; $T_j = 25 \text{ }^\circ C$	-	2.3	5	$\Omega$
		$V_{GS} = -1.2 V$ ; $I_D = -1 \text{ mA}$ ; $T_j = 25 \text{ }^\circ C$	-	3.5	-	$\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = -10 V$ ; $I_D = -500 \text{ mA}$ ; $T_j = 25 \text{ }^\circ C$	-	480	-	mS
<b>Dynamic characteristics (per transistor)</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -10 V$ ; $I_D = -450 \text{ mA}$ ; $V_{GS} = -4.5 V$ ; $T_j = 25 \text{ }^\circ C$	-	1.19	2.1	nC
$Q_{GS}$	gate-source charge		-	0.17	-	nC
$Q_{GD}$	gate-drain charge		-	0.1	-	nC
$C_{iss}$	input capacitance	$V_{DS} = -10 V$ ; $f = 1 \text{ MHz}$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	43	-	pF
$C_{oss}$	output capacitance		-	14	-	pF
$C_{rss}$	reverse transfer capacitance		-	8	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -10 V$ ; $I_D = -0.45 \text{ A}$ ; $R_L = 22 \Omega$ ; $V_{GS} = -4.5 V$ ; $R_{G(ext)} = 6 \Omega$ ; $T_j = 25 \text{ }^\circ C$	-	2.3	-	ns
$t_r$	rise time		-	5	-	ns
$t_{d(off)}$	turn-off delay time		-	13.5	-	ns
$t_f$	fall time		-	6	-	ns
<b>Source-drain diode (per transistor)</b>						
$V_{SD}$	source-drain voltage	$I_S = -115 \text{ mA}$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-0.7	-1.2	V



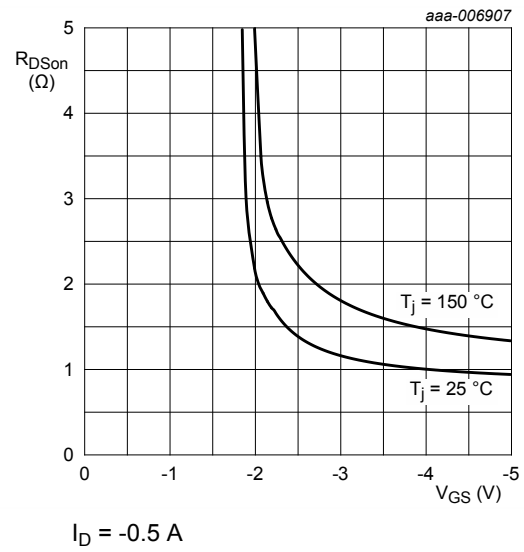
**Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values**



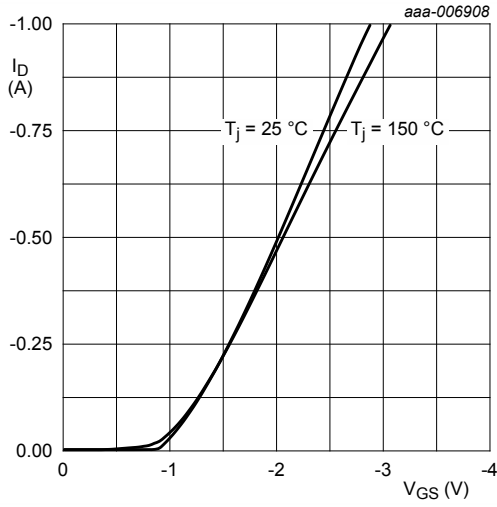
**Fig. 8. Sub-threshold drain current as a function of gate-source voltage**



**Fig. 9. Drain-source on-state resistance as a function of drain current; typical values**



**Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values**



$$V_{DS} > I_D \times R_{DSon}$$

Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values

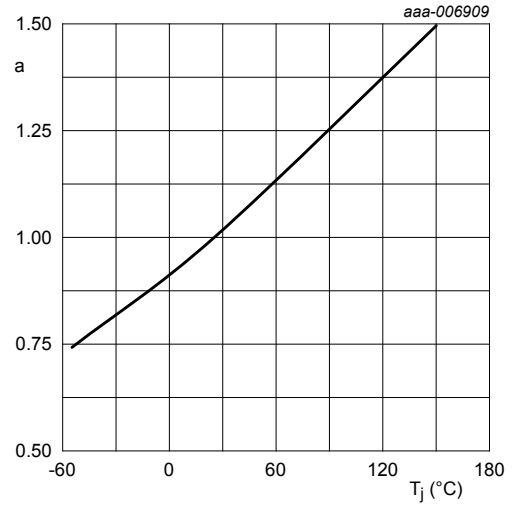
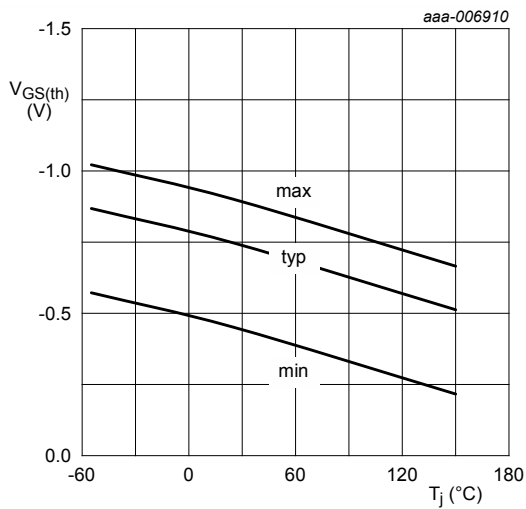


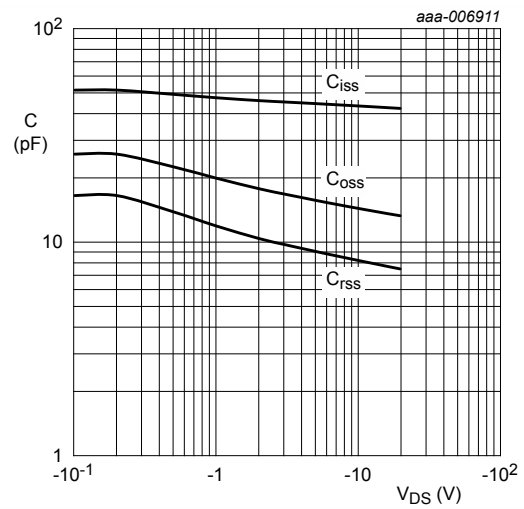
Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$



$$I_D = -0.25 \text{ mA}; V_{DS} = V_{GS}$$

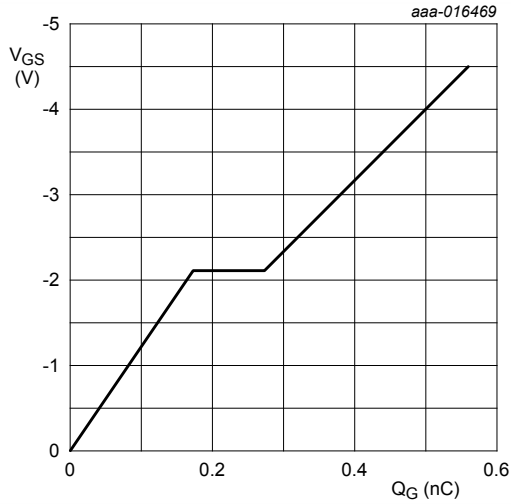
Fig. 13. Gate-source threshold voltage as a function of junction temperature



$$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$$

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



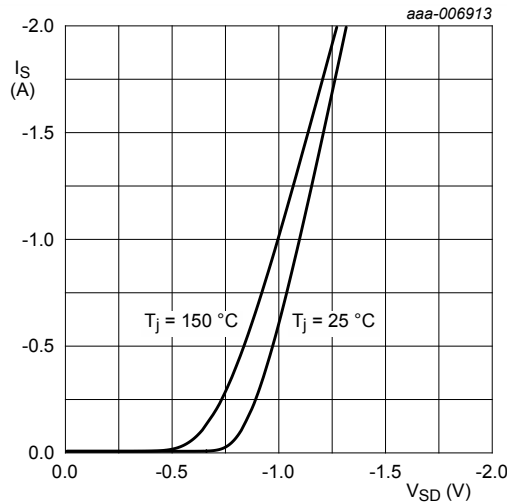


$I_D = -0.5$  A;  $V_{DS} = -10$  V;  $T_{amb} = 25$  °C

Fig. 15. Gate-source voltage as a function of gate charge; typical values



Fig. 16. MOSFET transistor: Gate charge waveform definitions



$V_{GS} = 0$  V

Fig. 17. Source current as a function of source-drain voltage; typical values

## 11. Test information



Fig. 18. Duty cycle definition

## 12. Package outline

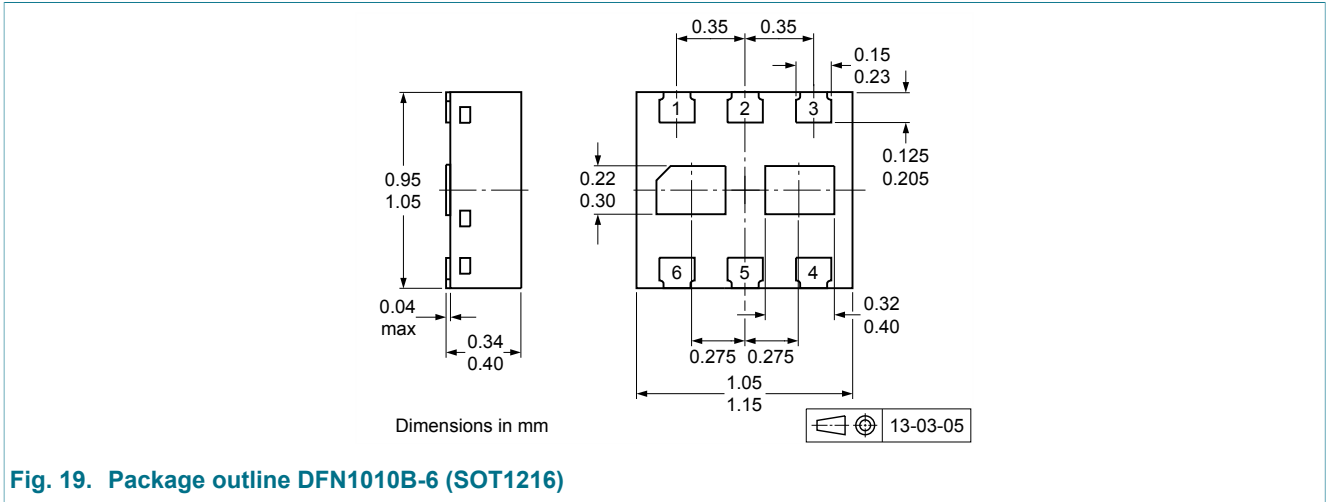


Fig. 19. Package outline DFN1010B-6 (SOT1216)

### 13. Soldering

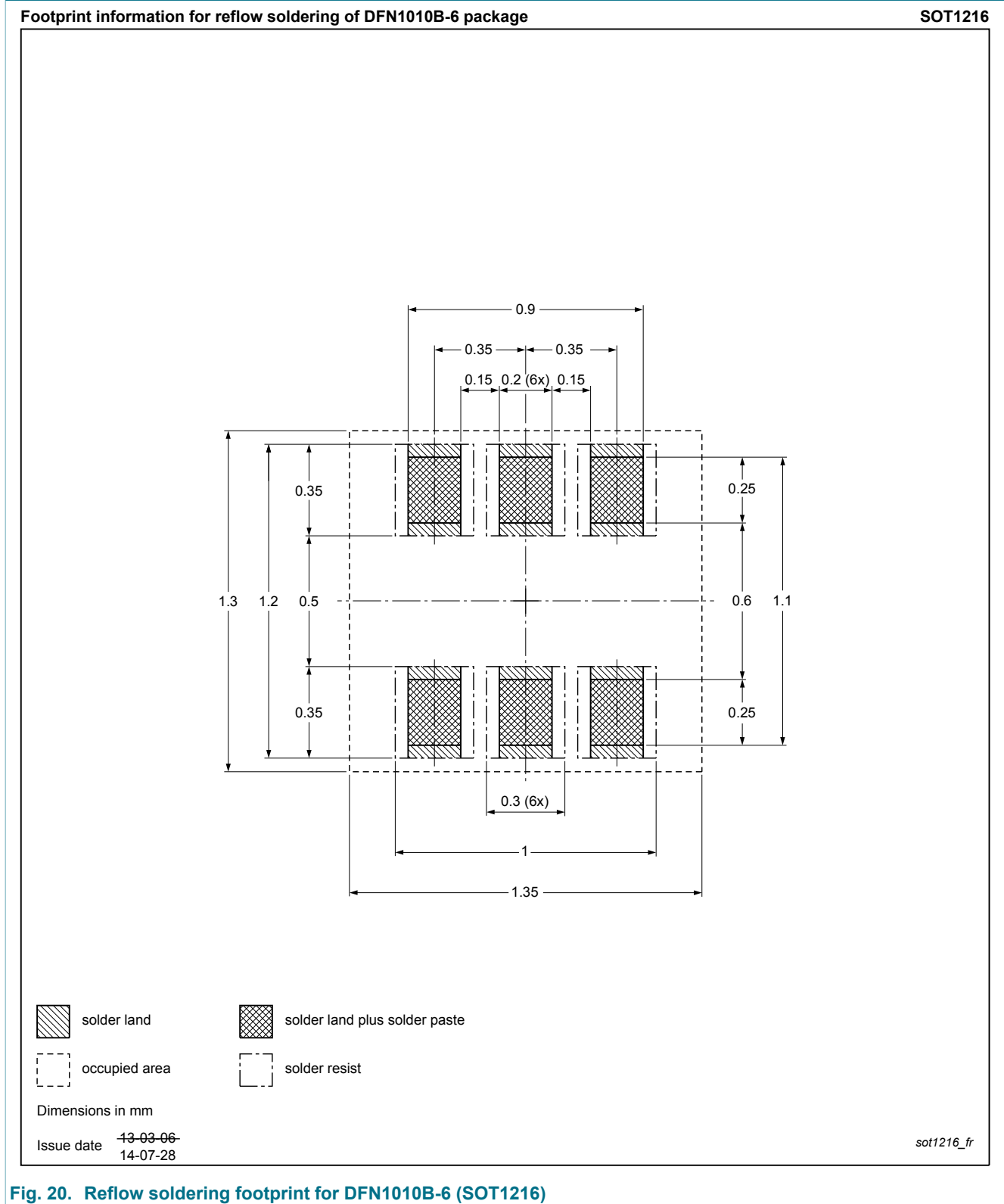


Fig. 20. Reflow soldering footprint for DFN1010B-6 (SOT1216)

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMDXB950UPE v.2	20150630	Product data sheet	-	PMDXB950UPE v.1
Modification:	<ul style="list-style-type: none"><li>Change of binary marking code position.</li></ul>			
PMDXB950UPE v.1	20130910	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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