

MOSFETs Silicon N-channel MOS (U-MOS<sup>Ⅷ</sup>-H)

# TK100E10N1

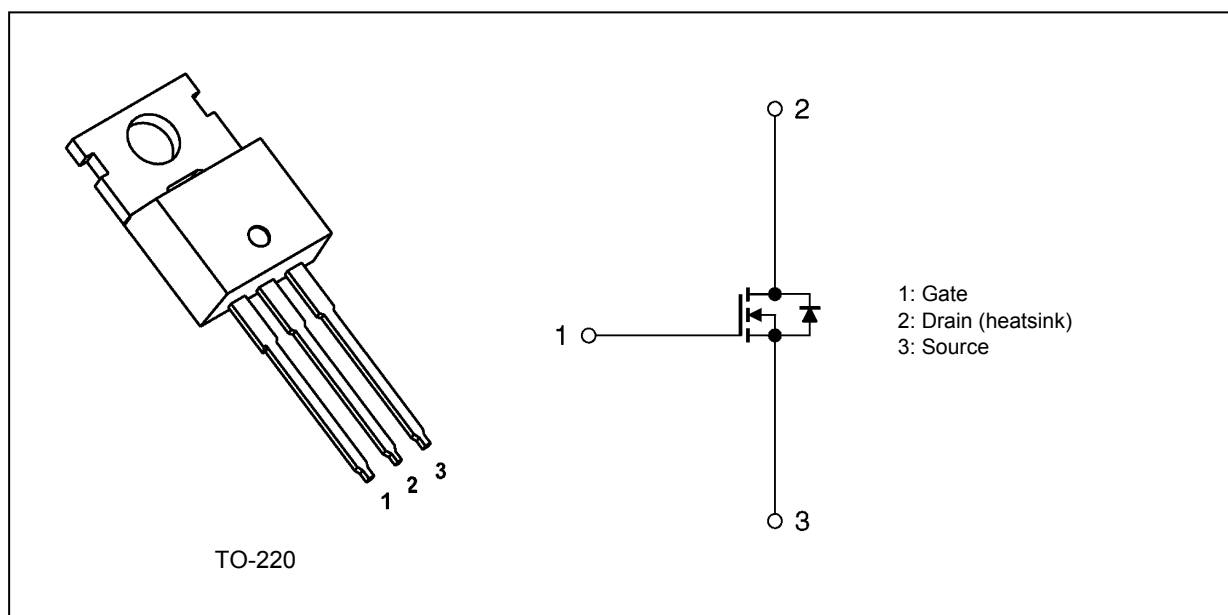
## 1. Applications

- Switching Voltage Regulators

## 2. Features

- (1) Low drain-source on-resistance:  $R_{DS(ON)} = 2.8 \text{ m}\Omega$  (typ.) ( $V_{GS} = 10 \text{ V}$ )
- (2) Low leakage current:  $I_{DSS} = 10 \text{ }\mu\text{A}$  (max) ( $V_{DS} = 100 \text{ V}$ )
- (3) Enhancement mode:  $V_{th} = 2.0 \text{ to } 4.0 \text{ V}$  ( $V_{DS} = 10 \text{ V}$ ,  $I_D = 1.0 \text{ mA}$ )

## 3. Packaging and Internal Circuit



## 4. Absolute Maximum Ratings (Note) ( $T_a = 25^\circ\text{C}$ unless otherwise specified)

| Characteristics  | Symbol    | Rating     | Unit             |
|--|-----------|------------|------------------|
| Drain-source voltage                                   | $V_{DSS}$ | 100        | V                |
| Gate-source voltage                                    | $V_{GSS}$ | $\pm 20$   |                  |
| Drain current (DC) (Silicon limit) (Note 1,2)          | $I_D$     | 207        | A                |
| Drain current (DC) (Note 1,3)                          | $I_D$     | 100        |                  |
| Drain current (pulsed) ( $t = 1 \text{ ms}$ ) (Note 1) | $I_{DP}$  | 434        |                  |
| Power dissipation ( $T_c = 25^\circ\text{C}$ )         | $P_D$     | 255        | W                |
| Single-pulse avalanche energy (Note 4)                 | $E_{AS}$  | 222        | mJ               |
| Avalanche current                                      | $I_{AR}$  | 100        | A                |
| Channel temperature                                    | $T_{ch}$  | 150        | $^\circ\text{C}$ |
| Storage temperature                                    | $T_{stg}$ | -55 to 150 |                  |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production

2012-01

## 5. Thermal Characteristics

| Characteristics                       | Symbol         | Max  | Unit |
|---------------------------------------|----------------|------|------|
| Channel-to-case thermal resistance    | $R_{th(ch-c)}$ | 0.49 | °C/W |
| Channel-to-ambient thermal resistance | $R_{th(ch-a)}$ | 83.3 |      |

Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: Limited by silicon chip capability. Package limit is 100 A.

Note 3: Device mounted with heatsink so that  $R_{th(ch-a)}$  becomes 2.77°C/W.

Note 4:  $V_{DD} = 80$  V,  $T_{ch} = 25$ °C (initial),  $L = 17.1$   $\mu$ H,  $I_{AR} = 100$  A

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

**6. Electrical Characteristics**

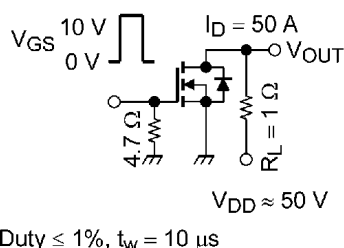
**6.1. Static Characteristics ( $T_a = 25^\circ\text{C}$  unless otherwise specified)**

| Characteristics                         | Symbol        | Test Condition                                  | Min | Typ. | Max       | Unit             |
|---|---------------|---|-----|------|-----------|------------------|
| Gate leakage current                    | $I_{GSS}$     | $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$ | —   | —    | $\pm 0.1$ | $\mu\text{A}$    |
| Drain cut-off current                   | $I_{DSS}$     | $V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$    | —   | —    | 10        |                  |
| Drain-source breakdown voltage          | $V_{(BR)DSS}$ | $I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$       | 100 | —    | —         | V                |
| Drain-source breakdown voltage (Note 5) | $V_{(BR)DSX}$ | $I_D = 10\text{ mA}, V_{GS} = -20\text{ V}$     | 65  | —    | —         |                  |
| Gate threshold voltage                  | $V_{th}$      | $V_{DS} = 10\text{ V}, I_D = 1.0\text{ mA}$     | 2.0 | —    | 4.0       |                  |
| Drain-source on-resistance              | $R_{DS(ON)}$  | $V_{GS} = 10\text{ V}, I_D = 50\text{ A}$       | —   | 2.8  | 3.4       | $\text{m}\Omega$ |

Note 5: If a reverse bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

**6.2. Dynamic Characteristics ( $T_a = 25^\circ\text{C}$  unless otherwise specified)**

| Characteristics                | Symbol    | Test Condition  | Min | Typ. | Max | Unit        |
|--------------------------------|-----------|---|-----|------|-----|-------------|
| Input capacitance              | $C_{iss}$ | $V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$ | —   | 8800 | —   | $\text{pF}$ |
| Reverse transfer capacitance   | $C_{rss}$ |   | —   | 63   | —   |             |
| Output capacitance             | $C_{oss}$ |   | —   | 1500 | —   |             |
| Gate resistance                | $r_g$     | —   | —   | 2.6  | —   | $\Omega$    |
| Switching time (rise time)     | $t_r$     | See Figure 6.2.1  | —   | 32   | —   | ns          |
| Switching time (turn-on time)  | $t_{on}$  |   | —   | 59   | —   |             |
| Switching time (fall time)     | $t_f$     |   | —   | 45   | —   |             |
| Switching time (turn-off time) | $t_{off}$ |   | —   | 140  | —   |             |



**Fig. 6.2.1 Switching Time Test Circuit**

**6.3. Gate Charge Characteristics ( $T_a = 25^\circ\text{C}$  unless otherwise specified)**

| Characteristics                                 | Symbol    | Test Condition   | Min | Typ. | Max | Unit |
|---|-----------|--|-----|------|-----|------|
| Total gate charge (gate-source plus gate-drain) | $Q_g$     | $V_{DD} \approx 80\text{ V}, V_{GS} = 10\text{ V}, I_D = 100\text{ A}$ | —   | 140  | —   | nC   |
| Gate-source charge 1                            | $Q_{gs1}$ |  | —   | 46   | —   |      |
| Gate-drain charge                               | $Q_{gd}$  |  | —   | 34   | —   |      |
| Gate switch charge                              | $Q_{sw}$  |  | —   | 55   | —   |      |

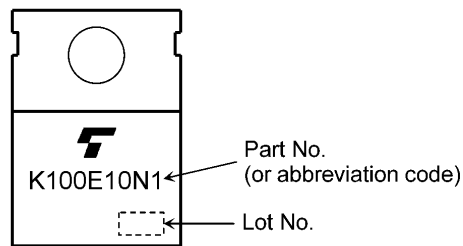
**6.4. Source-Drain Characteristics ( $T_a = 25^\circ\text{C}$  unless otherwise specified)**

| Characteristics                         | Symbol    | Test Condition   | Min | Typ. | Max  | Unit |
|---|-----------|--|-----|------|------|------|
| Reverse drain current (DC) (Note 6)     | $I_{DR}$  | —  | —   | —    | 100  | A    |
| Reverse drain current (pulsed) (Note 6) | $I_{DRP}$ | —  | —   | —    | 434  |      |
| Diode forward voltage                   | $V_{DSF}$ | $I_{DR} = 100\text{ A}, V_{GS} = 0\text{ V}$   | —   | —    | -1.2 | V    |
| Reverse recovery time (Note 7)          | $t_{rr}$  | $I_{DR} = 100\text{ A}, V_{GS} = 0\text{ V}$<br>$-di_{DR}/dt = 100\text{ A}/\mu\text{s}$ | —   | 93   | —    | ns   |
| Reverse recovery charge (Note 7)        | $Q_{rr}$  |  | —   | 220  | —    | nC   |

Note 6: Ensure that the channel temperature does not exceed  $150^\circ\text{C}$ .

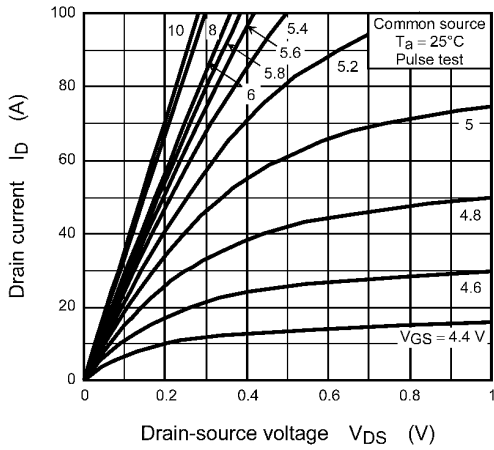
Note 7: Ensure that  $V_{DS}$  peak does not exceed  $V_{DSS}$ .

**7. Marking**

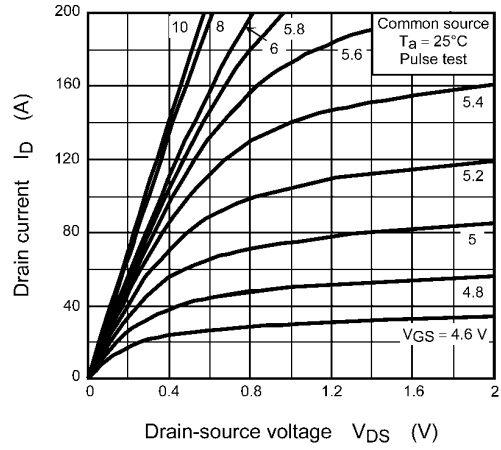


**Fig. 7.1 Marking**

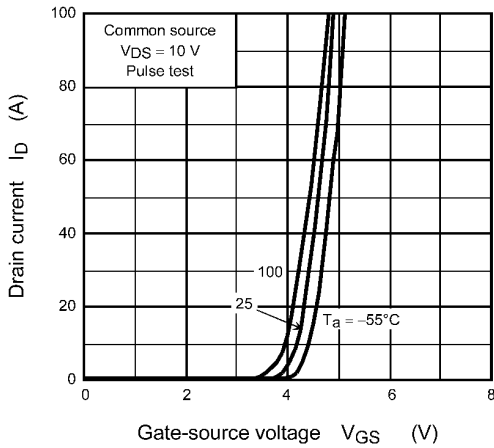
**8. Characteristics Curves (Note)**



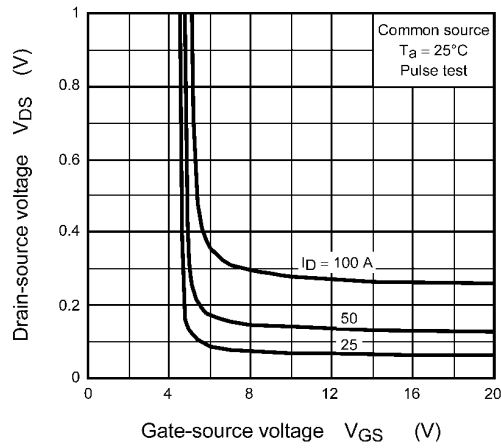
**Fig. 8.1  $I_D - V_{DS}$**



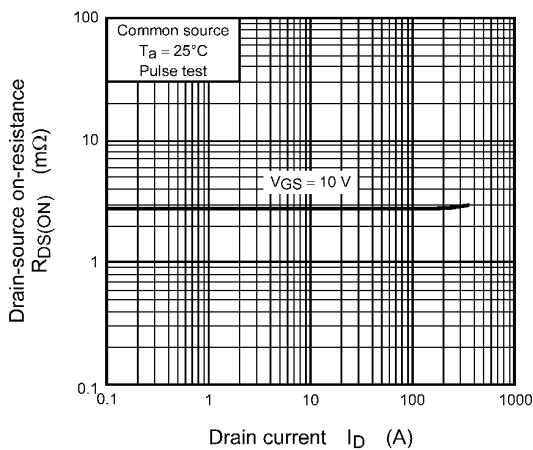
**Fig. 8.2  $I_D - V_{DS}$**



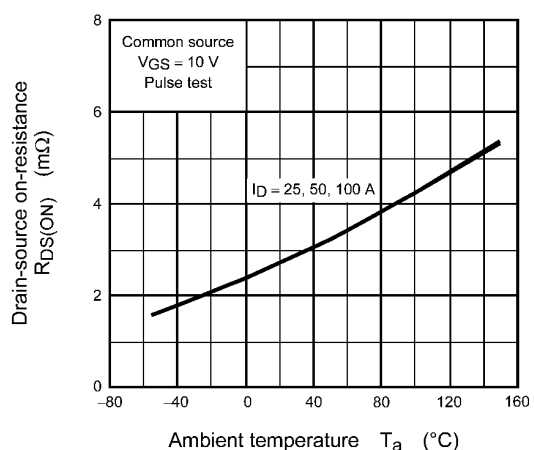
**Fig. 8.3  $I_D - V_{GS}$**



**Fig. 8.4  $V_{DS} - V_{GS}$**



**Fig. 8.5  $R_{DS(ON)} - I_D$**



**Fig. 8.6  $R_{DS(ON)} - T_a$**

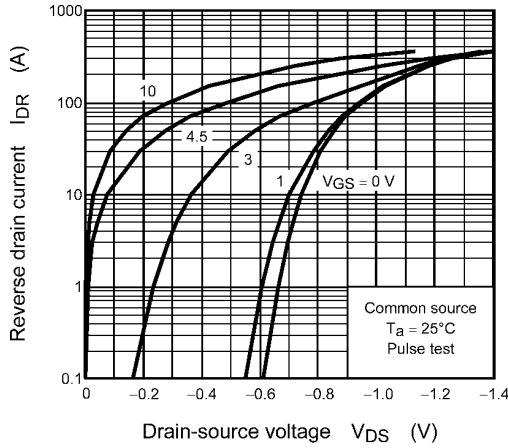


Fig. 8.7  $I_{DR} - V_{DS}$

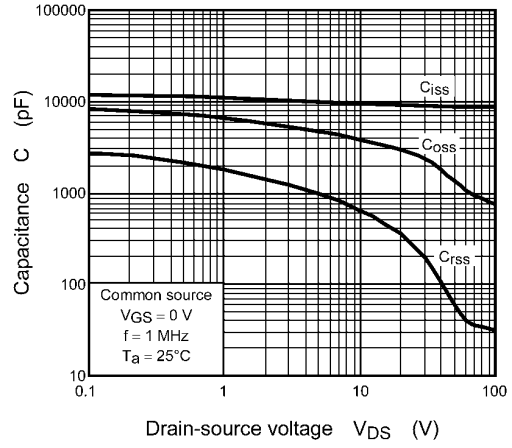


Fig. 8.8 Capacitance -  $V_{DS}$

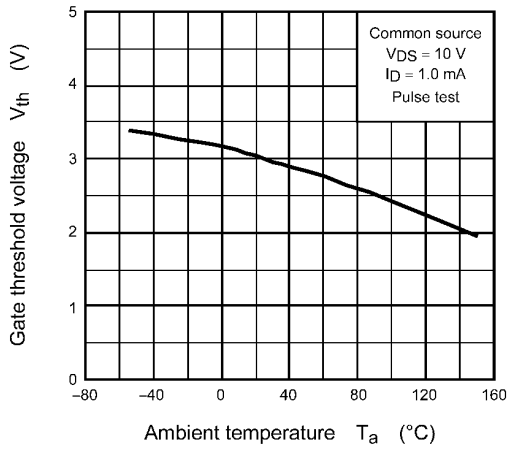


Fig. 8.9  $V_{th} - T_a$

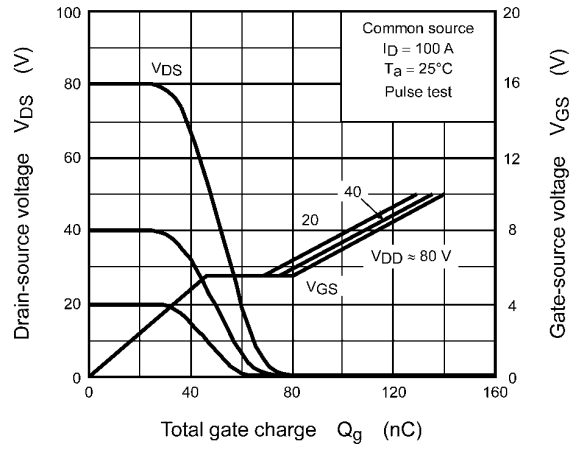


Fig. 8.10 Dynamic Input/Output Characteristics

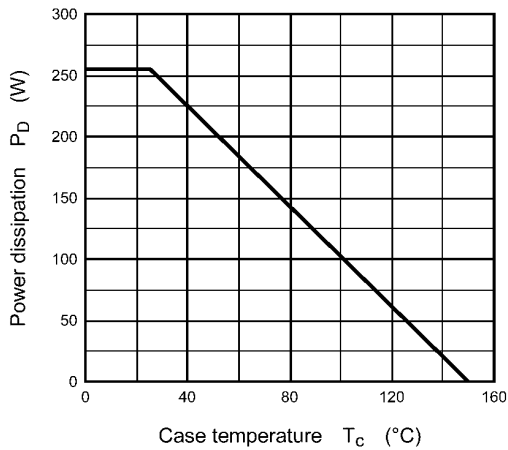
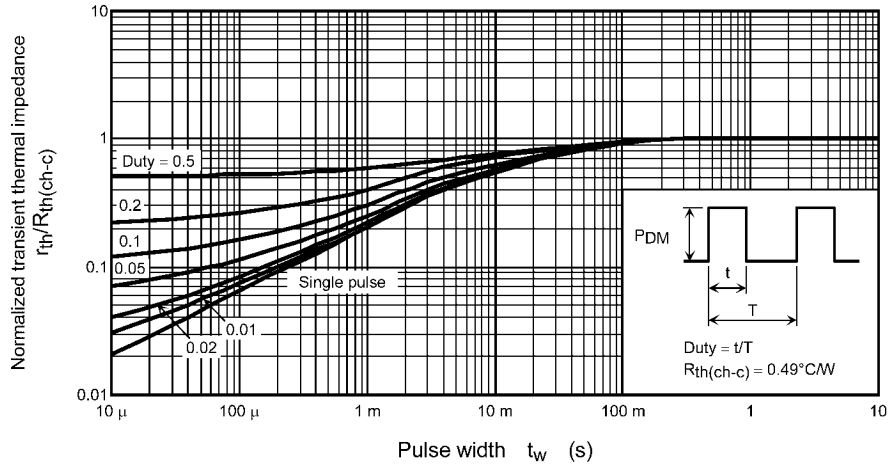
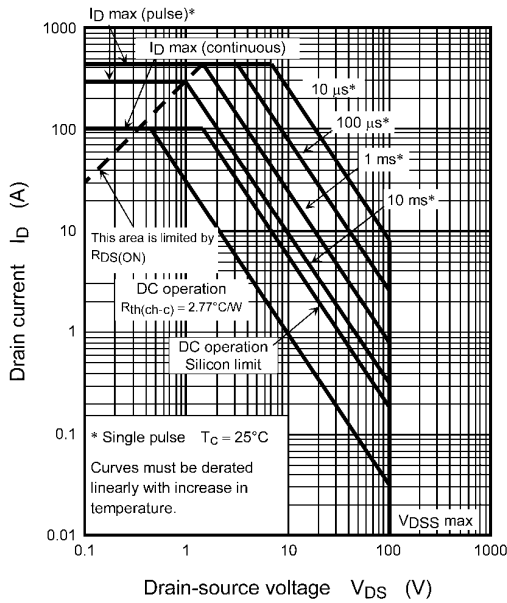


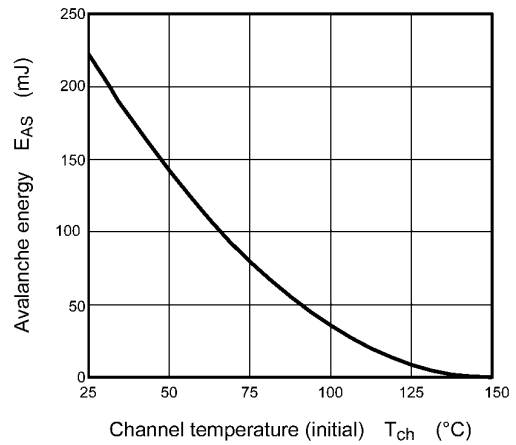
Fig. 8.11  $P_D - T_c$   
(Guaranteed Maximum)



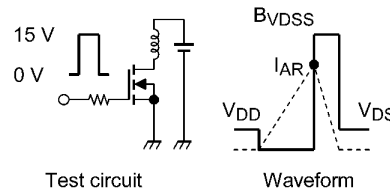
**Fig. 8.12  $r_{th}/R_{th(ch-c)} - t_w$  (Guaranteed Maximum)**



**Fig. 8.13 Safe Operating Area (Guaranteed Maximum)**



**Fig. 8.14  $E_{AS} - T_{ch}$  (Guaranteed Maximum)**



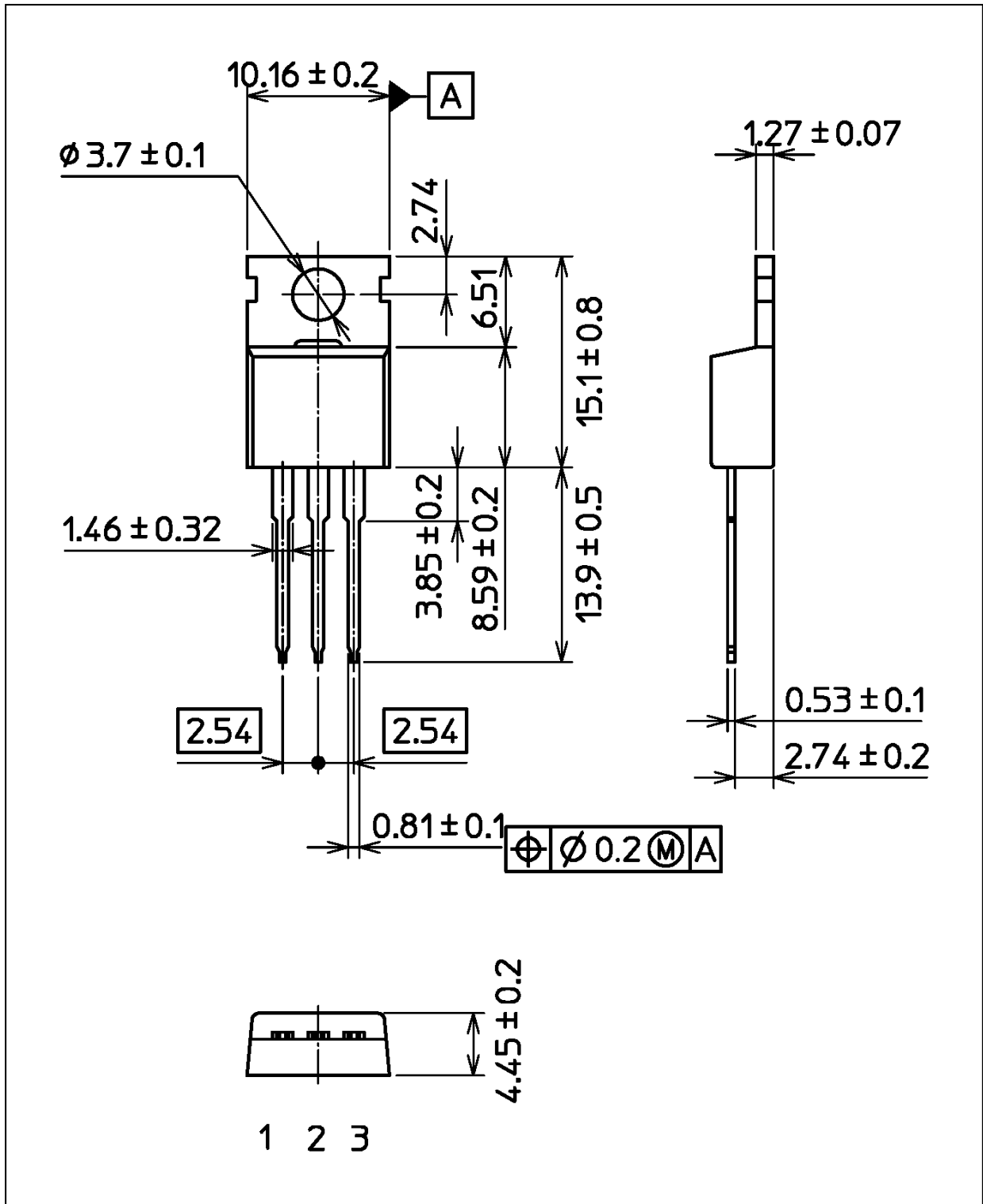
$$V_{DD} = 80 \text{ V}, I_{AR} = 100 \text{ A} \quad E_{AS} = \frac{1}{2} \cdot L \cdot I_{AR}^2 \cdot \left( \frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

**Fig. 8.15 Test Circuit/Waveform**

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 1.93 g (typ.)

|                  |
|------------------|
| Package Name(s)  |
| TOSHIBA: 2-10X1A |
| Nickname: TO-220 |



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