

TOSHIBA Field Effect Transistor Silicon N, P Channel MOS Type
(P Channel U-MOS IV/N Channel U-MOS III)

TPC8405

Lithium Ion Secondary Battery Applications

Portable Equipment Applications

Notebook PC Applications

Unit: mm

- Low drain-source ON resistance : P Channel $R_{DS(ON)} = 25 \text{ m}\Omega$ (typ.)
N Channel $R_{DS(ON)} = 20 \text{ m}\Omega$ (typ.)
- High forward transfer admittance : P Channel $|Y_{fs}| = 12\text{S}$ (typ.)
N Channel $|Y_{fs}| = 14\text{S}$ (typ.)
- Low leakage current : P Channel $I_{DSS} = -10 \text{ }\mu\text{A}$ ($V_{DS} = -30 \text{ V}$)
N Channel $I_{DSS} = 10 \text{ }\mu\text{A}$ ($V_{DS} = 30 \text{ V}$)
- Enhancement-mode
: P Channel $V_{th} = -0.8 \text{ to } -2.0 \text{ V}$ ($V_{DS} = -10 \text{ V}$, $I_D = -1 \text{ mA}$)
N Channel $V_{th} = 1.3 \text{ to } 2.5 \text{ V}$ ($V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$)

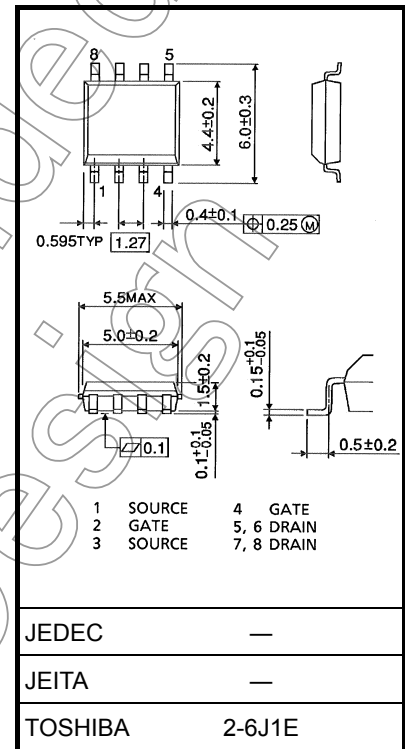
Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Characteristics		Symbol	Rating		Unit
			P Channel	N Channel	
Drain-source voltage		V_{DSS}	-30	30	V
Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)		V_{DGR}	-30	30	V
Gate-source voltage		V_{GSS}	± 20	± 20	V
Drain current	DC (Note 1)	I_D	-4.5	6	A
	Pulse (Note 1)	I_{DP}	-18	24	
Drain power dissipation ($t = 10\text{s}$) (Note 2a)	Single-device operation (Note 3a)	$P_D(1)$	1.5	1.5	W
	Single-device value at dual operation (Note 3b)	$P_D(2)$	1.1	1.1	
Drain power dissipation ($t = 10\text{s}$) (Note 2b)	Single-device operation (Note 3a)	$P_D(1)$	0.75	0.75	
	Single-device value at dual operation (Note 3b)	$P_D(2)$	0.45	0.45	
Single pulse avalanche energy		E_{AS}	13.2 (Note 4a)	23.4 (Note 4b)	mJ
Avalanche current		I_{AR}	-4.5	6	A
Repetitive avalanche energy Single-device value at operation (Note 2a, 3b, 5)		E_{AR}	0.1		mJ
Channel temperature		T_{ch}	150		$^\circ\text{C}$
Storage temperature range		T_{stg}	-55 to 150		$^\circ\text{C}$

Note: For Notes 1 to 5, refer to the next page.

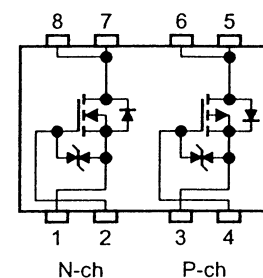
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

This transistor is an electrostatic-sensitive device. Handle with care.



Weight: 0.080 g (typ.)

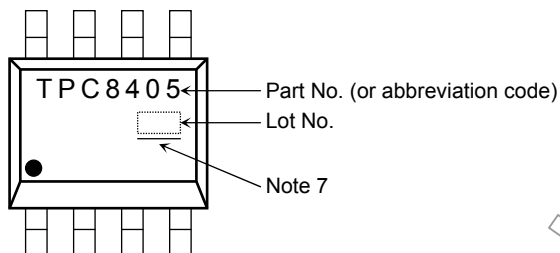
Circuit Configuration



Thermal Characteristics

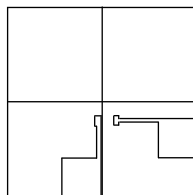
Characteristics		Symbol	Max	Unit
Thermal resistance, channel to ambient (t = 10s)	Single-device operation (Note 3a)	$R_{th(ch-a)}(1)$	83.3	°C/W
	Single-device value at dual operation (Note 3b)	$R_{th(ch-a)}(2)$	114	
Thermal resistance, channel to ambient (t = 10s)	Single-device operation (Note 3a)	$R_{th(ch-a)}(1)$	167	
	Single-device value at dual operation (Note 3b)	$R_{th(ch-a)}(2)$	278	

Marking (Note 6)

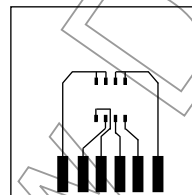


Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: a) Device mounted on a glass-epoxy board (a) b) Device mounted on a glass-epoxy board (b)



(a)



(b)

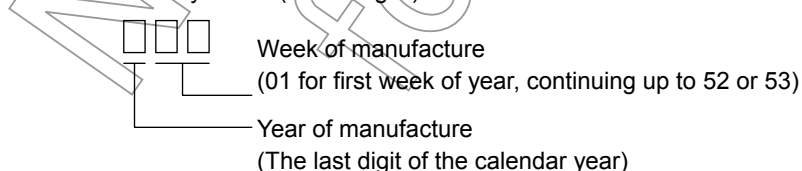
Note 3: a) The power dissipation and thermal resistance values shown are for a single device. (During single-device operation, power is applied to one device only.)
b) The power dissipation and thermal resistance values shown are for a single device. (During dual operation, power is evenly applied to both devices.)

Note 4: a) $V_{DD} = -24$ V, $T_{ch} = 25^\circ\text{C}$ (initial), $L = 0.5$ mH, $R_G = 25$ Ω , $I_{AR} = -4.5$ A
b) $V_{DD} = 24$ V, $T_{ch} = 25^\circ\text{C}$ (initial), $L = 0.5$ mH, $R_G = 25$ Ω , $I_{AR} = 6.0$ A

Note 5: Repetitive rating: pulse width limited by maximum channel temperature

Note 6: • on the lower left of the marking indicates Pin 1.

* Weekly code: (Three digits)



Note 7: A line under a Lot No. identifies the indication of product Labels.

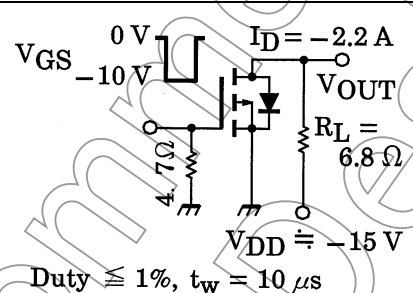
Not underlined: [[Pb]]/INCLUDES > MCV

Underlined: [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

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P-ch

Electrical Characteristics (Ta = 25°C)

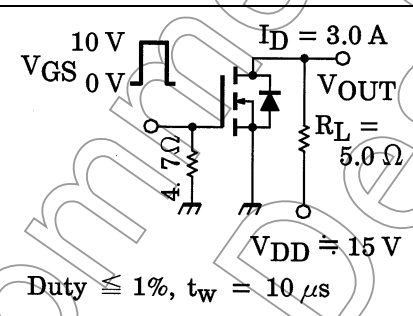
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	± 10	μA
Drain cut-OFF current		I_{DSS}	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	-10	μA
Drain-source breakdown voltage	$V_{(BR) DSS}$		$I_D = -10 \text{ mA}, V_{GS} = 0 \text{ V}$	-30	—	—	V
	$V_{(BR) DSX}$		$I_D = -10 \text{ mA}, V_{GS} = 20 \text{ V}$	-15	—	—	
Gate threshold voltage		V_{th}	$V_{DS} = -10 \text{ V}, I_D = -1 \text{ mA}$	-0.8	—	-2.0	V
Drain-source ON resistance	$R_{DS(ON)}$		$V_{GS} = -4.5 \text{ V}, I_D = -2.2 \text{ A}$	—	32	42	m Ω
	$R_{DS(ON)}$		$V_{GS} = -10 \text{ V}, I_D = -2.2 \text{ A}$	—	25	33	
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = -10 \text{ V}, I_D = -2.2 \text{ A}$	6	12	—	S
Input capacitance		C_{iss}	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	1540	—	pF
Reverse transfer capacitance		C_{rss}		—	220	—	
Output capacitance		C_{oss}		—	250	—	
Switching time	Rise time	t_r	 <p> V_{GS} 0 V -10 V $I_D = -2.2 \text{ A}$ V_{OUT} $R_L = 6.8 \Omega$ $V_{DD} = -15 \text{ V}$ $\text{Duty} \leq 1\%, t_w = 10 \mu\text{s}$ </p>	—	5.0	—	ns
	Turn-ON time	t_{on}		—	13	—	
	Fall time	t_f		—	35	—	
	Turn-OFF time	t_{off}		—	125	—	
Total gate charge (Gate-source plus gate-drain)		Q_g	$V_{DD} \approx -24 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -4.5 \text{ A}$	—	40	—	nC
Gate-source charge 1		Q_{gs1}		—	4.4	—	
Gate-drain ("miller") charge		Q_{gd}		—	8.2	—	

Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	-18	A
Forward voltage (diode)		V_{DSF}	$I_{DR} = -4.5 \text{ A}, V_{GS} = 0 \text{ V}$	—	—	1.2	V

N-ch

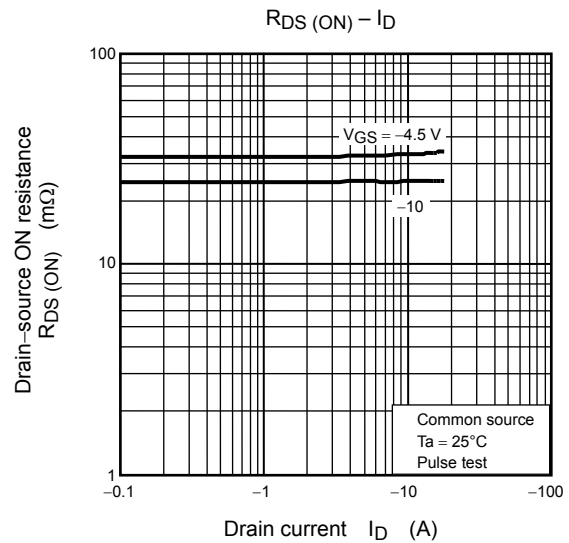
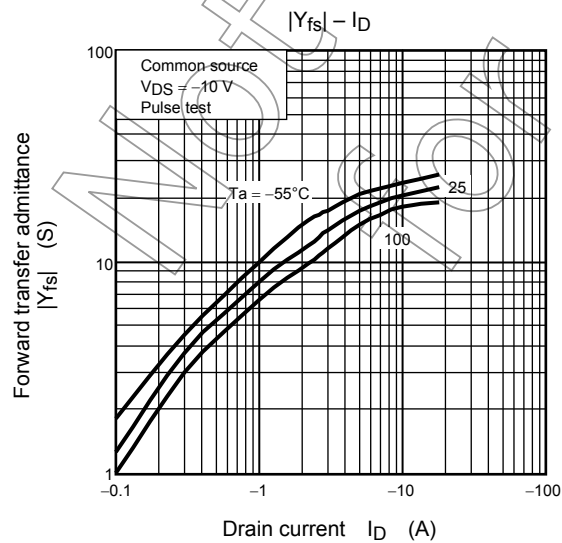
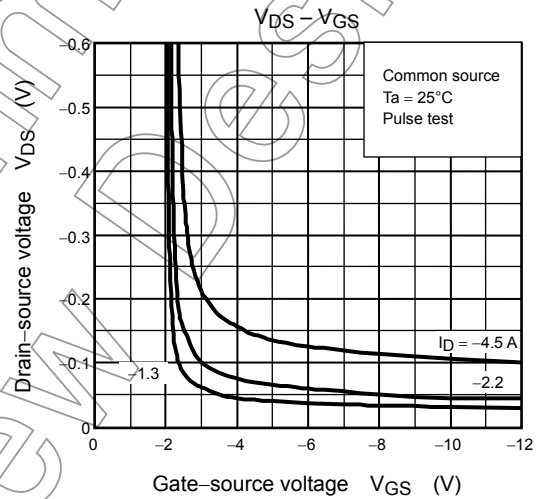
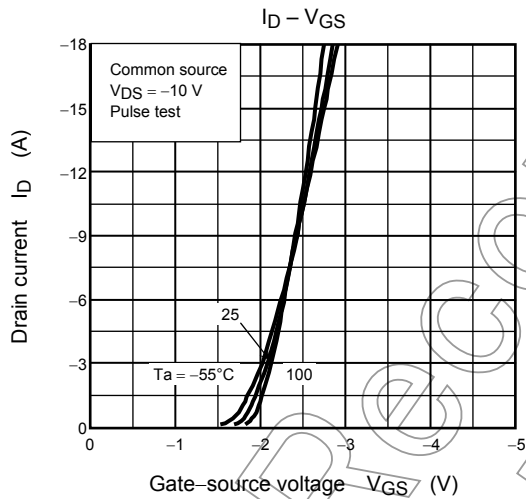
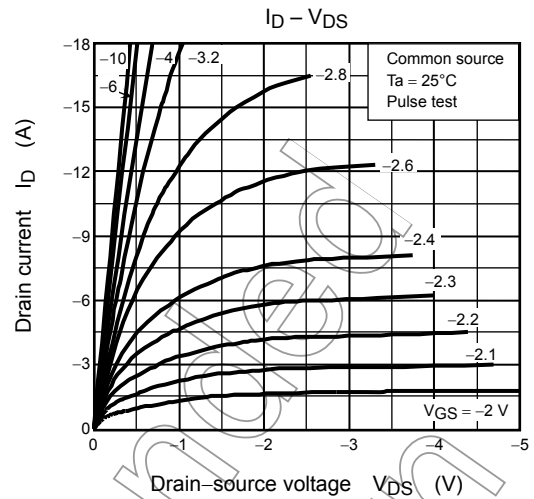
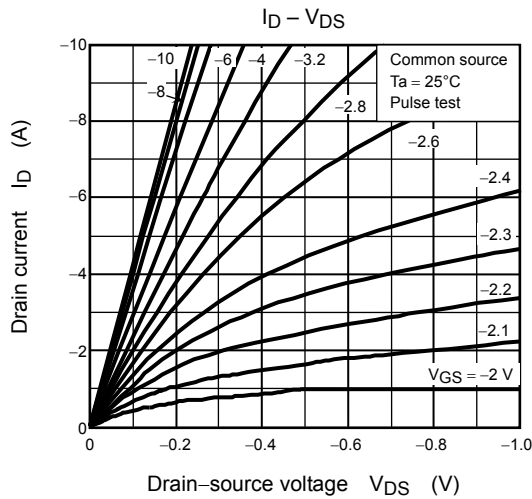
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	± 10	μA
Drain cut-OFF current		I_{DSS}	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	10	μA
Drain-source breakdown voltage	$V_{(BR) DSS}$		$I_D = 10 \text{ mA}, V_{GS} = 0 \text{ V}$	30	—	—	V
	$V_{(BR) DSX}$		$I_D = 10 \text{ mA}, V_{GS} = -20 \text{ V}$	15	—	—	
Gate threshold voltage		V_{th}	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$	1.3	—	2.5	V
Drain-source ON resistance	$R_{DS(ON)}$		$V_{GS} = 4.5 \text{ V}, I_D = 3 \text{ A}$	—	25	33	m Ω
	$R_{DS(ON)}$		$V_{GS} = 10 \text{ V}, I_D = 3 \text{ A}$	—	20	26	
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = 10 \text{ V}, I_D = 3 \text{ A}$	7	14	—	S
Input capacitance		C_{iss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	1240	—	pF
Reverse transfer capacitance		C_{rss}		—	180	—	
Output capacitance		C_{oss}		—	230	—	
Switching time	Rise time	t_r	 <p> 10 V V_{GS} 0 V $I_D = 3.0 \text{ A}$ V_{OUT} $R_L = 5.0 \Omega$ $V_{DD} \approx 15 \text{ V}$ $\text{Duty} \leq 1\%, t_w = 10 \mu\text{s}$ </p>	—	4.5	—	ns
	Turn-ON time	t_{on}		—	12.5	—	
	Fall time	t_f		—	6.6	—	
	Turn-OFF time	t_{off}		—	33	—	
Total gate charge (Gate-source plus gate-drain)		Q_g	$V_{DD} \approx 24 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 6 \text{ A}$	—	27	—	nC
Gate-source charge 1		Q_{gs1}		—	3.9	—	
Gate-drain ("miller") charge		Q_{gd}		—	7.0	—	

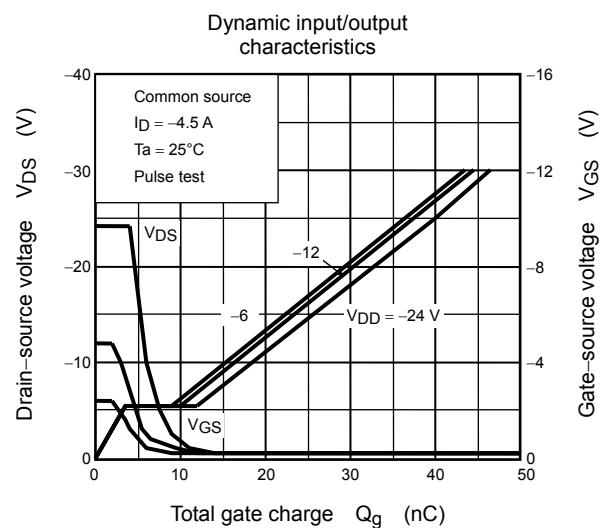
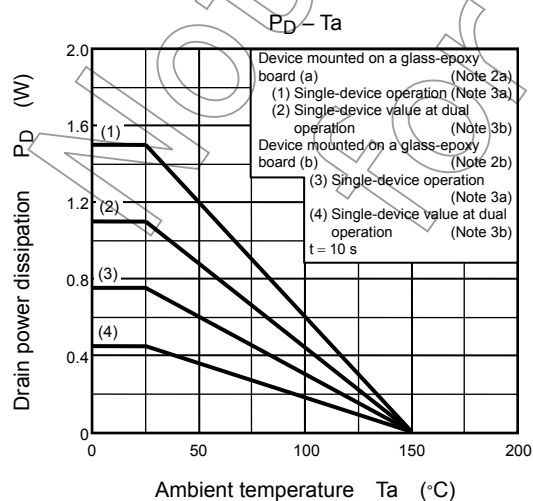
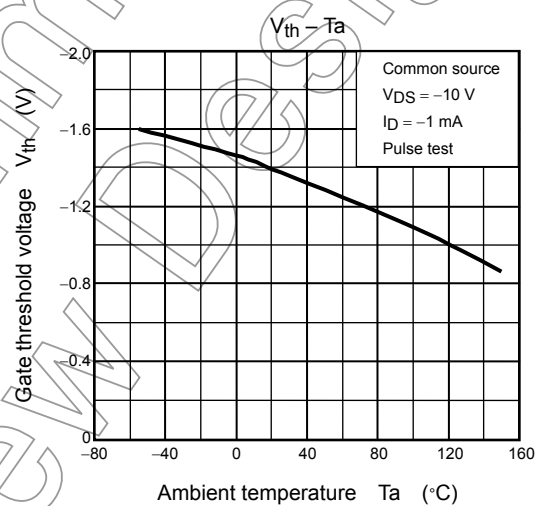
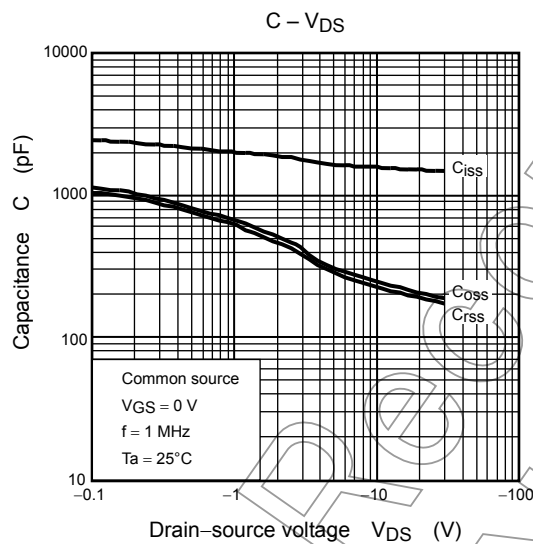
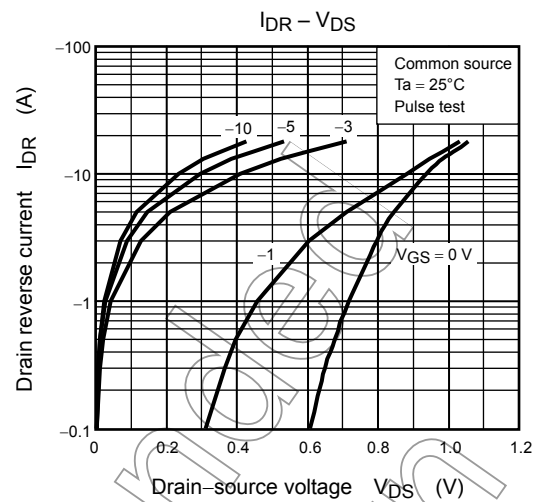
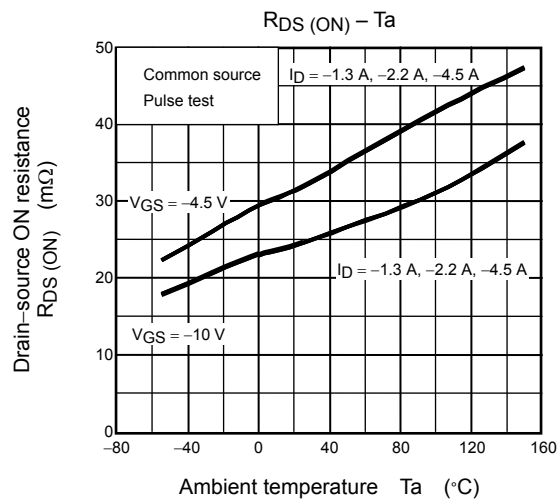
Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	24	A
Forward voltage (diode)		V_{DSF}	$I_{DR} = 6 \text{ A}, V_{GS} = 0 \text{ V}$	—	—	-1.2	V

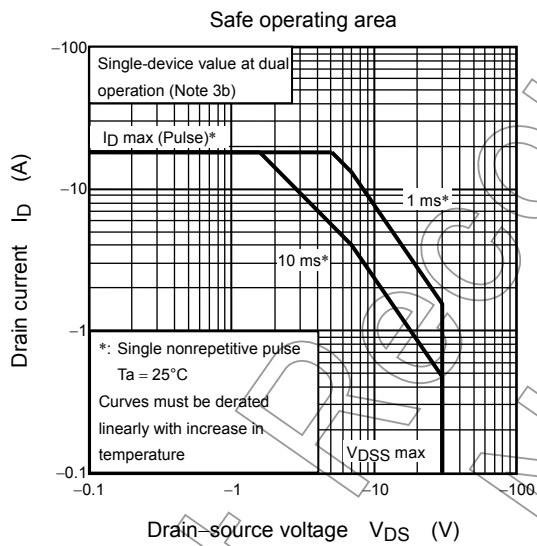
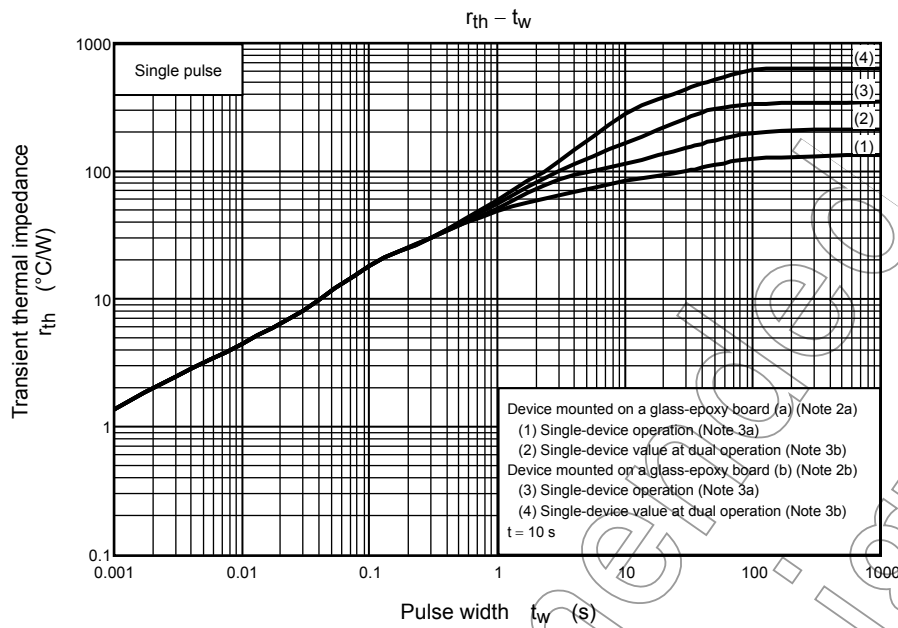
P-ch



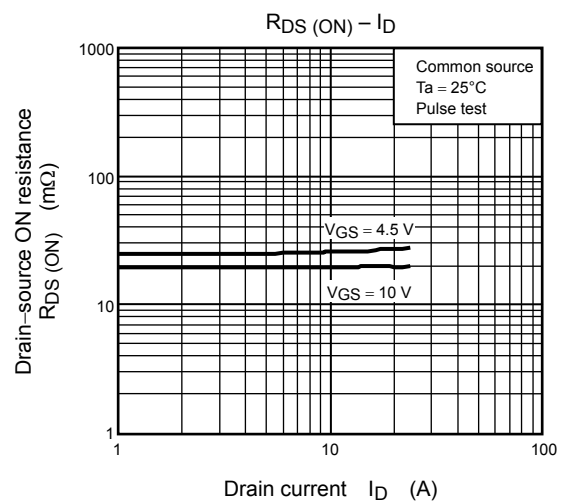
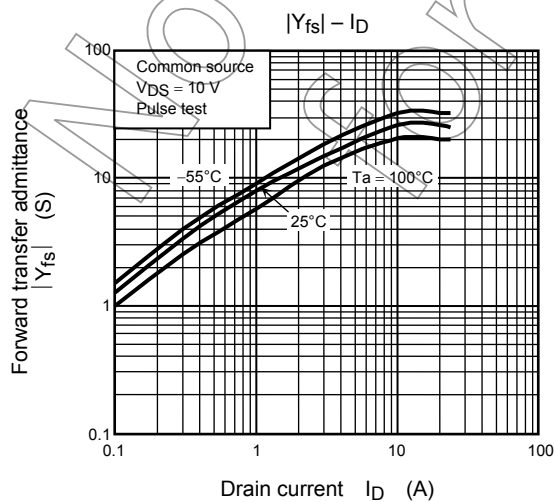
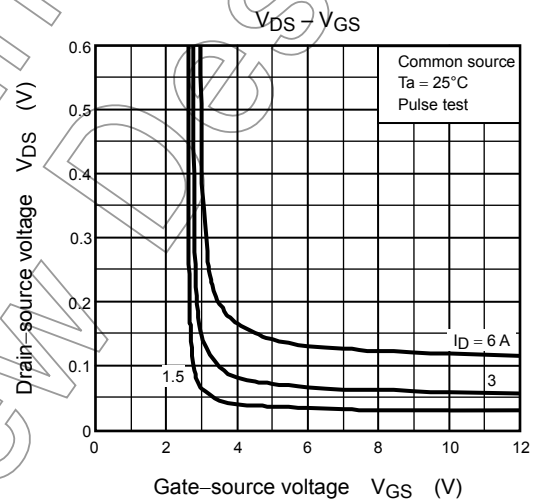
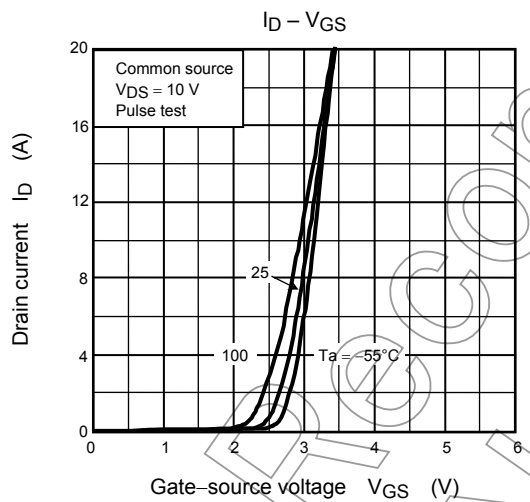
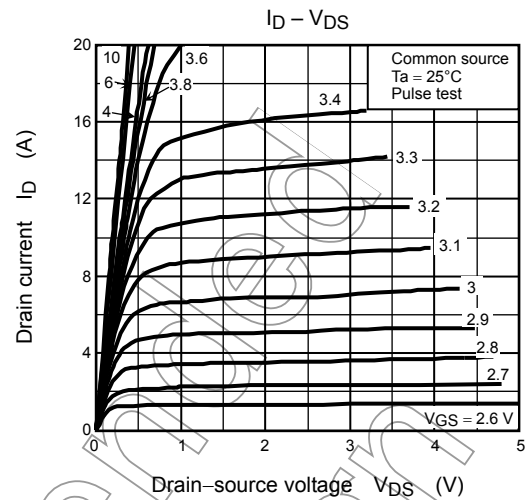
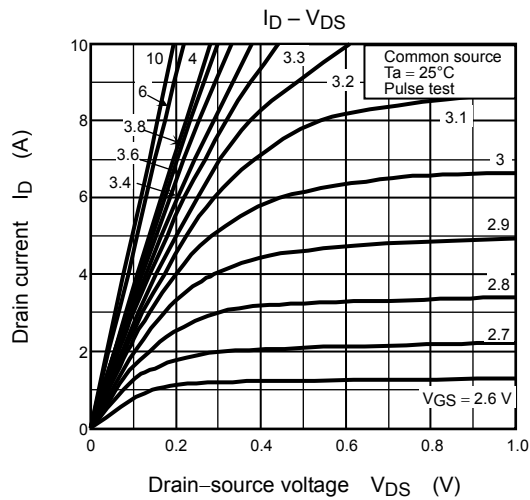
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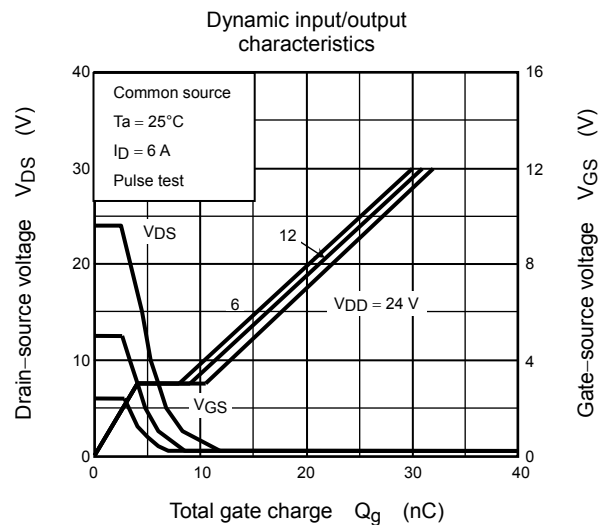
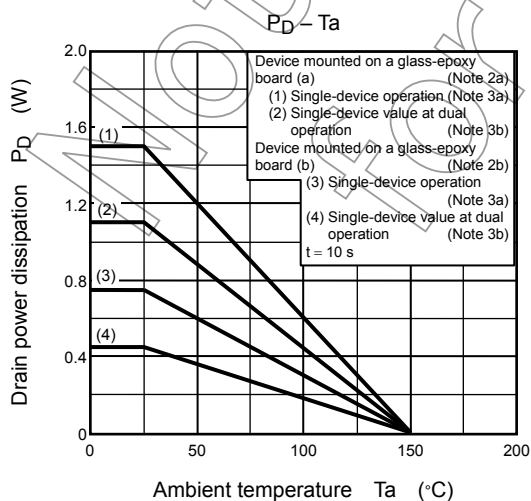
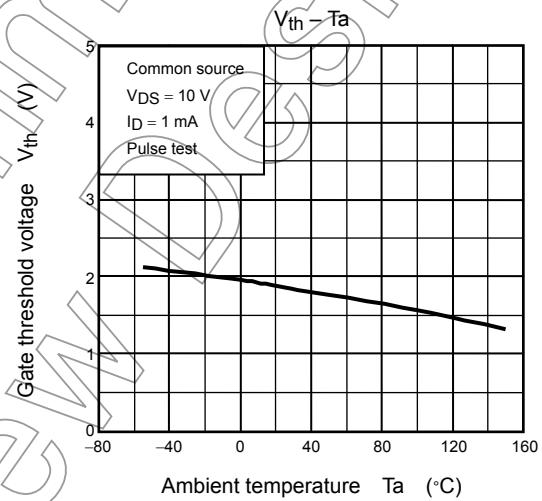
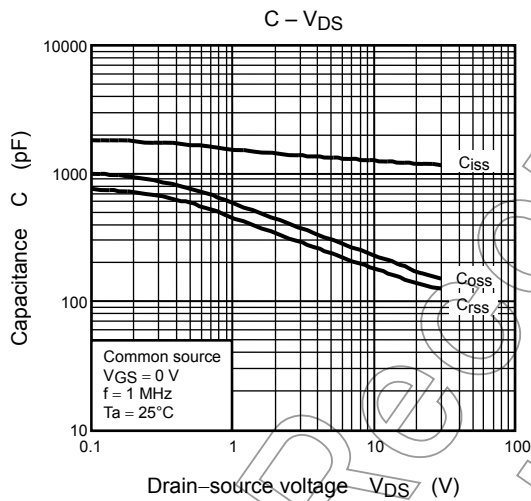
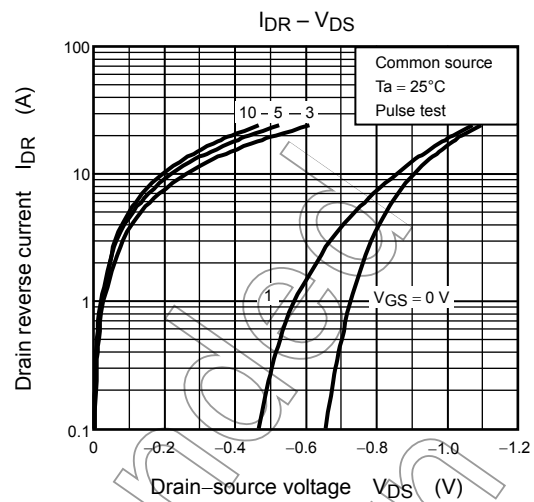
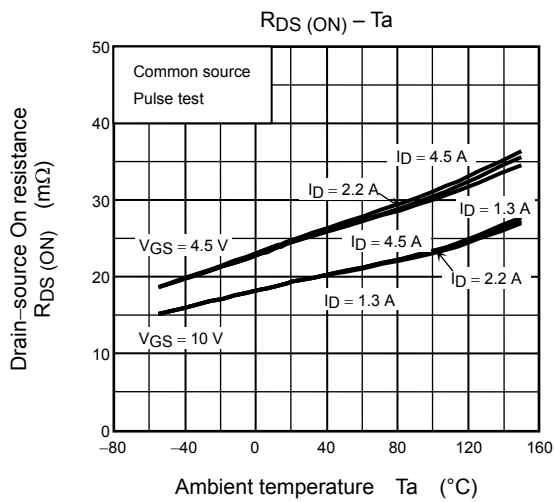
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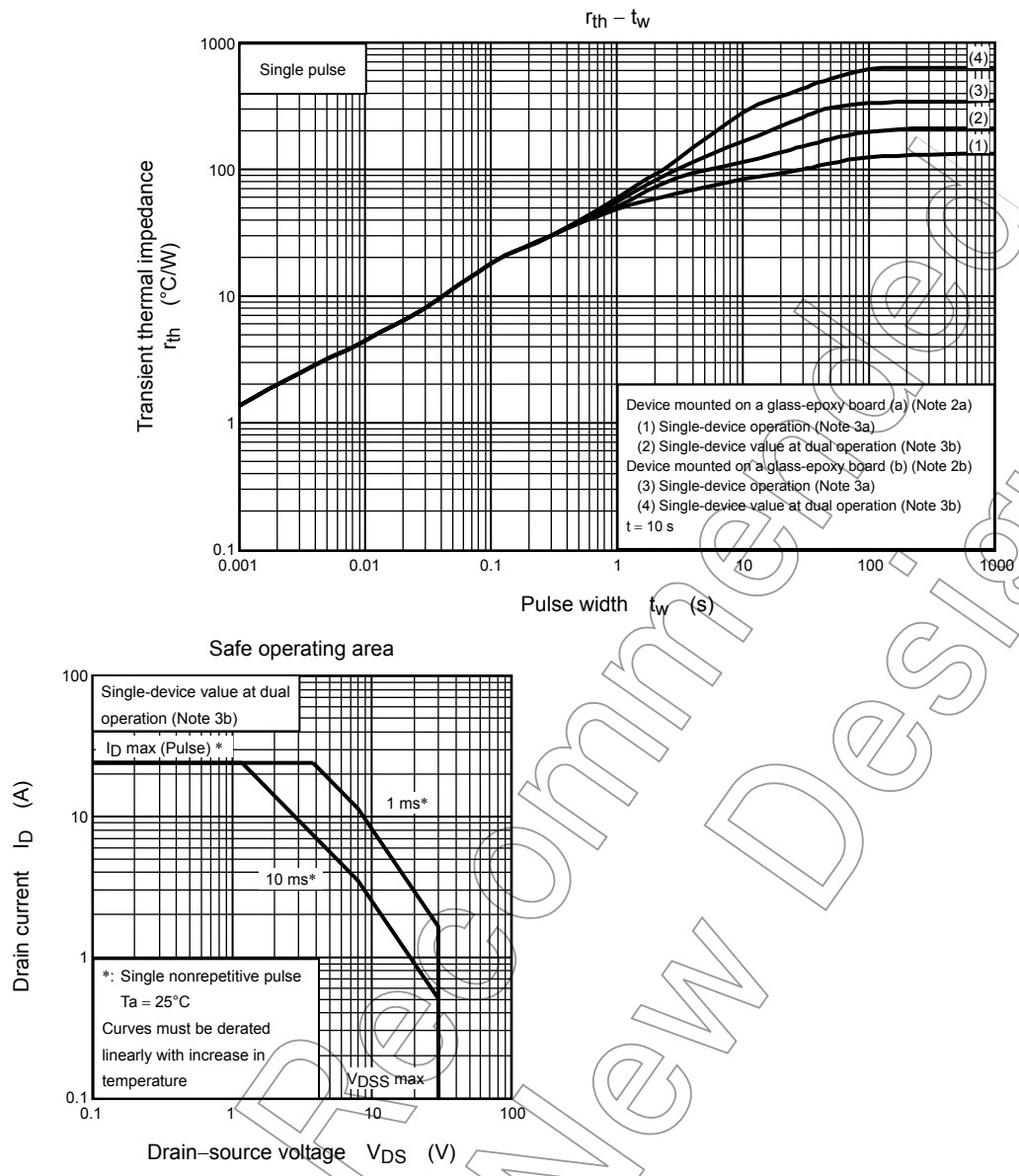
N-ch



N-ch



N-ch



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