

74LCX74FT

1. Functional Description

- Low-Voltage Dual D-Type Flip-Flop with 5-V Tolerant Inputs and Outputs

2. General

The 74LCX74FT is a high-performance CMOS D-type flip-flop. Designed for use in 3.3 V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (3.3 V) V_{CC} applications, but it could be used to interface to 5 V supply environment for inputs.

The signal level applied to the D input is transferred to Q output during the positive going transition of the CK pulse.

\overline{CLR} and \overline{PR} are independent of the CK and are accomplished by setting the appropriate input low.

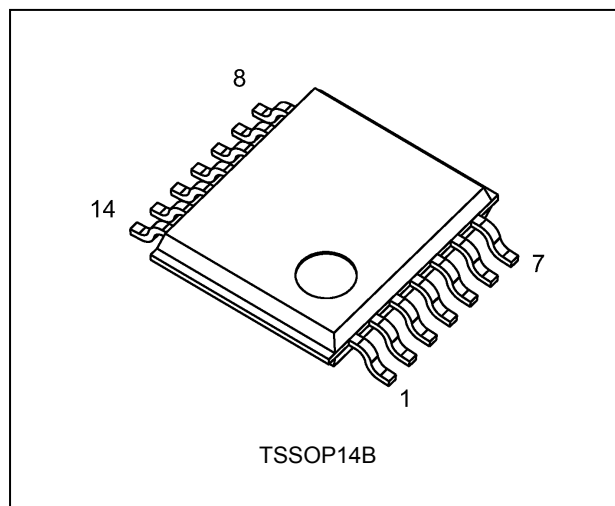
All inputs are equipped with protection circuits against static discharge.

3. Features

- (1) AEC-Q100 (Rev. H) (Note 1)
- (2) Wide operating temperature range: $T_{opr} = -40$ to $125\text{ }^{\circ}\text{C}$
- (3) Low-voltage operation: $V_{CC} = 1.65$ to 3.6 V
- (4) High-speed operation: $t_{pd} = 8.0\text{ ns}$ (max) ($V_{CC} = 3.3 \pm 0.3\text{ V}$)
- (5) Output current: $|I_{OH}|/I_{OL} = 24\text{ mA}$ (min) ($V_{CC} = 3.0\text{ V}$)
- (6) Power-down protection provided on all inputs and outputs
- (7) Pin and function compatible with the 74 series
(74LVC/ALVC/ etc.) 74 type

Note 1: This device is compliant with the reliability requirements of AEC-Q100. For details, contact your Toshiba sales representative.

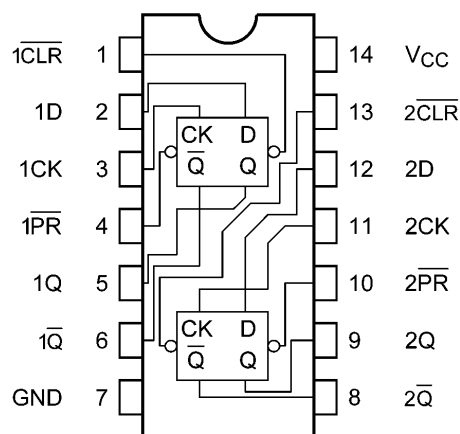
4. Packaging



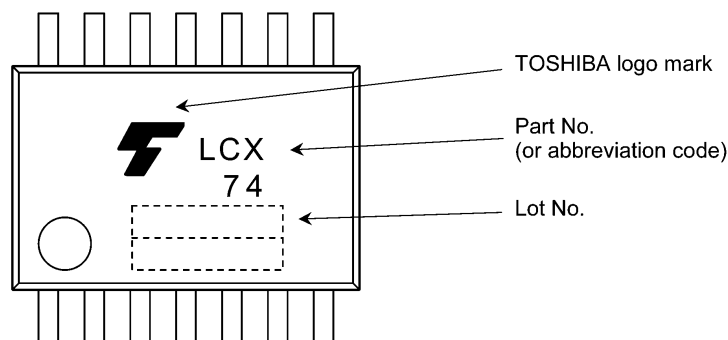
Start of commercial production

2014-06

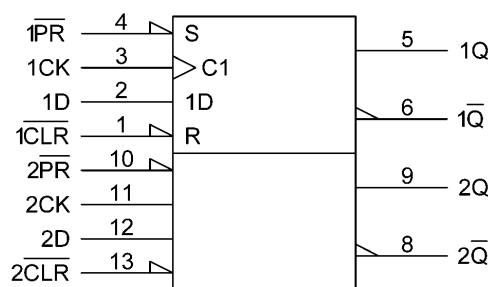
5. Pin Assignment



6. Marking



7. IEC Logic Symbol



8. Truth Table

Inputs				Outputs		Function
CLR	PR	D	CK	Q	Q̄	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	—
H	H	L	↑	L	H	—
H	H	H	↑	H	L	—
H	H	X	↓	Qn	Q̄n	No change

X: Don't care

9. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CC}		-0.5 to 6.5	V
Input voltage	V_{IN}		-0.5 to 6.5	V
Output voltage	V_{OUT}	(Note 1)	-0.5 to 6.5	V
		(Note 2)	-0.5 to $V_{CC} + 0.5$	
Input diode current	I_{IK}		-50	mA
Output diode current	I_{OK}	(Note 3)	± 50	mA
Output current	I_{OUT}		± 50	mA
Power dissipation	P_D	(Note 4)	180	mW
V_{CC} /ground current	I_{CC}/I_{GND}		± 100	mA
Storage temperature	T_{stg}		-65 to 150	$^{\circ}\text{C}$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: $V_{CC} = 0\text{ V}$

Note 2: High (H) or Low (L) state. I_{OUT} absolute maximum rating must be observed.

Note 3: $V_{OUT} < \text{GND}$, $V_{OUT} > V_{CC}$

Note 4: 180 mW in the range of $T_a = -40$ to $85\text{ }^{\circ}\text{C}$. From $T_a = 85$ to $125\text{ }^{\circ}\text{C}$ a derating factor of $-3.25\text{ mW}/^{\circ}\text{C}$ shall be applied until 50 mW.

10. Operating Ranges (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CC}		1.65 to 3.6	V
		(Note 1)	1.5 to 3.6	
Input voltage	V_{IN}		0 to 5.5	V
Output voltage	V_{OUT}	(Note 2)	0 to 5.5	V
		(Note 3)	0 to V_{CC}	
Output current	I_{OH}, I_{OL}	(Note 4)	± 24	mA
	I_{OH}, I_{OL}	(Note 5)	± 12	
Operating temperature	T_{opr}		-40 to 125	$^{\circ}\text{C}$
Input rise and fall times	dt/dv	(Note 6)	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.

Unused inputs must be tied to either V_{CC} or GND.

Note 1: Data retention only.

Note 2: $V_{CC} = 0\text{ V}$

Note 3: High or low state

Note 4: $V_{CC} = 3.0$ to 3.6 V

Note 5: $V_{CC} = 2.7$ to 3.0 V

Note 6: $V_{IN} = 0.8$ to 2.0 V , $V_{CC} = 3.0\text{ V}$

11. Electrical Characteristics

11.1. DC Characteristics (Unless otherwise specified, $T_a = -40$ to $85\text{ }^\circ\text{C}$)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
High-level input voltage	V_{IH}	—		1.65 to 2.3	$V_{CC} \times 0.9$	—	V
				2.3 to 2.7	1.7	—	
				2.7 to 3.6	2.0	—	
Low-level input voltage	V_{IL}	—		1.65 to 2.3	—	$V_{CC} \times 0.1$	V
				2.3 to 2.7	—	0.7	
				2.7 to 3.6	—	0.8	
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -100\text{ }\mu\text{A}$	1.65 to 3.6	$V_{CC} - 0.2$	—	V
			$I_{OH} = -4\text{ mA}$	1.65	1.05	—	
			$I_{OH} = -8\text{ mA}$	2.3	1.7	—	
			$I_{OH} = -12\text{ mA}$	2.7	2.2	—	
			$I_{OH} = -18\text{ mA}$	3.0	2.4	—	
			$I_{OH} = -24\text{ mA}$	3.0	2.2	—	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 100\text{ }\mu\text{A}$	1.65 to 3.6	—	0.2	V
			$I_{OL} = 4\text{ mA}$	1.65	—	0.45	
			$I_{OL} = 8\text{ mA}$	2.3	—	0.7	
			$I_{OL} = 12\text{ mA}$	2.7	—	0.4	
			$I_{OL} = 16\text{ mA}$	3.0	—	0.4	
			$I_{OL} = 24\text{ mA}$	3.0	—	0.55	
Input leakage current	I_{IN}	$V_{IN} = 0$ to 5.5 V		1.65 to 3.6	—	± 5.0	μA
Power-OFF leakage current	I_{OFF}	$V_{IN}/V_{OUT} = 5.5\text{ V}$		0	—	10.0	μA
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND		1.65 to 3.6	—	10.0	μA
	I_{CC}	$V_{IN} = 3.6$ to 5.5 V		1.65 to 3.6	—	± 10.0	
Quiescent supply current	ΔI_{CC}	$V_{IH} = V_{CC} - 0.6\text{ V}$ (per 1 input)		2.7 to 3.6	—	500	μA

11.2. DC Characteristics (Unless otherwise specified, $T_a = -40$ to $125\text{ }^\circ\text{C}$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit
High-level input voltage	V_{IH}	—	1.65 to 2.3	$V_{CC} \times 0.9$	—	V
			2.3 to 2.7	1.7	—	
			2.7 to 3.6	2.0	—	
Low-level input voltage	V_{IL}	—	1.65 to 2.3	—	$V_{CC} \times 0.1$	V
			2.3 to 2.7	—	0.7	
			2.7 to 3.6	—	0.8	
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -100\text{ }\mu\text{A}$	1.65 to 3.6	$V_{CC} - 0.2$	V
			$I_{OH} = -4\text{ mA}$	1.65	0.9	
			$I_{OH} = -8\text{ mA}$	2.3	1.55	
			$I_{OH} = -12\text{ mA}$	2.7	2.0	
			$I_{OH} = -18\text{ mA}$	3.0	2.2	
			$I_{OH} = -24\text{ mA}$	3.0	2.0	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 100\text{ }\mu\text{A}$	1.65 to 3.6	—	V
			$I_{OL} = 4\text{ mA}$	1.65	—	
			$I_{OL} = 8\text{ mA}$	2.3	—	
			$I_{OL} = 12\text{ mA}$	2.7	—	
			$I_{OL} = 16\text{ mA}$	3.0	—	
			$I_{OL} = 24\text{ mA}$	3.0	—	
Input leakage current	I_{IN}	$V_{IN} = 0$ to 5.5 V	1.65 to 3.6	—	± 20.0	μA
Power-OFF leakage current	I_{OFF}	$V_{IN}/V_{OUT} = 5.5\text{ V}$	0	—	40.0	μA
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND	1.65 to 3.6	—	40.0	μA
	I_{CC}	$V_{IN} = 3.6$ to 5.5 V	1.65 to 3.6	—	± 40.0	
Quiescent supply current	ΔI_{CC}	$V_{IH} = V_{CC} - 0.6\text{ V}$ (per 1 input)	2.7 to 3.6	—	5.0	mA

11.3. AC Characteristics (Unless otherwise specified, $T_a = -40$ to $85\text{ }^\circ\text{C}$)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	Min	Max	Unit
Maximum clock frequency	f_{MAX}		See 11.7 AC Test Circuit, Table 11.8.1, Fig. 11.8.1	1.8 ± 0.15	50	—	MHz
				2.5 ± 0.2	100	—	
				2.7	100	—	
				3.3 ± 0.3	150	—	
Propagation delay time (CK-Q, \bar{Q})	t_{PLH}, t_{PHL}		See 11.7 AC Test Circuit, Table 11.8.1, Fig. 11.8.1	1.8 ± 0.15	—	22.0	ns
				2.5 ± 0.2	—	9.0	
				2.7	—	8.0	
				3.3 ± 0.3	1.5	7.0	
Propagation delay time (CLR, PR-Q, \bar{Q})	t_{PLH}, t_{PHL}		See 11.7 AC Test Circuit, Table 11.8.1, Fig. 11.8.3	1.8 ± 0.15	—	22.0	ns
				2.5 ± 0.2	—	9.0	
				2.7	—	8.0	
				3.3 ± 0.3	1.5	7.0	
Minimum pulse width (CK)	$t_{w(L)}, t_{w(H)}$		See 11.7 AC Test Circuit, Table 11.8.1, Fig. 11.8.1	1.8 ± 0.15	10.0	—	ns
				2.5 ± 0.2	5.0	—	
				2.7	3.3	—	
				3.3 ± 0.3	3.3	—	
Minimum pulse width (CLR, PR)	$t_{w(L)}$		See 11.7 AC Test Circuit, Table 11.8.1, Fig. 11.8.3	1.8 ± 0.15	10.0	—	ns
				2.5 ± 0.2	5.0	—	
				2.7	3.6	—	
				3.3 ± 0.3	3.3	—	
Minimum setup time	t_s		See 11.7 AC Test Circuit, Table 11.8.1, Fig. 11.8.1	1.8 ± 0.15	10.0	—	ns
				2.5 ± 0.2	5.0	—	
				2.7	2.5	—	
				3.3 ± 0.3	2.5	—	
Minimum hold time	t_h		See 11.7 AC Test Circuit, Table 11.8.1, Fig. 11.8.1	1.8 ± 0.15	1.5	—	ns
				2.5 ± 0.2	1.5	—	
				2.7	1.5	—	
				3.3 ± 0.3	1.5	—	
Minimum removal time	t_{rem}		See 11.7 AC Test Circuit, Table 11.8.1, Fig. 11.8.2	1.8 ± 0.15	10.0	—	ns
				2.5 ± 0.2	5.0	—	
				2.7	3.0	—	
				3.3 ± 0.3	2.5	—	
Output skew	t_{osLH}, t_{osHL}	(Note 1)	—	2.7	—	—	ns
				3.3 ± 0.3	—	1.0	

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLHm} - t_{PLHn}|$, $t_{osHL} = |t_{PHLm} - t_{PHLn}|$)

11.4. AC Characteristics (Unless otherwise specified, $T_a = -40$ to $125\text{ }^{\circ}\text{C}$)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	Min	Max	Unit
Maximum clock frequency	f_{MAX}		See 11.7 AC Test Circuit, Table 11.8.1, Fig. 11.8.1	1.8 ± 0.15	45.0	—	MHz
				2.5 ± 0.2	90.0	—	
				2.7	90.0	—	
				3.3 ± 0.3	135.0	—	
Propagation delay time (CK-Q, \bar{Q})	t_{PLH}, t_{PHL}		See 11.7 AC Test Circuit, Table 11.8.1, Fig. 11.8.1	1.8 ± 0.15	—	24.5	ns
				2.5 ± 0.2	—	10.0	
				2.7	—	9.0	
				3.3 ± 0.3	1.5	8.0	
Propagation delay time (CLR, PR-Q, \bar{Q})	t_{PLH}, t_{PHL}		See 11.7 AC Test Circuit, Table 11.8.1, Fig. 11.8.3	1.8 ± 0.15	—	24.5	ns
				2.5 ± 0.2	—	10.0	
				2.7	—	9.0	
				3.3 ± 0.3	1.5	8.0	
Minimum pulse width (CK)	$t_{w(L)}, t_{w(H)}$		See 11.7 AC Test Circuit, Table 11.8.1, Fig. 11.8.1	1.8 ± 0.15	10.0	—	ns
				2.5 ± 0.2	5.0	—	
				2.7	3.3	—	
				3.3 ± 0.3	3.3	—	
Minimum pulse width (CLR, PR)	$t_{w(L)}$		See 11.7 AC Test Circuit, Table 11.8.1, Fig. 11.8.3	1.8 ± 0.15	10.0	—	ns
				2.5 ± 0.2	5.0	—	
				2.7	3.6	—	
				3.3 ± 0.3	3.3	—	
Minimum setup time	t_s		See 11.7 AC Test Circuit, Table 11.8.1, Fig. 11.8.1	1.8 ± 0.15	10.0	—	ns
				2.5 ± 0.2	5.0	—	
				2.7	2.5	—	
				3.3 ± 0.3	2.5	—	
Minimum hold time	t_h		See 11.7 AC Test Circuit, Table 11.8.1, Fig. 11.8.1	1.8 ± 0.15	1.5	—	ns
				2.5 ± 0.2	1.5	—	
				2.7	1.5	—	
				3.3 ± 0.3	1.5	—	
Minimum removal time	t_{rem}		See 11.7 AC Test Circuit, Table 11.8.1, Fig. 11.8.2	1.8 ± 0.15	10.0	—	ns
				2.5 ± 0.2	5.0	—	
				2.7	3.0	—	
				3.3 ± 0.3	2.5	—	
Output skew	t_{osLH}, t_{osHL}	(Note 1)	—	2.7	—	—	ns
				3.3 ± 0.3	—	1.0	

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLHm} - t_{PLHn}|$, $t_{osHL} = |t_{PHLm} - t_{PHLn}|$)

11.5. Dynamic Switching Characteristics (Unless otherwise specified, $T_a = 25\text{ }^{\circ}\text{C}$, Input: $t_r = t_f = 2.5\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 500\text{ }\Omega$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Quiet output maximum dynamic V_{OL}	V_{OLP}	$V_{IH} = 3.3\text{ V}$, $V_{IL} = 0\text{ V}$	3.3	0.8	V
Quiet output minimum dynamic V_{OL}	$ V_{OLV} $	$V_{IH} = 3.3\text{ V}$, $V_{IL} = 0\text{ V}$	3.3	0.8	V

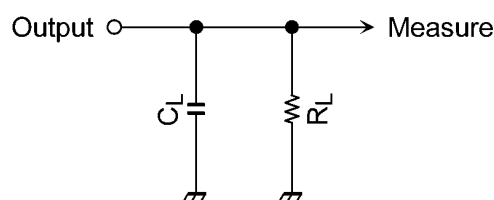
11.6. Capacitive Characteristics (Unless otherwise specified, $T_a = 25\text{ }^{\circ}\text{C}$)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	Typ.	Unit
Input capacitance	C_{IN}		—	3.3	7	pF
Output capacitance	C_{OUT}		—	0	8	pF
Power dissipation capacitance	C_{PD}	(Note 1)	$f_{IN} = 10\text{ MHz}$	3.3	25	pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$$I_{CC}(\text{opr}) = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/2 \text{ (per 1 bit)}$$

11.7. AC Test Circuit



11.8. AC Waveform

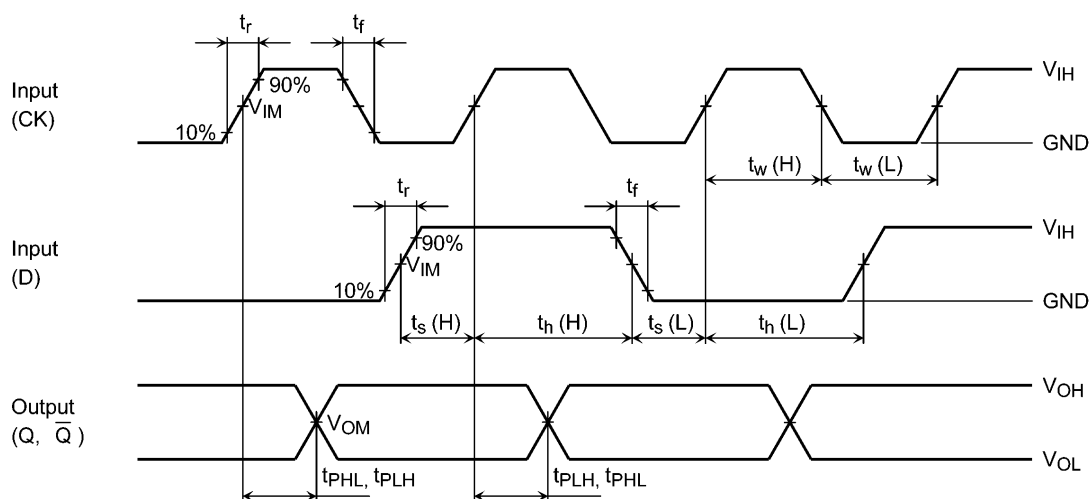


Fig. 11.8.1 t_{PLH} , t_{PHL} , t_w , t_s , t_h

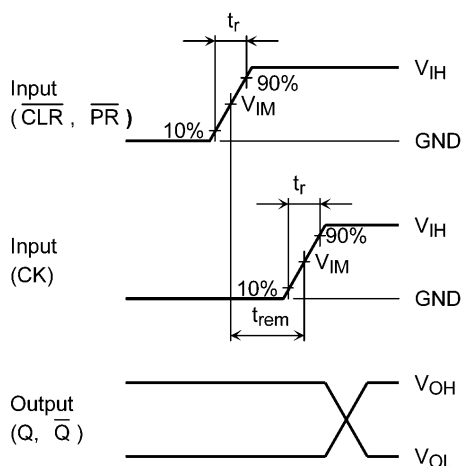


Fig. 11.8.2 t_{rem}

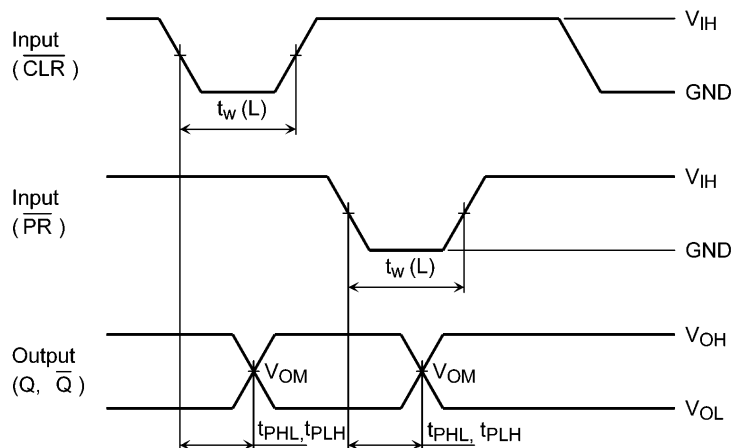


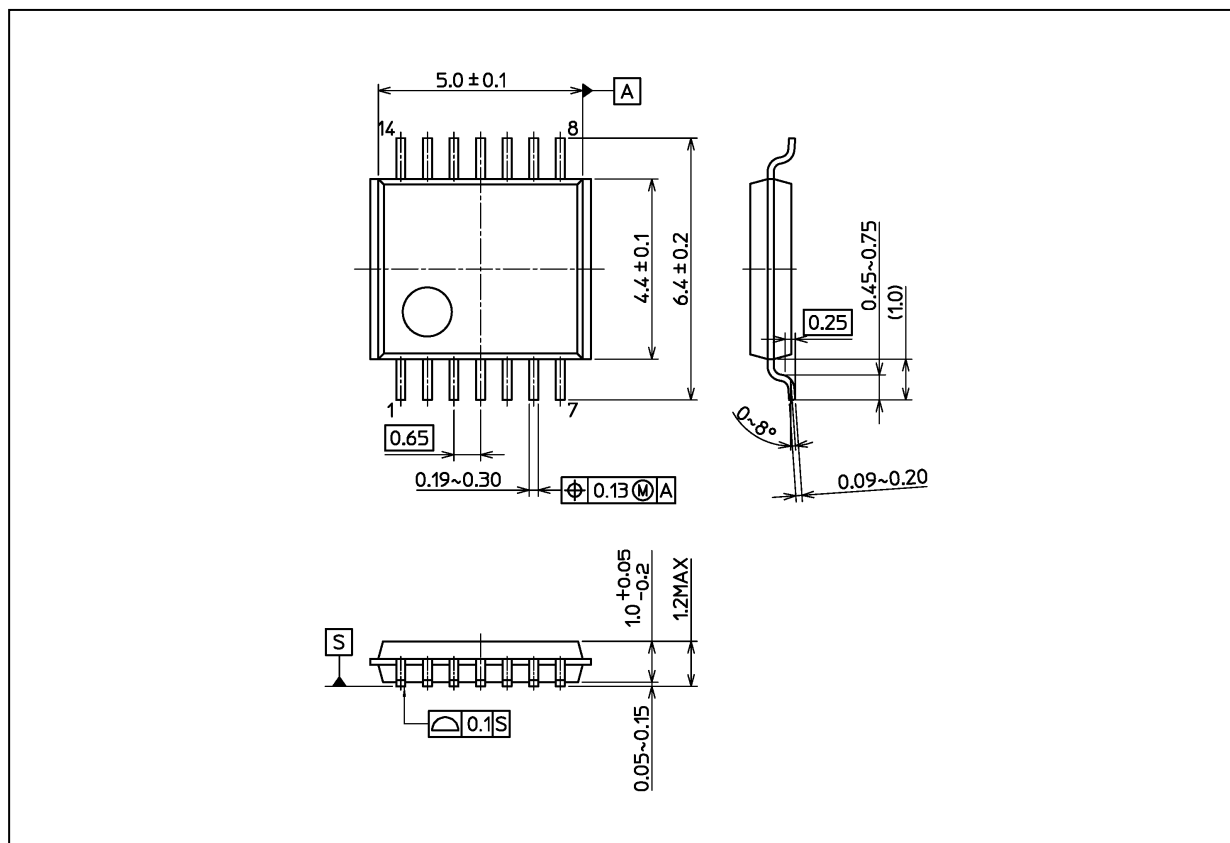
Fig. 11.8.3 t_{PLH} , t_{PHL}

Table 11.8.1 AC Waveform Symbols

	Symbol	$V_{CC} = 3.3 \pm 0.3 \text{ V}$ $V_{CC} = 2.7 \text{ V}$	$V_{CC} = 2.5 \pm 0.2 \text{ V}$	$V_{CC} = 1.8 \pm 0.15 \text{ V}$
Input	V_{IH}	2.7 V	V_{CC}	V_{CC}
	V_{IM}	1.5 V	$V_{CC}/2$	$V_{CC}/2$
	t_r, t_f	2.5 ns	2.0 ns	2.0 ns
Output	V_{OM}	1.5 V	$V_{OH}/2$	$V_{OH}/2$
Load	C_L	50 pF	30 pF	30 pF
	R_L	500 Ω	500 Ω	1 k Ω

Package Dimensions

Unit: mm



Weight: 0.054 g (typ.)

Package Name(s)
Nickname: TSSOP14B

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