Unit: mm

TOSHIBA Diode Silicon Epitaxial Planar Type

1SS362FV

Ultra-High-Speed Switching Applications

Small package

Excellent in forward current and forward voltage characteristics: V_{F (3)} = 0.97 V (typ.)
 Fast reverse recovery time: t_{rr} = 1.6 ns (typ.)

Small total capacitance: C_T = 0.9 pF (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Maximum (peak) reverse voltage	V_{RM}	85	V
Reverse voltage	V _R	80	V
Maximum (peak) forward current	I _{FM}	300 *	mA
Average forward current	Io	100 *	mA
Surge current (10 ms)	I _{FSM}	1 *	Α
Power dissipation	Р	150 **	mW
Junction temperature	Tj	150	°C
Storage temperature range	T _{stg}	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

1.2±0.05 0.8±0.05 0.8±0.05 0.00+2.0 1.ANODE1 2.CATHODE2 3.CATHODE1 ANODE2 JEDEC —

JEITA —

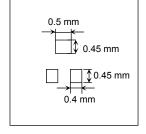
TOSHIBA 1-1Q1A

Weight: 1.5 mg (typ.)

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

*: Unit rating. Total rating = unit rating × 0.7

**: Mounted on an FR4 board (25.4 mm \times 25.4 mm \times 1.6 mm (t))

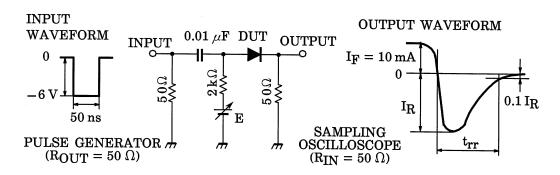


Electrical Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Тур.	Max	Unit
Forward voltage	V _{F (1)}	_	I _F = 1 mA	ı	0.63	-	
	V _{F (2)}	_	I _F = 10 mA		0.75	1	V
	V _{F (3)}	_	I _F = 100 mA	_	0.97	1.20	
Reverse current	I _{R (1)}	_	V _R = 30 V	_	_	0.1	
	I _{R (2)}	_	V _R = 80 V	_	_	0.5	μΑ
Total capacitance	C _T	_	V _R = 0 V, f = 1 MHz	_	0.9	-	pF
Reverse recovery time	t _{rr}	_	I _F = 10 mA (Fig. 1)	_	1.6	4.0	ns

Start of commercial production 2004-09

Fig. 1 Reverse Recovery Time (trr) Test Circuit

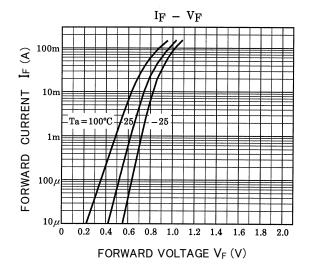


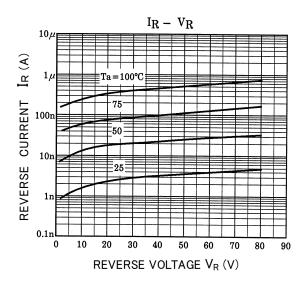
Marking

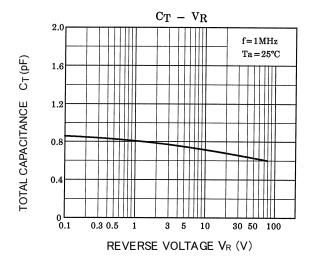
Equivalent Circuit (Top View)

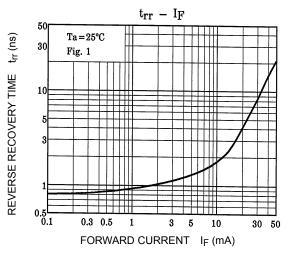












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