ESD Protection Diodes Silicon Epitaxial Planar

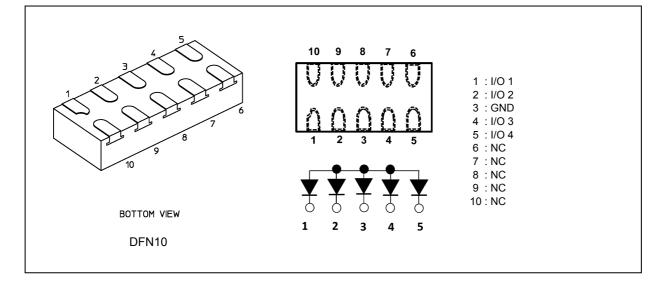
# DF10G6M4N

#### 1. Applications

ESD Protection

Note: This product is designed for protection against electrostatic discharge (ESD) and is not intended for any other purpose, including, but not limited to, voltage regulation.

#### 2. Packaging and Internal Circuit



#### 3. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25$ °C)

Characteristics	Symbol	Note	Rating	Unit
Electrostatic discharge voltage (IEC61000-4-2)(Contact)	V <sub>ESD</sub>	(Note 1)	±20	kV
Electrostatic discharge voltage (IEC61000-4-2)(Air)			±20	
Peak pulse power (tp = 8/20 μs)	P <sub>PK</sub>		30	W
Peak pulse current (tp = 8/20 μs)	I <sub>PP</sub>	(Note 2)	2	А
Junction temperature	Tj		150	°C
Storage temperature	T <sub>stg</sub>		-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: According to IEC61000-4-5.

Note 1: According to IEC61000-4-2.

#### 4. Electrical Characteristics (Unless otherwise specified, T<sub>a</sub> = 25 °C)

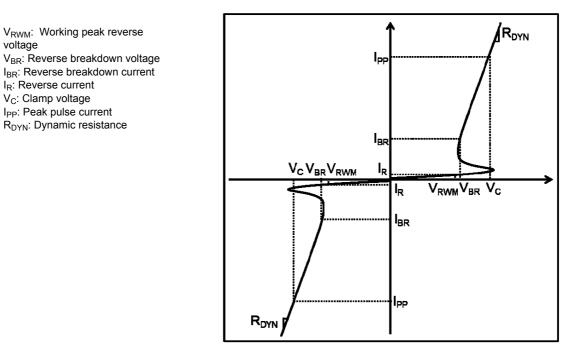


Fig. 4.1 Definitions of Electrical Characteristics

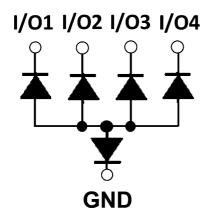
Characteristics	Symbol	Note	Test Condition	Min	Тур.	Max	Unit
Working peak reverse voltage	V <sub>RWM</sub>			_	_	5.5	V
Reverse breakdown voltage	V <sub>BR</sub>		I <sub>BR</sub> = 1 mA	5.6	6.2	8	V
Reverse current	I <sub>R</sub>		V <sub>RWM</sub> = 5.5 V	_	_	0.1	μA
Clamp voltage	V <sub>C</sub>	(Note 1)	I <sub>PP</sub> = 1 A	_	8.5	_	V
			I <sub>PP</sub> = 2 A	_	10	15	
Clamp voltage	V <sub>C</sub>	(Note 2)	I <sub>TLP</sub> = 16 A	_	18	_	V
			I <sub>TLP</sub> = 30 A	_	25	_	
Dynamic resistance	R <sub>DYN</sub>	(Note 2)	—	_	0.5	_	Ω
Total capacitance	Ct	(Note 3)	V <sub>R</sub> = 0 V, f = 1 MHz	_	0.2	0.3	pF

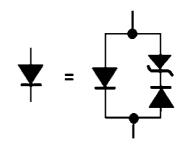
Note 1: Based on IEC61000-4-5 8/20  $\mu s$  pulse.

Note 2: TLP parameter: Z0 = 50  $\Omega$ , tp = 100 ns, tr = 300 ps, averaging window: t1 = 30 ns to t2 = 60 ns,

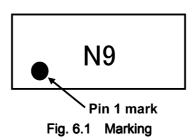
extraction of dynamic resistance using a least-squares fit of TLP characteristics at  $I_{PP}$  between 8 A to 16 A. Note 3: Guaranteed by design.

5. Equivalent Circuit





6. Marking



Marking Code	Part Number
N9	DF10G6M4N

7. Land Pattern Dimensions (for reference only)

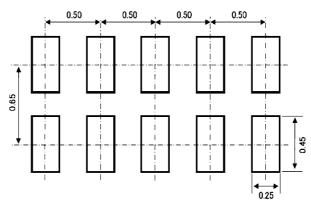
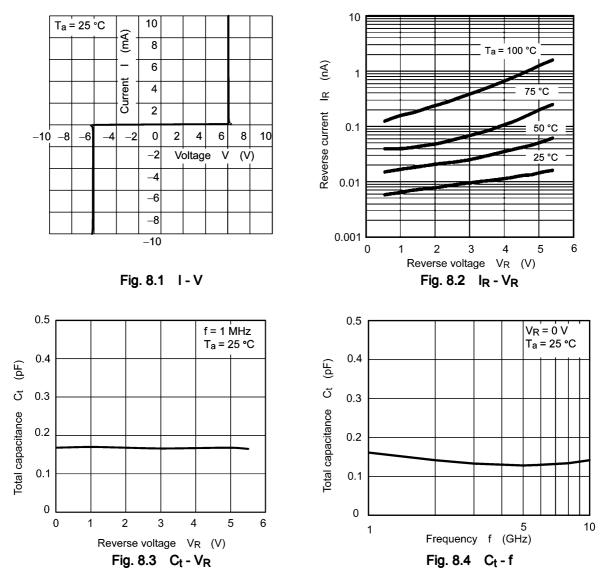


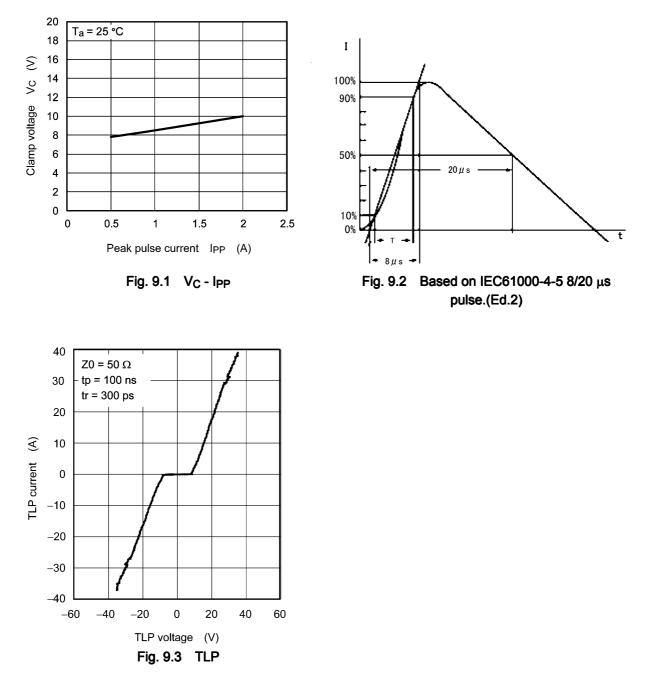
Fig. 7.1 Land Pattern Dimensions (Unit: mm)

### 8. Characteristics Curves (Note)



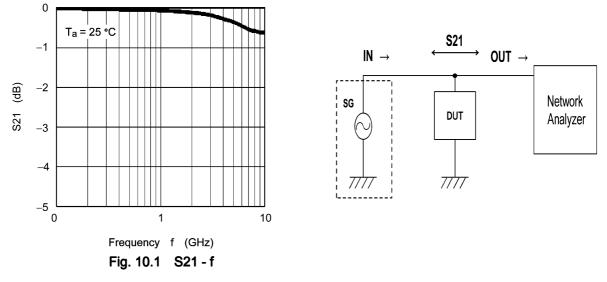
Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

### 9. Clamp Voltage V<sub>C</sub> - Peak Pulse Current (I<sub>PP</sub>) (Note)



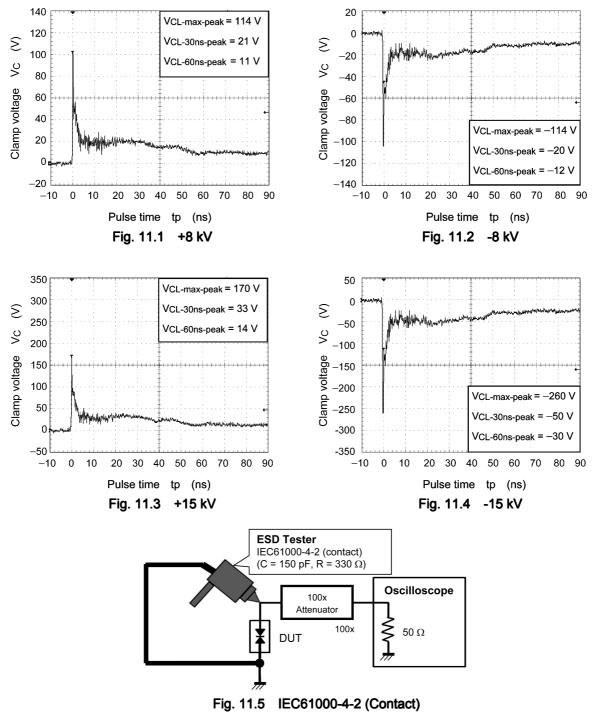
Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

### 10. Insertion Loss (S21) (Note)



Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

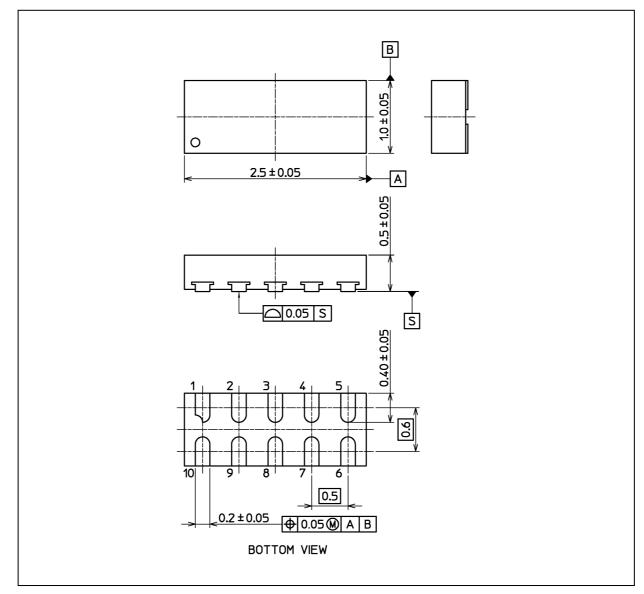
#### 11. ESD Clamp Waveform (Note)



Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

#### Package Dimensions

Unit: mm



Weight: 0.0032 g (typ.)

Package Name(s)			
TOSHIBA: 1-3V1A			
Nickname: DFN10			

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