Unit: mm

TOSHIBA Diode Silicon Epitaxial Planar Type

# **1SS361**

## **Ultra High Speed Switching Application**

• Small package

Low forward voltage : V<sub>F</sub> = 0.9V (typ.)
 Fast reverse recovery time: t<sub>rr</sub> = 1.6ns (typ.)
 Small total capacitance : C<sub>T</sub> = 0.9pF (typ.)

## Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Maximum (peak) reverse voltage	$V_{RM}$	85	V
Reverse voltage	V <sub>R</sub>	80	<b>V</b>
Maximum (peak) forward current	I <sub>FM</sub>	300 *	mA
Average forward current	IO	100 *	mA
Surge current (10ms)	I <sub>FSM</sub>	2 *	Α
Power dissipation	Р	100	mW
Junction temperature	Tj	125	°C
Storage temperature	T <sub>stg</sub>	-55 to 125	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the

reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

# Electrical Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Тур.	Max	Unit
Forward voltage	V <sub>F (1)</sub>	_	I <sub>F</sub> = 1mA	_	0.60	_	٧
	V <sub>F (2)</sub>	_	I <sub>F</sub> = 10mA	_	0.72	_	
	V <sub>F (3)</sub>	_	I <sub>F</sub> = 100mA	_	0.90	1.20	
Reverse current	I <sub>R (1)</sub>	_	V <sub>R</sub> = 30V	_	_	0.1	μА
	I <sub>R (2)</sub>	_	V <sub>R</sub> = 80V	_	_	0.5	
Total capacitance	C <sub>T</sub>	_	V <sub>R</sub> = 0, f = 1MH <sub>z</sub>	_	0.9	3.0	pF
Reverse recovery time	t <sub>rr</sub>	_	I <sub>F</sub> = 10mA, Fig.1	_	1.6	4.0	ns

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1-2S1B

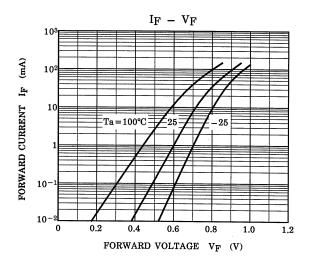
Weight: 2.4mg (typ.)

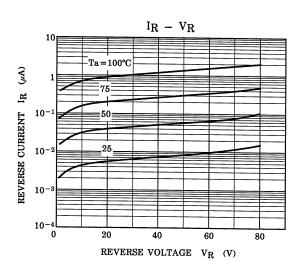
TOSHIBA

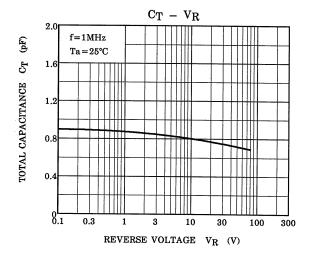
<sup>\*</sup> Unit rating. Total rating = unit rating × 1.5

### Marking









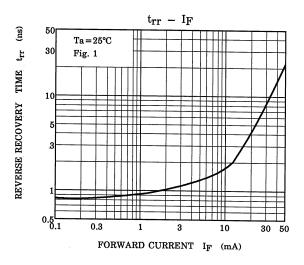
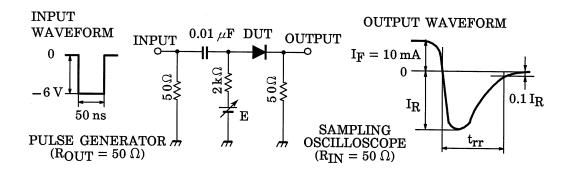


Fig.1 Reverse Recovery Time (t<sub>rr</sub>) Test Circuit



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