

TOSHIBA Diodes for Protecting against ESD

# DF5A3.6CFU

Product for Use Only as Protection against Electrostatic Discharge (ESD)

\* This product is for protection against electrostatic discharge (ESD) only and is not intended for any other usage, including without limitation, the constant voltage diode application.

- The mounting of four devices on an ultra-compact package allows the number of parts and the mounting cost to be reduced.
- Low terminal capacitance :  $C_T = 52 \text{ pF}$  (typ.)

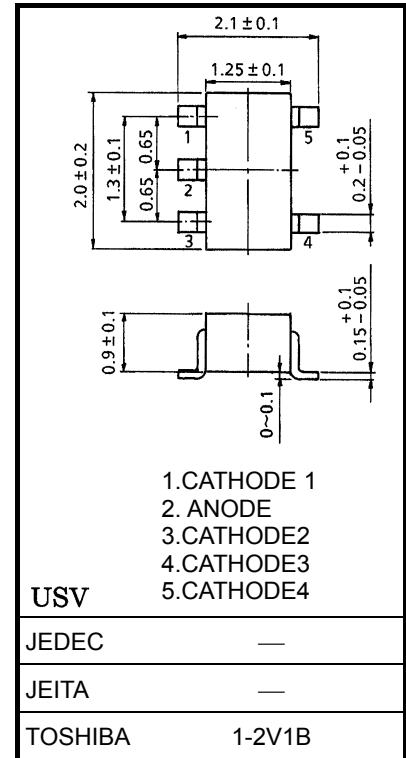
### Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Power dissipation	P	200	mW
Junction temperature	T <sub>j</sub>	150	°C
Storage temperature range	T <sub>stg</sub>	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Unit: mm



Weight: 0.0062 g (typ.)

### Electrical Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Zener voltage	V <sub>Z</sub>	I <sub>Z</sub> = 5 mA	3.4	3.6	3.8	V
Dynamic impedance	Z <sub>Z</sub>	I <sub>Z</sub> = 5 mA	—	—	130	Ω
Reverse current	I <sub>R</sub>	V <sub>R</sub> = 1.8 V	—	—	100	μA
Terminal capacitance (between Cathode and Anode)	C <sub>T</sub>	V <sub>R</sub> = 0 V, f = 1 MHz	—	52	—	pF

### Guaranteed Level of ESD Immunity

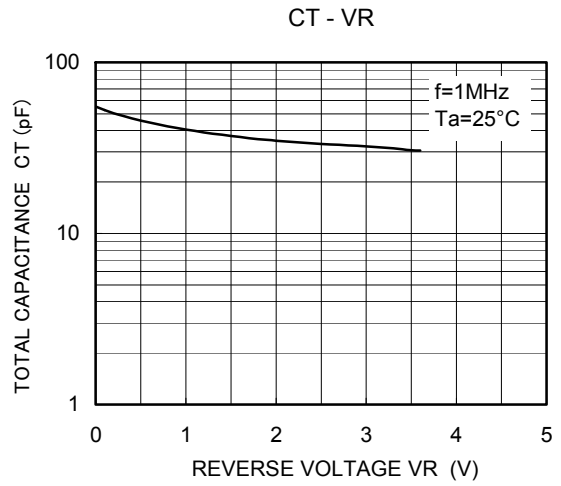
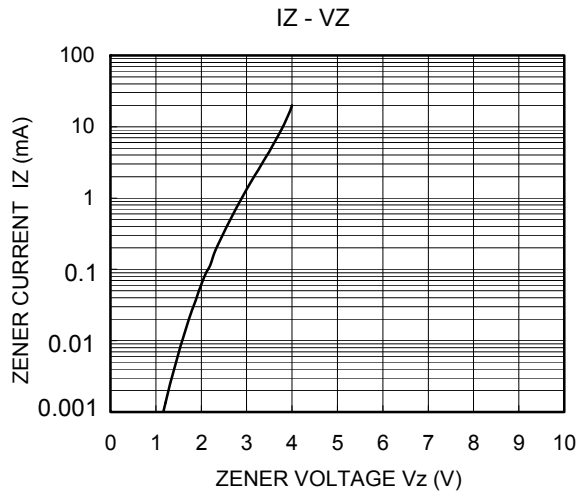
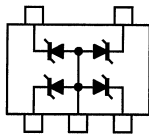
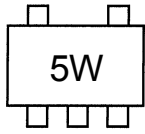
Test Condition	ESD Immunity Level
IEC61000-4-2 (Contact discharge)	± 15 kV

Criterion: No damage to device elements

Start of commercial production  
2003-06

**Marking**

**Equivalent Circuit (Top View)**



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