

# SSM3K7002KFU

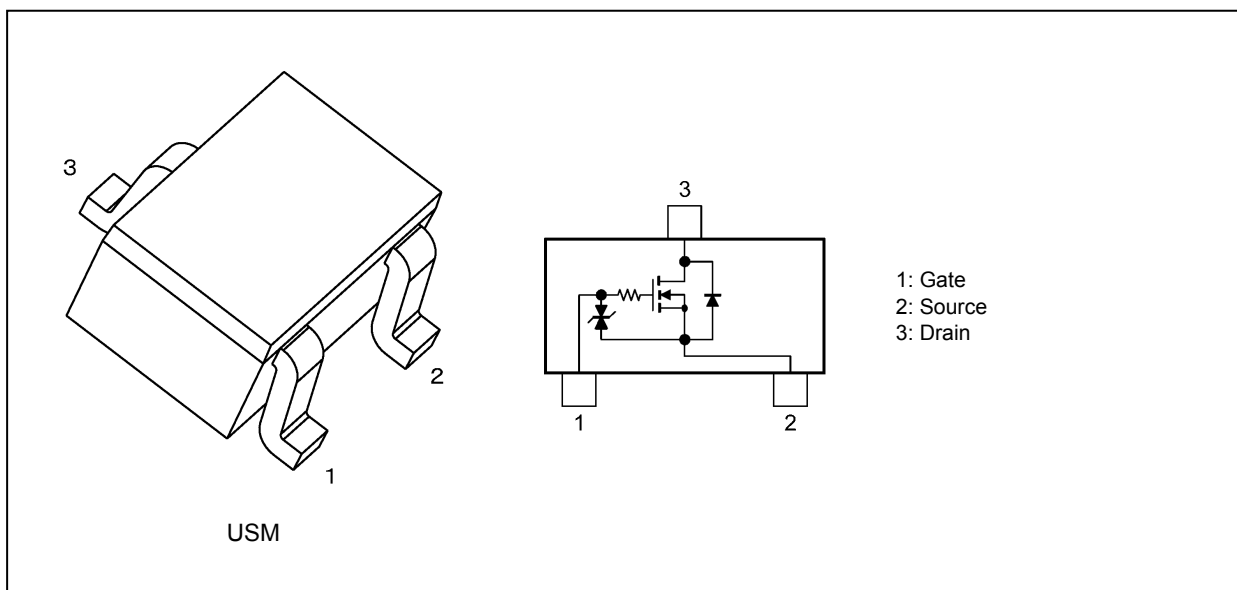
## 1. Applications

- High-Speed Switching

## 2. Features

- (1) ESD(HBM) level 2 kV
- (2) Low drain-source on-resistance
  - :  $R_{DS(ON)} = 1.05 \Omega$  (typ.) (@ $V_{GS} = 10 \text{ V}$ )
  - $R_{DS(ON)} = 1.15 \Omega$  (typ.) (@ $V_{GS} = 5.0 \text{ V}$ )
  - $R_{DS(ON)} = 1.2 \Omega$  (typ.) (@ $V_{GS} = 4.5 \text{ V}$ )

## 3. Packaging and Internal Circuit



Start of commercial production

2016-01

#### 4. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Rating	Unit
Drain-source voltage	$V_{DSS}$	60	V
Gate-source voltage	$V_{GSS}$	$\pm 20$	
Drain current (DC) (Note 1)	$I_D$	400	mA
Drain current (pulsed) (Note 1), (Note 2)	$I_{DP}$	1200	
Power dissipation (Note 3)	$P_D$	150	mW
Power dissipation (Note 4)		700	
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Ensure that the channel temperature does not exceed  $150\text{ }^\circ\text{C}$ .

Note 2: pulse width  $\leq 10\text{ }\mu\text{s}$ , Duty  $\leq 1\%$

Note 3: Device mounted on a  $25.4\text{ mm} \times 25.4\text{ mm} \times 1.6\text{ mm}$  FR4 glass epoxy board (Cu pad:  $0.6\text{ mm}^2 \times 3$ )

Note 4: Device mounted on a  $25.4\text{ mm} \times 25.4\text{ mm} \times 1.6\text{ mm}$  FR4 glass epoxy board (Cu pad:  $645\text{ mm}^2$ )

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.

Note: The channel-to-ambient thermal resistance,  $R_{th(ch-a)}$ , and the drain power dissipation,  $P_D$ , vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.

**5. Electrical Characteristics**

**5.1. Static Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 16\text{ V}$	—	—	$\pm 10$	$\mu\text{A}$
Drain cut-off current	$I_{DSS}$	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	—	—	1	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	60	—	—	V
Gate threshold voltage	$V_{th}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.1	—	2.1	
Drain-source on-resistance (Note 1)	$R_{DS(ON)}$	$I_D = 100\text{ mA}, V_{GS} = 4.5\text{ V}$	—	1.2	1.75	$\Omega$
		$I_D = 100\text{ mA}, V_{GS} = 5.0\text{ V}$	—	1.15	1.65	
		$I_D = 100\text{ mA}, V_{GS} = 10\text{ V}$	—	1.05	1.5	
Forward transfer admittance (Note 1)	$ Y_{fs} $	$V_{DS} = 10\text{ V}, I_D = 200\text{ mA}$	—	1	—	S

Note 1: Pulse measurement.

**5.2. Dynamic Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	$C_{iss}$	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	—	26	40	$\text{pF}$
Reverse transfer capacitance	$C_{rss}$		—	1.3	—	
Output capacitance	$C_{oss}$		—	5.5	—	
Switching time (rise time)	$t_r$	$V_{DD} = 30\text{ V}, I_D = 200\text{ mA},$ $V_{GS} = 0\text{ to }10\text{ V}, R_G = 50\text{ }\Omega,$ Duty $\leq 1\%$ , $V_{IN}: t_r, t_f < 5\text{ ns},$ Common source, See Chapter 5.3.	—	3.6	—	ns
Switching time (turn-on delay time)	$t_{d(on)}$		—	5.5	11	
Switching time (fall time)	$t_f$		—	17	—	
Switching time (turn-off delay time)	$t_{d(off)}$		—	38	90	

**5.3. Switching Time Test Circuit**

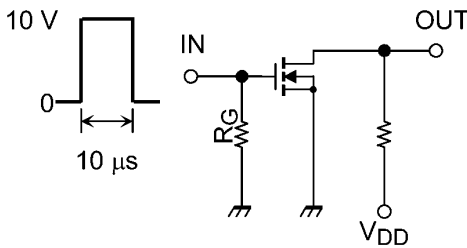


Fig. 5.3.1 Switching Time Test Circuit

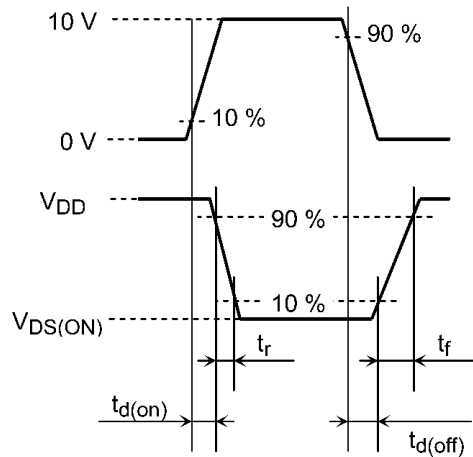


Fig. 5.3.2 Input Waveform/Output Waveform

**5.4. Gate Charge Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ )**

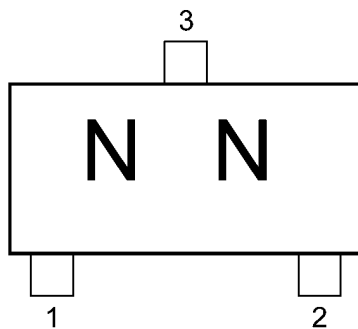
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	$Q_g$	$V_{DD} = 30\text{ V}, I_D = 200\text{ mA},$ $V_{GS} = 4.5\text{ V}$	—	0.39	0.6	nC
Gate-source charge	$Q_{gs}$		—	0.2	—	
Gate-drain charge	$Q_{gd}$		—	0.11	—	

**5.5. Source-Drain Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage (Note 1)	$V_{DSF}$	$I_D = -115\text{ mA}$ , $V_{GS} = 0\text{ V}$	—	-0.79	-1.1	V

Note 1: Pulse measurement.

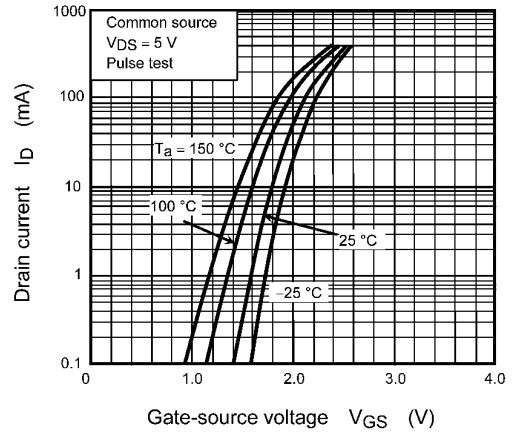
**6. Marking**



**7. Characteristics Curves (Note)**



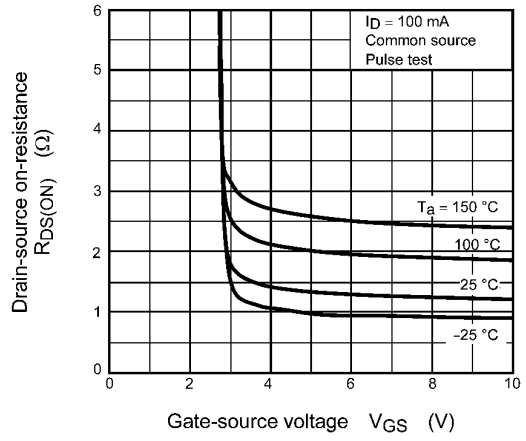
**Fig. 7.1  $I_D - V_{DS}$**



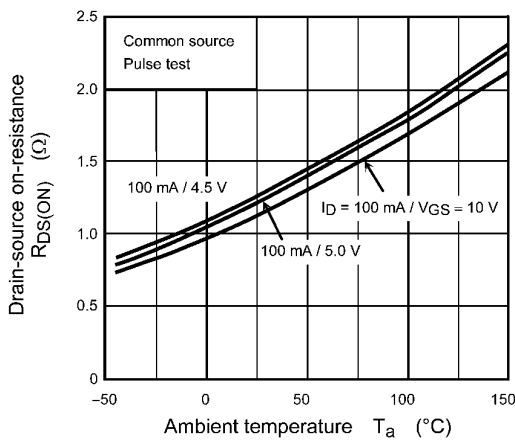
**Fig. 7.2  $I_D - V_{GS}$**



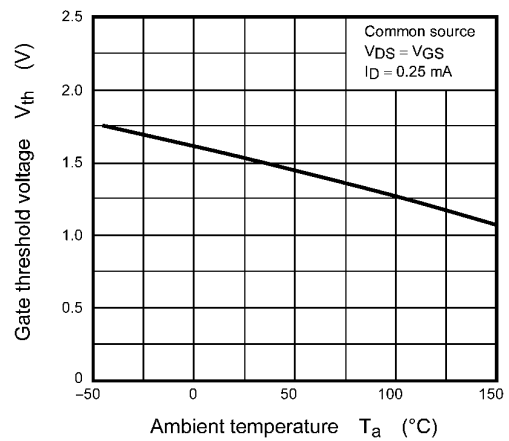
**Fig. 7.3  $R_{DS(ON)} - I_D$**



**Fig. 7.4  $R_{DS(ON)} - V_{GS}$**



**Fig. 7.5  $R_{DS(ON)} - T_a$**



**Fig. 7.6  $V_{th} - T_a$**



Fig. 7.7 C -  $V_{DS}$

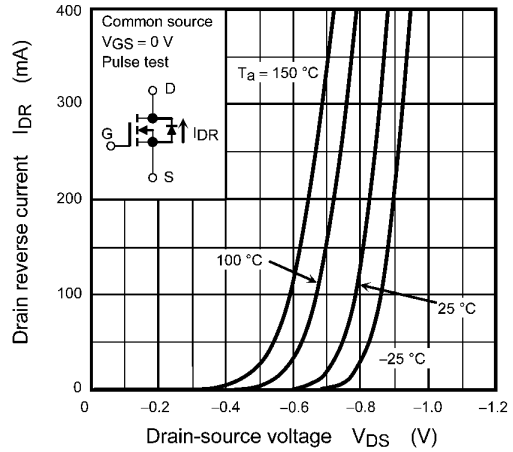


Fig. 7.8  $I_{DR}$  -  $V_{DS}$



Fig. 7.9 Dynamic Input Characteristics

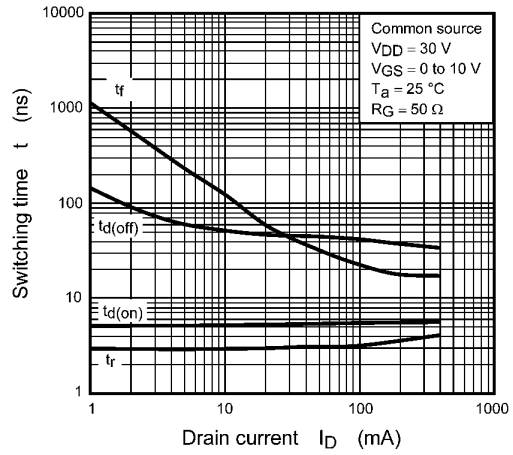


Fig. 7.10  $t$  -  $I_D$

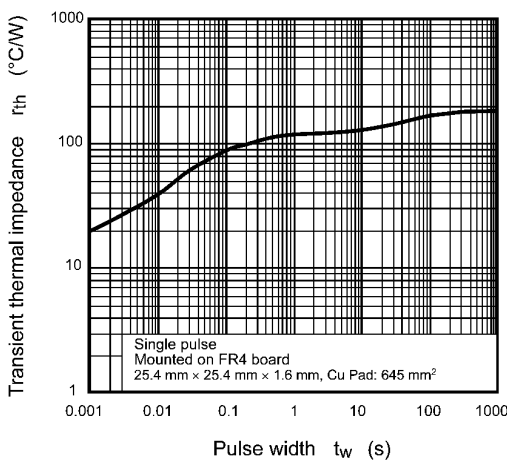


Fig. 7.11  $r_{th}$  -  $t_w$

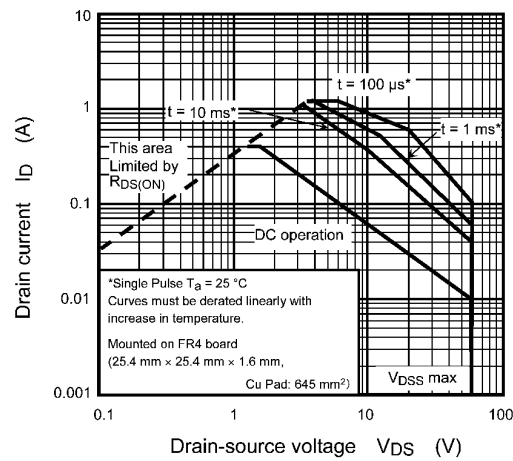
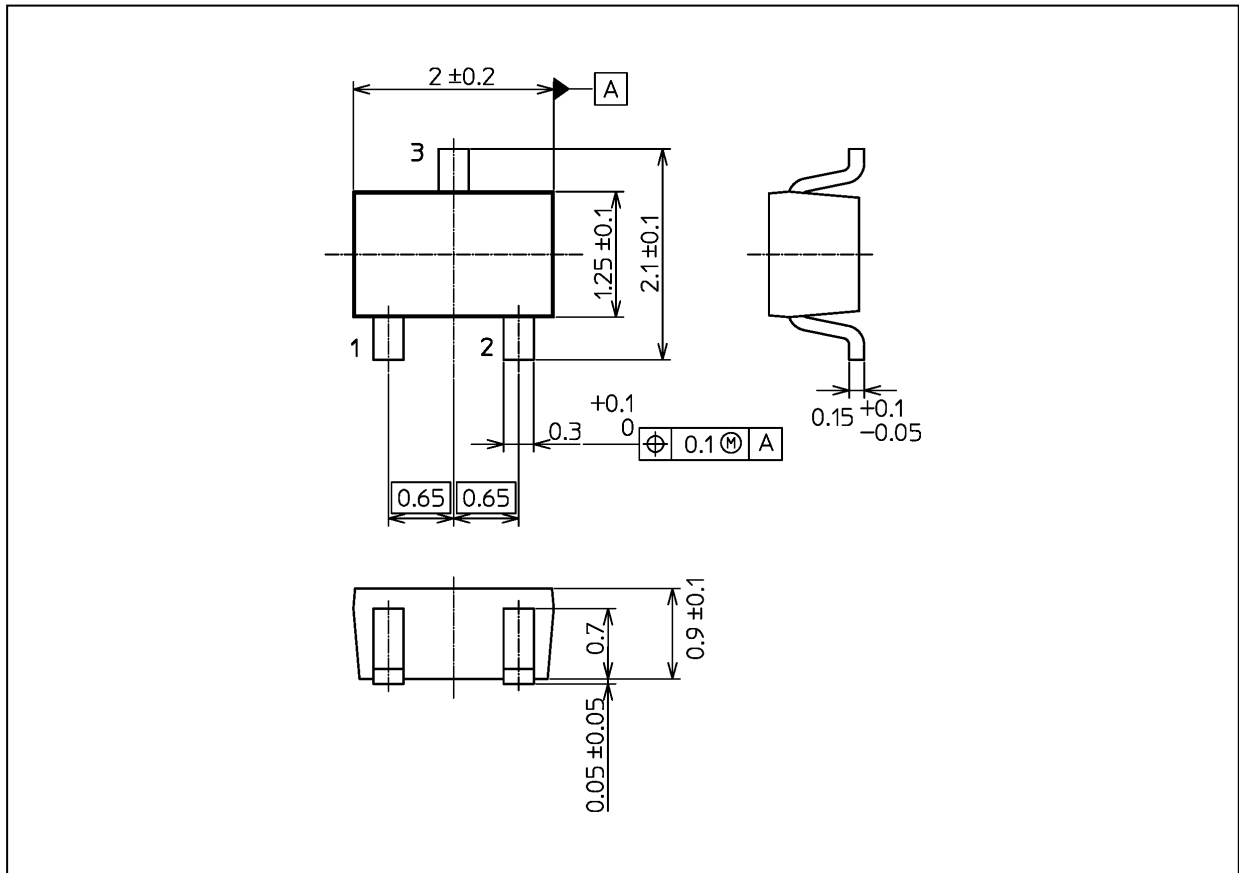


Fig. 7.12 Safe Operating Area

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 6.0 mg (typ.)

Package Name(s)
TOSHIBA: 2-2E1S
Nickname: USM

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