

ESD Protection Diodes Silicon Epitaxial Planar

# DF2B36FU

# 1. Applications

· ESD Protection

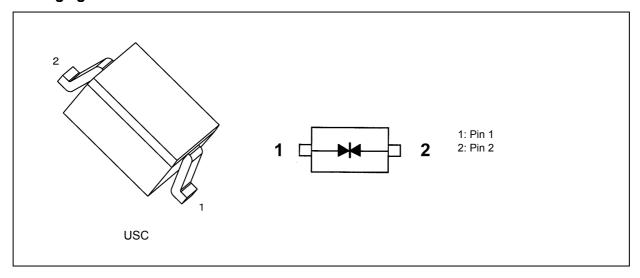
Note: This product is designed for protection against electrostatic discharge (ESD) and is not intended for any other purpose, including, but not limited to, voltage regulation.

#### 2. Features

(1) AEC-Q101 qualified (Note 1)

Note 1: For detail information, please contact to our sales.

#### 3. Packaging and Internal Circuit





#### 4. Absolute Maximum Ratings (Note) (Unless otherwise specified, Ta = 25°C)

Characteristics	Symbol	Note	Rating	Unit
Electrostatic discharge voltage (IEC61000-4-2)(Contact)	V <sub>ESD</sub>	(Note 1)	±20	kV
Electrostatic discharge voltage (IEC61000-4-2)(Air)				
Electrostatic discharge voltage (ISO10605)(Contact)	V <sub>ESD</sub>	(Note 2)	±20	kV
Electrostatic discharge voltage (ISO10605)(Air)				
Peak pulse power (tp = 8/20 μs)	P <sub>PK</sub>		150	W
Peak pulse current (tp = 8/20 μs)	I <sub>PP</sub>	(Note 3)	2.5	Α
Junction temperature	Tj		150	°C
Storage temperature	T <sub>stg</sub>		-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: According to IEC61000-4-2.

Note 2: According to ISO10605. (@ C = 330 pF, R =  $2 \text{ k}\Omega$ )

Note 3: According to IEC61000-4-5.

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# 5. Electrical Characteristics (Unless otherwise specified, T<sub>a</sub> = 25°C)

 $V_{\text{RWM}}$ : Working peak reverse voltage

V<sub>BR</sub>: Reverse breakdown voltage I<sub>BR</sub>: Reverse breakdown current

I<sub>R</sub>: Reverse current V<sub>C</sub>: Clamp voltage I<sub>PP</sub>: Peak pulse current R<sub>DYN</sub>: Dynamic resistance

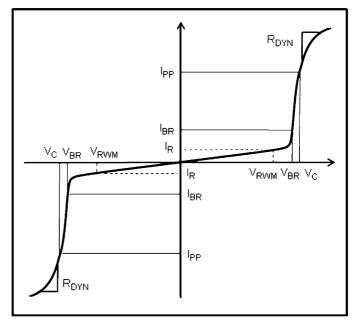


Fig. 5.1 Definitions of Electrical Characteristics

Characteristics	Symbol	Note	Test Condition	Min	Тур.	Max	Unit
Working peak reverse voltage	$V_{RWM}$		_	_	_	28	V
Reverse breakdown voltage	$V_{BR}$		I <sub>BR</sub> = 1 mA	32	36	40	٧
Reverse current	I <sub>R</sub>		V <sub>RWM</sub> = 28 V	_	_	0.1	μА
Clamp voltage	V <sub>C</sub>	(Note 1)	I <sub>PP</sub> = 1 A	_	40	_	٧
			I <sub>PP</sub> = 2.5 A	_	50	60	
Dynamic resistance	R <sub>DYN</sub>	(Note 2)	_		1.5	_	Ω
Total capacitance	Ct	(Note 3)	V <sub>R</sub> = 0 V, f = 1 MHz		6.5	8	pF

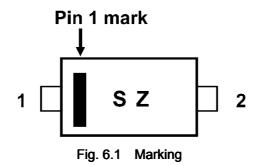
Note 1: Based on IEC61000-4-5 8/20 µs pulse.

Note 2: TLP parameter: Z0 = 50  $\Omega$ , tp = 100 ns, tr = 300 ps, averaging window: t1 = 30 ns to t2 = 60 ns, extraction of dynamic resistance using a least-squares fit of TLP characteristics at I<sub>PP</sub> between 8 A to 16 A.

Note 3: Guaranteed by design.



# 6. Marking



# 7. Land Pattern Dimensions (for reference only)

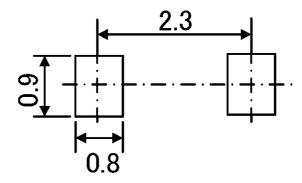


Fig. 7.1 Land Pattern Dimensions (Unit: mm)



# 8. Characteristics Curves (Note)

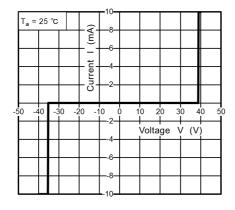


Fig. 8.1 I-V

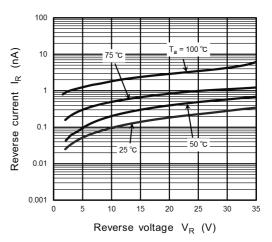


Fig. 8.2 I<sub>R</sub> - V<sub>R</sub>

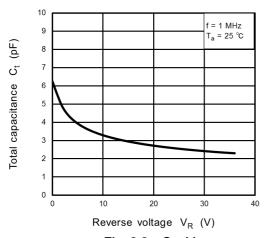
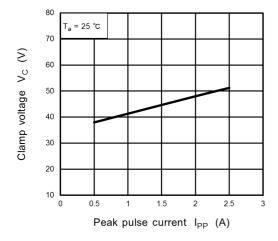


Fig. 8.3 Ct - VR



# 9. Clamp Voltage V<sub>C</sub> - Peak Pulse Current (I<sub>PP</sub>) (Note)



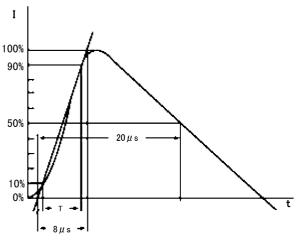


Fig. 9.1 V<sub>C</sub> - I<sub>PP</sub>

Fig. 9.2 Based on IEC61000-4-5 8/20  $\mu$ s pulse. (Ed.2)

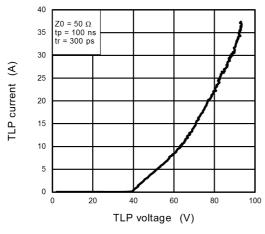


Fig. 9.3 TLP



#### 10. ESD Clamp Waveform (Note)

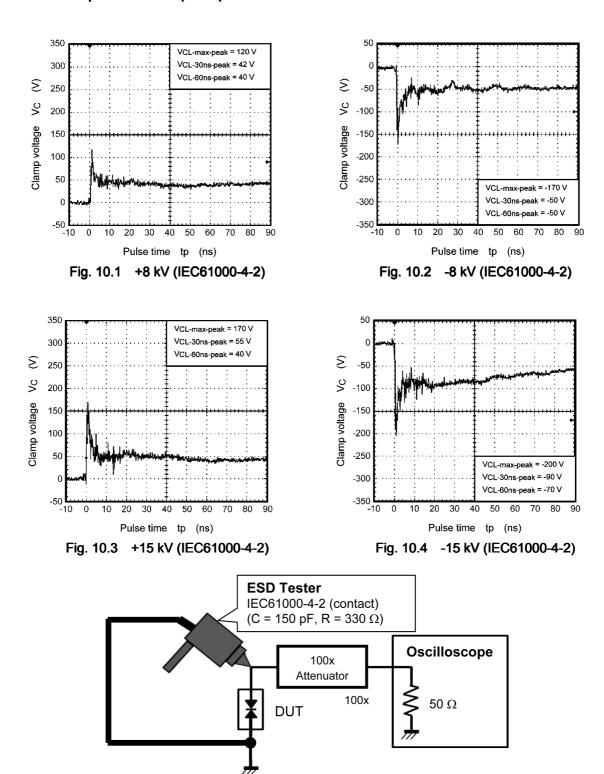
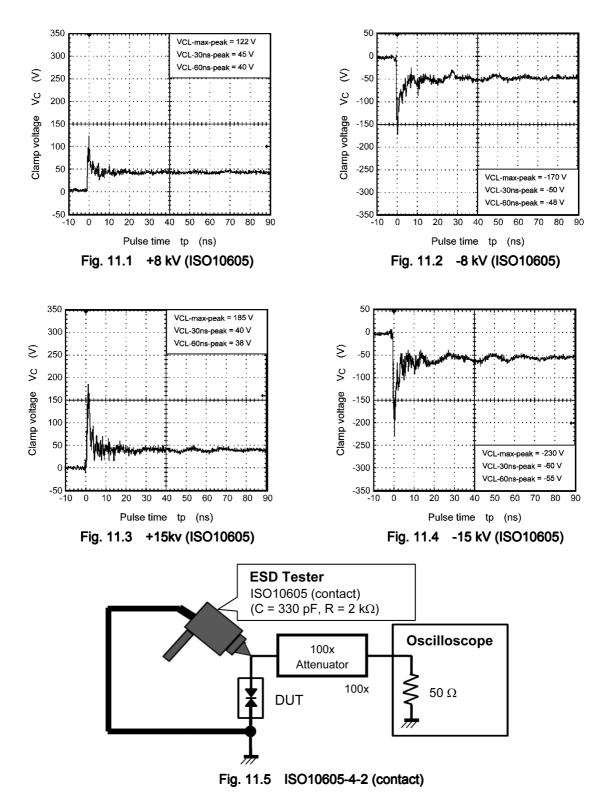


Fig. 10.5 IEC61000-4-2 (Contact)



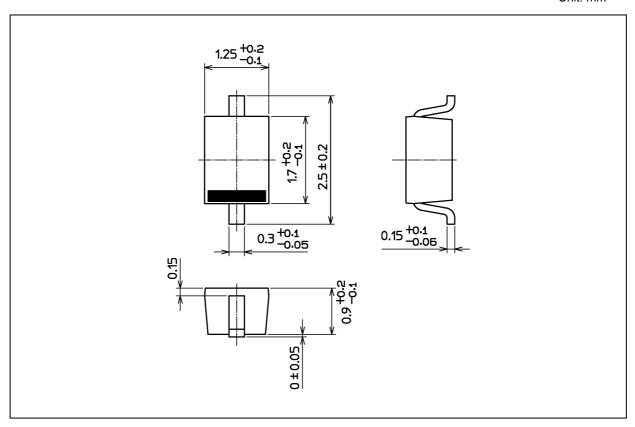
#### 11. ESD Clamp Waveform (Note)





# **Package Dimensions**

Unit: mm



Weight: 4.5 mg (typ.)

	Package Name(s)	
Nickname: USC	_	



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