CMOS Digital Integrated Circuits Silicon Monolithic

74HC123D

1. Functional Description

· Dual Monostable Multivibrator

2. General

The 74HC123D is a high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

There are two trigger inputs, \overline{A} input (negative edge), and B input (positive edge). These inputs are valid for a slow rise/fall time signal ($t_r = t_f = 1$ s) as they are schmitt trigger inputs. This device may also be triggered by using \overline{CLR} input (positive edge).

After triggering, the output stays in a MONOSTABLE state for a time period determined by the external resistor and capacitor (R_X, C_X) . A low level at the \overline{CLR} input breaks this state. In the MONOSTABLE state, if a new trigger is applied, it extends the MONOSTABLE period (retrigger mode).

Limits for C_X and R_X are:

External capacitor, C_X : No limit

External resistor, $R_{X}\mbox{:}\ V_{CC}$ = 2.0 V more than 5 $k\Omega$

 $V_{CC} \geq 3.0~V$ more than $1~k\Omega$

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

3. Features (Note)

- (1) High speed: $t_{pd} = 25$ ns (typ.) at $V_{CC} = 5$ V
- (2) Low power dissipation:

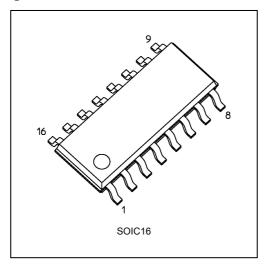
Standby state: I_{CC} = 4.0 μA (max) at T_a = 25 $^{\circ}C$

Active state: I_{CC} = 1000 μA (max) at T_a = 25 $^{\circ}C$

- (3) Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
- (4) Wide operating voltage range: $V_{CC(opr)} = 2.0$ to 6.0 V

Note: In the case of using only one circuit, $\overline{\text{CLR}}$ should be tied to GND, $R_X/C_X \cdot C_X \cdot Q \cdot \overline{Q}$ should be tied to OPEN, the other inputs should be tied to V_{CC} or GND.

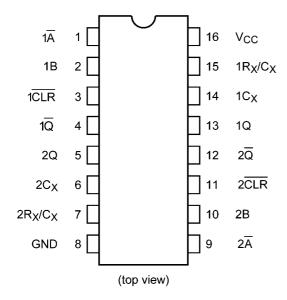
4. Packaging



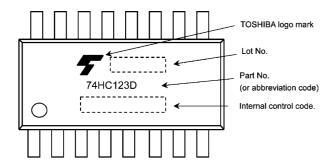
Start of commercial production



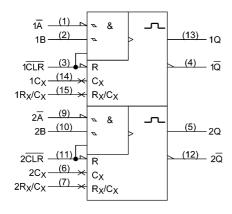
5. Pin Assignment



6. Marking



7. IEC Logic Symbol



Rev.3.0

8. Truth Table

	Inputs			puts	Function
Ā	В	CLR	Q	Q	FullCuoli
\neg	Н	H			Output Enable
Х	L	Н	L	Н	Inhibit
Н	Х	Н	L	Н	Inhibit
L		Н			Output Enable
L	Н	Ļ,		\supset	Output Enable
Х	Х	L	L H		Reset

X: Don't care

9. Block Diagram

(1) C_X, R_X, D_X are external Capacitor, resistor, and diode, respectively.

(2) External clamping diode, D_X;

The external capacitor is charged to V_{CC} level in the wait state, i.e. when no trigger is applied. If the supply voltage is turned off, C_X is discharges mainly through the internal (parasitic) diode. If C_X is sufficiently large and V_{CC} drops rapidly, there will be some possibility of damaging the IC through in rush current or latch-up. If the capacitance of the supply voltage filter is large enough and V_{CC} drops slowly, the in rush current is automatically limited and damage to the IC is avoided.

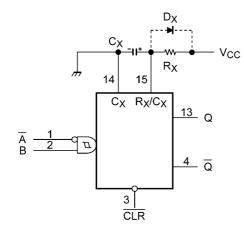
The maximum value of forward current through the parasitic diode is ± 20 mA.

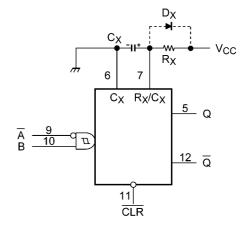
In the case of a large C_X , the limit of fall time of the supply voltage is determined as follows:

$$t_f \ge (V_{CC} - 0.7) C_X/20 \text{ mA}$$

(t_f is the time between the supply voltage turn off and the supply voltage reaching 0.4 V_{CC} .)

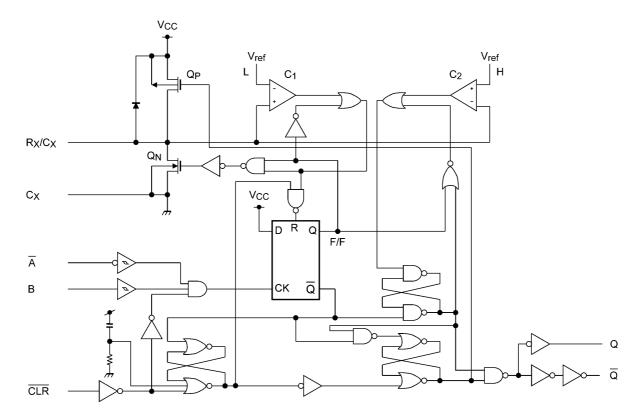
In the even a system does not satisfy the above condition, an external clamping diode (D_X) is needed to protect the IC from rush current.



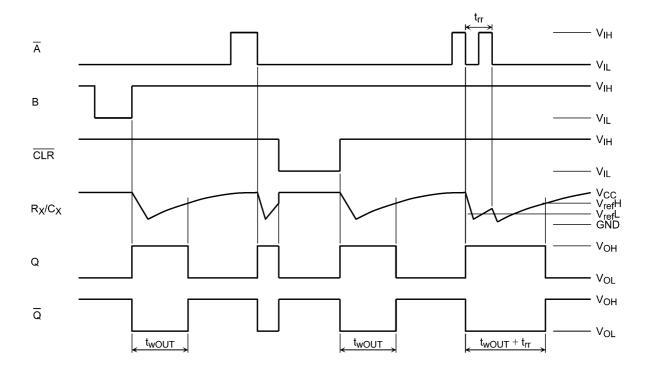




10. System Diagram



11. Timing Chart



Rev.3.0



12. Functional Description

(1) Standby state

The external capacitor (C_X) is fully charged to V_{CC} in the stand-by state. That means, before triggering, the Q_P and Q_N transistors which are connected to the R_X/C_X node are in the off state. Two comparators that relate to the timing of the output pulse, and two reference voltage supplies turn off. The total supply current is only leakage current.

(2) Trigger operation

Trigger operation is effective in any of the following three cases. First, the condition where the \overline{A} input is low, and the B input has a rising signal; second, where the B input is high, and the \overline{A} input has a falling signal; and third, where the \overline{A} input is low and the B input is high, and the \overline{CLR} input has a rising signal. After a trigger becomes effective, comparators C_1 and C_2 start operating, and Q_N is turned on. The external capacitor discharges through Q_N . The voltage level at the R_X/C_X node drops. If the R_X/C_X voltage level falls to the internal reference voltage $V_{ref}L$, the output of C_1 becomes low. The flip-flop is then reset and Q_N turns off. At that moment C_1 stops but C_2 continues operating.

After Q_N turns off, the voltage at the R_X/C_X node starts rising at a rate determined by the time constant of external capacitor C_X and resistor R_X .

Upon triggering, output Q becomes high, following some delay time of the internal F/F and gates. It stays high even if the voltage of R_X/C_X changes from falling to rising. When R_X/C_X reaches the internal reference voltage $V_{ref}H$, the output of C_2 becomes low, the output Q goes low and C_2 stops its operation. That means, after triggering, when the voltage level of the R_X/C_X node reaches $V_{ref}H$, the IC returns to its MONOSTABLE state.

With large values of C_X and R_X , and ignoring the discharge time of the capacitor and internal delays of the IC, the width of the output pulse, t_{wOUT} , is as follows:

$$t_{wOUT} = 1.0 \times C_X \times R_X$$

(3) Retrigger operation

When a new trigger is applied to either input \overline{A} or B while in the MONOSTABLE state, it is effective only if the IC is charging C_X . The voltage level of the R_X/C_X node then falls to $V_{ref}L$ level again. Therefore the Q output stays high if the next trigger comes in before the time period set by C_X and R_X .

If the new trigger is very close to previous trigger, such as an occurrence during the discharge cycle, it will have no effect.

The minimum time for a trigger to be effective 2 nd trigger, t_{rr} (min), depends on V_{CC} and C_X.

(4) Reset operation

In normal operation, the \overline{CLR} input is held high. If \overline{CLR} is low, a trigger has no effect because the Q output is held low and the trigger control F/F is reset. Also, Q_P turns on and C_X is charged rapidly to V_{CC} . This means if \overline{CLR} is set low, the IC goes into a wait state.



13. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V _{CC}		-0.5 to 7.0	V
Input voltage	V _{IN}		-0.5 to V _{CC} + 0.5	V
Output voltage	V _{OUT}		-0.5 to V _{CC} + 0.5	V
Input diode current	I _{IK}		±20	mA
Output diode current	I _{OK}		±20	mA
Output current	I _{OUT}		±25	mA
V _{CC} /ground current	I _{CC}		±50	mA
Power dissipation	P _D		500	mW
Storage temperature	T _{stg}		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

14. Operating Ranges (Note)

Characteristics	Symbol	Note	Test Condition Rating		Unit
Supply voltage	V _{CC}		_	2.0 to 6.0	V
Input voltage	V _{IN}		_	0 to V _{CC}	V
Output voltage	V _{OUT}			0 to V _{CC}	V
Operating temperature	T _{opr}		_	-40 to 85	°C
Input rise and fall times	t _r ,t _f		V _{CC} = 2.0 V	0 to 1000	ns
			V _{CC} = 4.5 V	0 to 500	ns
			V _{CC} = 6.0 V	0 to 400	ns
External capacitor	C _X	(Note 1)	_	No limitation	F
External resistor	R _X	(Note 1)	V _{CC} = 2.0 V	≥ 5 k	Ω
			$V_{CC} \ge 3.0 \text{ V}$	≥ 1 k	Ω

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Note 1: The maximum allowable values of C_X and R_X are a function of leakage of capacitor C_X , the leakage of 74HC123D, and leakage due to board layout and surface resistance.

Susceptibility to externally induced noise signals may occur for $R_X > 1 M\Omega$.



15. Electrical Characteristics

15.1. DC Characteristics (Unless otherwise specified, $T_a = 25$ °C)

Characteristics	Symbol	Test Condition		V _{CC} (V)	Min	Тур.	Max	Unit
High-level input voltage	V_{IH}	_		2.0	1.50	_	_	V
				4.5	3.15	_	_	
				6.0	4.20	_	_	V
Low-level input voltage	V _{IL}	_		2.0	-	_	0.50	V
				4.5	_	_	1.35	
				6.0	-		1.80	V
High-level output voltage	V _{OH}	$V_{IN} = V_{IH}$ or V_{IL}	I _{OH} = -20 μA	2.0	1.9	2.0		V
				4.5	4.4	4.5		
				6.0	5.9	6.0	_	
			$I_{OH} = -4 \text{ mA}$	4.5	4.18	4.31	_	
			$I_{OH} = -5.2 \text{ mA}$	6.0	5.68	5.80		
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	I _{OL} = 20 μA	2.0		0.0	0.1	V
				4.5	_	0.0	0.1	
				6.0	_	0.0	0.1	
			I _{OL} = 4 mA	4.5		0.17	0.26	
			I _{OL} = 5.2 mA	6.0	_	0.18	0.26	V
Input leakage current	I _{IN}	$V_{IN} = V_{CC}$ or GND		6.0	1		±0.1	μΑ
R _X /C _X terminal OFF-state current	I _{IN}	$V_{IN} = V_{CC}$ or GND		6.0			±0.1	μΑ
Quiescent supply current	I _{CC}	$V_{IN} = V_{CC}$ or GND		6.0	1	1	4.0	μА
Active-state supply current	I _{CC(opr)}	V _{IN} = V _{CC} or GND		2.0	1	45	200	μА
(per circuit)		$R_X/C_X = 0.5 V_{CC}$		4.5	1	400	500	
				6.0		700	1000	



15.2. DC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Test Conditio	n	V _{CC} (V)	Min	Max	Unit
High-level input voltage	V _{IH}	_		2.0	1.50	_	V
				4.5	3.15	_	
				6.0	4.20	_	
Low-level input voltage	V _{IL}	_		2.0		0.50	V
				4.5		1.35	
				6.0		1.80	
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20 μA	2.0	1.9	_	V
				4.5	4.4	_	
				6.0	5.9	_]
			I _{OH} = -4 mA	4.5	4.13	_]
			I _{OH} = -5.2 mA	6.0	5.63	_	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20 μA	2.0	_	0.1	V
				4.5	_	0.1	
				6.0	_	0.1	
			I _{OL} = 4 mA	4.5	_	0.33]
			I _{OL} = 5.2 mA	6.0	_	0.33	V
Input leakage current	I _{IN}	$V_{IN} = V_{CC}$ or GND		6.0	_	±1.0	μА
R _X /C _X terminal OFF-state current	I _{IN}	V _{IN} = V _{CC} or GND		6.0	_	±1.0	μА
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND		6.0	_	40.0	μА
Active-state supply current	I _{CC(opr)}	V _{IN} = V _{CC} or GND		2.0	_	260	μА
(per circuit)		$R_X/C_X = 0.5 V_{CC}$		4.5	_	650]
				6.0		1300	

15.3. Timing Requirements (Unless otherwise specified, T_a = 25 °C, Input: t_r = t_f = 6 ns)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Тур.	Limit	Unit
Minimum pulse width	$t_{w(L)},t_{w(H)}$	_	2.0	_	75	ns
			4.5	_	15	
			6.0	_	13	
Minimum pulse width	t _{w(L)}	_	2.0		75	ns
(CLR)			4.5		15	
			6.0	_	13	
Minimum retrigger time	t _{rr}	$R_X = 1 \text{ k}\Omega, C_X = 100 \text{ pF}$	2.0	325	_	ns
			4.5	108	_	
			6.0	78	_	
Minimum retrigger time	t _{rr}	$R_X = 1 \text{ k}\Omega, C_X = 0.01 \mu\text{F}$	2.0	5.0	_	μS
			4.5	1.4	_	
			6.0	1.2	_	

15.4. Timing Requirements (Unless otherwise specified, T_a = -40 to 85 °C, Input: t_r = t_f = 6 ns)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Limit	Unit
Minimum pulse width	$t_{w(L)}, t_{w(H)}$	_	2.0	95	ns
			4.5	19	
			6.0	16	
Minimum pulse width	t _{w(L)}		2.0	95	ns
(CLR)			4.5	19	
			6.0	16	



16. AC Characteristics (Unless otherwise specified, $C_L = 15 \text{ pF}$, $V_{CC} = 5 \text{ V}$, $T_a = 25 ^{\circ}\text{C}$, Input: $t_r = t_f = 6 \text{ ns}$)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Output transition time	t _{TLH} ,t _{THL}	_		4	8	ns
Propagation delay time $(\overline{A}, B - Q, \overline{Q})$	t _{PLH} ,t _{PHL}	_		25	36	
Propagation delay time (CLR Trigger - Q, Q)	t _{PLH} ,t _{PHL}	_	I	26	41	
Propagation delay time $(\overline{\text{CLR}} - Q, \overline{Q})$	t _{PLH} ,t _{PHL}	_	I	16	27	

16.1. AC Characteristics (Unless otherwise specified, C_L = 50 pF, T_a = 25 °C, Input: t_r = t_f = 6 ns)

Characteristics	Symbol	Note	Test Condition	V _{CC} (V)	Min	Тур.	Max	Unit
Output transition time	t_{TLH}, t_{THL}		_	2.0	_	30	75	ns
				4.5		8	15	
				6.0	_	7	13	
Propagation delay time	t_{PLH}, t_{PHL}		_	2.0		102	210	ns
$(\overline{A}, B-Q, \overline{Q})$				4.5		29	42	
				6.0		22	36	
Propagation delay time	t_{PLH}, t_{PHL}		_	2.0		102	235	ns
(CLR trigger-Q, Q)				4.5		31	47	
				6.0	_	22	40	
Propagation delay time	t _{PLH} ,t _{PHL}		_	2.0	_	68	160	ns
$(\overline{CLR}-Q,\overline{Q})$				4.5		20	32	
				6.0		16	27	
Output pulse width	t _{wOUT}		$C_X = 28 \text{ pF}$ $R_X = 6 \text{ k}\Omega$	2.0		700	2000	ns
			C _X = 28 pF	4.5		250	400	
			$R_X = 2 k\Omega$	6.0	_	210	340	
			$C_X = 0.01 \mu F$,	2.0	90	110	130	μS
			$R_X = 10 \text{ k}\Omega$	4.5	95	105	115	
				6.0	95	105	115	
			$C_X = 0.1 \mu F$,	2.0	0.9	1.0	1.2	ms
			$R_X = 10 \text{ k}\Omega$	4.5	0.9	1.0	1.1	
				6.0	0.9	1.0	1.1	
Output pulse width error between circuits (in same package)	Δt_{wOUT}		_		_	±1	_	%
Input capacitance	C _{IN}		_			5	_	pF
Power dissipation capacitance	C _{PD}	(Note 1)	_			162	_	pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

 $I_{CC(opr)}$ = $C_{PD} \times V_{CC} \times f_{IN}$ + $I_{CC'} \times Duty/100$ + $I_{CC}/2$ (per circuit),

(I_{CC'}: Active supply current),

(Duty: %)

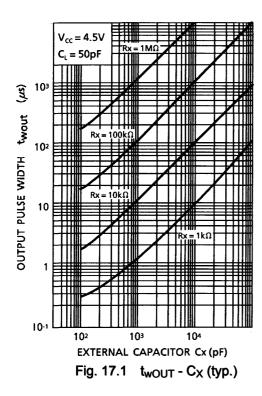


16.2. AC Characteristics (Unless otherwise specified, C_L = 50 pF, T_a = -40 to 85 °C, Input: t_r = t_f = 6 ns)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Min	Max	Unit
Output transition time	t _{TLH} ,t _{THL}	_	2.0	_	95	ns
			4.5	_	19	
			6.0		16	1
Propagation delay time	t _{PLH} ,t _{PHL}	_	2.0		265	ns
$(\overline{A}, B-Q, \overline{Q})$			4.5		53	
			6.0	_	45	1
Propagation delay time	t _{PLH} ,t _{PHL}	_	2.0		295	ns
$(\overline{CLR}\ trigger-Q,\overline{Q})$			4.5		59	
			6.0		50	1
Propagation delay time	t _{PLH} ,t _{PHL}	_	2.0		200	ns
$(\overline{CLR}-Q,\overline{Q})$			4.5		40	
			6.0	_	34	1
Output pulse width	t _{wOUT}	$C_X = 28 \text{ pF}, R_X = 6 \text{ k}\Omega$	2.0	_	2500	ns
		$C_X = 28 \text{ pF}, R_X = 2 \text{ k}\Omega$	4.5	_	500	ns
			6.0	_	425	ns
		$C_X = 0.01 \mu F, R_X = 10 k\Omega$	2.0	90	130	μS
			4.5	95	115	μS
			6.0	95	115	μS
		$C_X = 0.1 \mu F, R_X = 10 k\Omega$	2.0	0.9	1.2	ms
			4.5	0.9	1.1	ms
			6.0	0.9	1.1	ms



17. Characteristics Curves (Note)



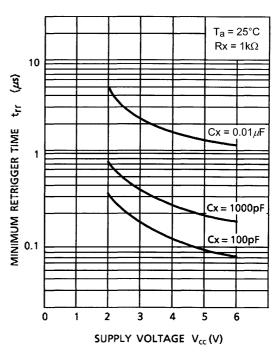


Fig. 17.2 t_{rr} - V_{CC} (typ.)

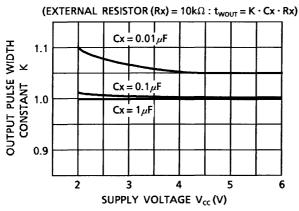


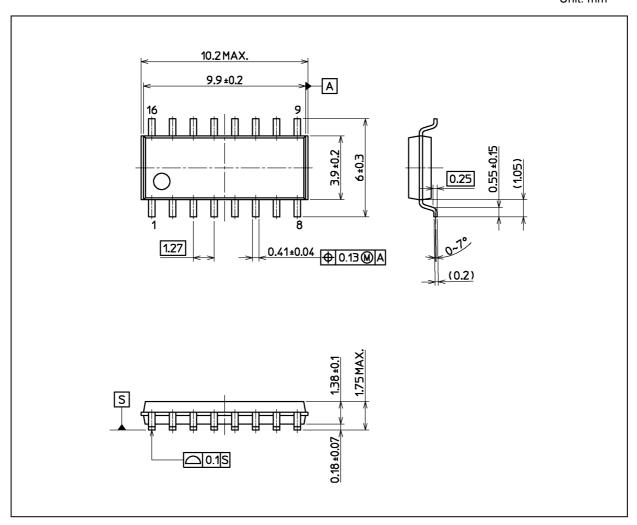
Fig. 17.3 Output Pulse Width Constant K - Supply Voltage (typ.)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



Package Dimensions

Unit: mm



Weight: 0.15 g (typ.)

	Package Name(s)
Nickname: SOIC16	



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