

# 74HC259D

## 1. Functional Description

- 8-Bit Addressable Latch

## 2. General

The 74HC259D is a high speed CMOS ADDRESSABLE LATCH fabricated with silicon gate C<sup>2</sup>MOS technology. It achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The respective bits are controlled by address inputs A, B, and C. When  $\overline{\text{CLEAR}}$  input is held high and enable input  $\overline{\text{G}}$  is held low, the data is written into the bit selected by address inputs, the other bit hold their previous conditions.

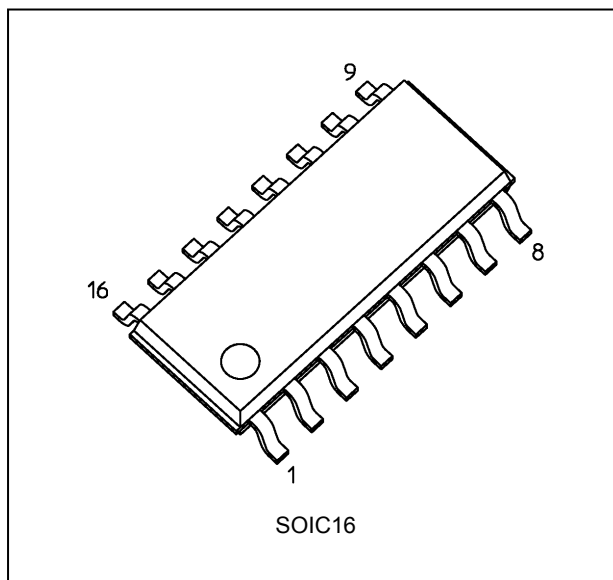
When both  $\overline{\text{CLEAR}}$  and  $\overline{\text{G}}$  held high, writing of all bits is inhibited regardless of adress inputs, and their previous condition are held. When  $\overline{\text{CLEAR}}$  is held low and  $\overline{\text{G}}$  is held high, all bits are resented to low regardless of the other inputs. When both of  $\overline{\text{CLEAR}}$  and  $\overline{\text{G}}$  held low, all bits which isn't selected by adress inputs are resented to low.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

## 3. Features

- (1) High speed:  $t_{pd} = 15 \text{ ns (typ.)}$  at  $V_{CC} = 5 \text{ V}$
- (2) Low power dissipation:  $I_{CC} = 4.0 \mu\text{A (max)}$  at  $T_a = 25 \text{ }^\circ\text{C}$
- (3) Balanced propagation delays:  $t_{PLH} \approx t_{PHL}$
- (4) Wide operating voltage range:  $V_{CC(opr)} = 2.0 \text{ to } 6.0 \text{ V}$

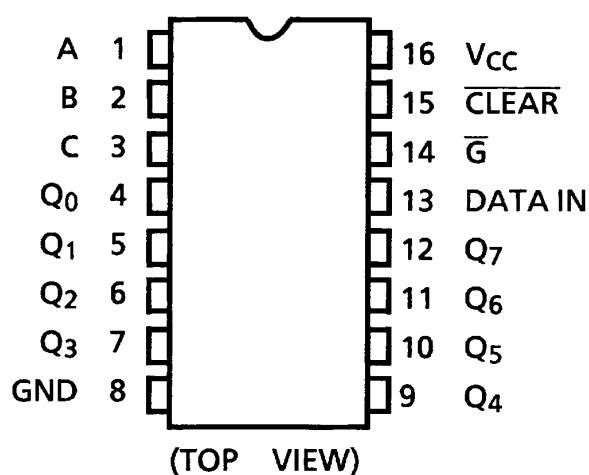
## 4. Packaging



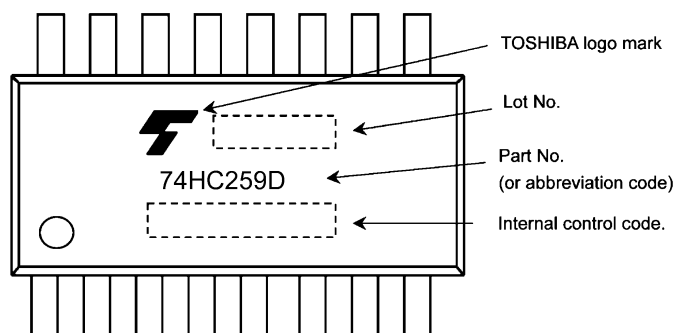
Start of commercial production

2016-05

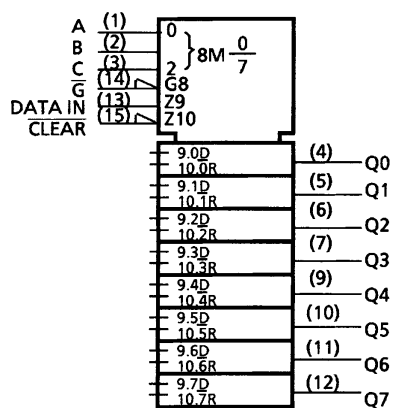
## 5. Pin Assignment



## 6. Marking



## 7. IEC Logic Symbol



## 8. Truth Table

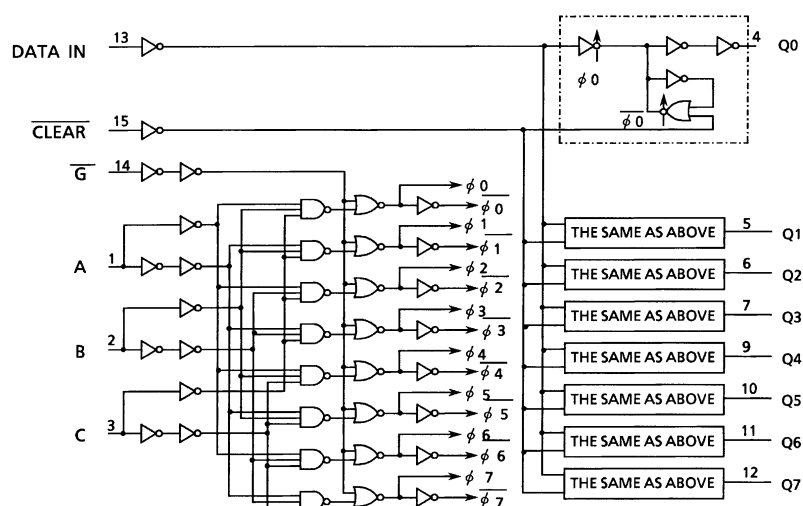
Inputs		Output of Addressed Latch	Each Other Output	Function
$\overline{\text{CLEAR}}$	$\overline{\text{G}}$			
H	L	D	QiO	Addressable Latch
H	H	QiO	QiO	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear All Bits to "L"

Select Inputs			Latch Addressed
C	B	A	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

D: The level at the data input

QiO: The level before the indicated steady-state input conditions were established ( $i = 0, 1, \dots, 7$ )

## 9. System Diagram



## 10. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	$V_{CC}$		-0.5 to 7.0	V
Input voltage	$V_{IN}$		-0.5 to $V_{CC} + 0.5$	V
Output voltage	$V_{OUT}$		-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$		$\pm 20$	mA
Output diode current	$I_{OK}$		$\pm 20$	mA
Output current	$I_{OUT}$		$\pm 25$	mA
$V_{CC}$ /ground current	$I_{CC}$		$\pm 50$	mA
Power dissipation	$P_D$	(Note 1)	500	mW
Storage temperature	$T_{stg}$		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1:  $P_D$  derates linearly with -8 mW/°C above 85 °C

## 11. Operating Ranges (Note)

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	$V_{CC}$	—	2.0 to 6.0	V
Input voltage	$V_{IN}$	—	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	—	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	—	-40 to 125	°C
Input rise and fall times	$t_r, t_f$	—	0 to 50	μs

Note: The operating ranges are required to ensure the normal operation of the device. Unused inputs must be tied to either  $V_{CC}$  or GND.

## 12. Electrical Characteristics

12.1. DC Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^{\circ}\text{C}$ )

Characteristics	Symbol	Test Condition		$V_{CC}$ (V)	Min	Typ.	Max	Unit
High-level input voltage	$V_{IH}$	—		2.0	1.50	—	—	V
				4.5	3.15	—	—	
				6.0	4.20	—	—	
Low-level input voltage	$V_{IL}$	—		2.0	—	—	0.50	V
				4.5	—	—	1.35	
				6.0	—	—	1.80	
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20\text{ }\mu\text{A}$	2.0	1.9	2.0	—	V
				4.5	4.4	4.5	—	
				6.0	5.9	6.0	—	
			$I_{OH} = -4\text{ mA}$	4.5	4.18	4.31	—	
			$I_{OH} = -5.2\text{ mA}$	6.0	5.68	5.80	—	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20\text{ }\mu\text{A}$	2.0	—	0.0	0.1	V
				4.5	—	0.0	0.1	
				6.0	—	0.0	0.1	
			$I_{OL} = 4\text{ mA}$	4.5	—	0.17	0.26	
			$I_{OL} = 5.2\text{ mA}$	6.0	—	0.18	0.26	
Input leakage current	$I_{IN}$	$V_{IN} = V_{CC} \text{ or } GND$		6.0	—	—	$\pm 0.1$	$\mu\text{A}$
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC} \text{ or } GND$		6.0	—	—	4.0	$\mu\text{A}$

12.2. DC Characteristics (Unless otherwise specified,  $T_a = -40 \text{ to } 85\text{ }^{\circ}\text{C}$ )

Characteristics	Symbol	Test Condition		$V_{CC}$ (V)	Min	Max	Unit
High-level input voltage	$V_{IH}$	—		2.0	1.50	—	V
				4.5	3.15	—	
				6.0	4.20	—	
Low-level input voltage	$V_{IL}$	—		2.0	—	0.50	V
				4.5	—	1.35	
				6.0	—	1.80	
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20\text{ }\mu\text{A}$	2.0	1.9	—	V
				4.5	4.4	—	
				6.0	5.9	—	
			$I_{OH} = -4\text{ mA}$	4.5	4.13	—	
			$I_{OH} = -5.2\text{ mA}$	6.0	5.63	—	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20\text{ }\mu\text{A}$	2.0	—	0.1	V
				4.5	—	0.1	
				6.0	—	0.1	
			$I_{OL} = 4\text{ mA}$	4.5	—	0.33	
			$I_{OL} = 5.2\text{ mA}$	6.0	—	0.33	
Input leakage current	$I_{IN}$	$V_{IN} = V_{CC} \text{ or } GND$		6.0	—	$\pm 1.0$	$\mu\text{A}$
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC} \text{ or } GND$		6.0	—	40.0	$\mu\text{A}$

12.3. DC Characteristics (Unless otherwise specified,  $T_a = -40$  to  $125\text{ }^{\circ}\text{C}$ )

Characteristics	Symbol	Test Condition		$V_{CC}$ (V)	Min	Max	Unit
High-level input voltage	$V_{IH}$	—		2.0	1.50	—	V
				4.5	3.15	—	
				6.0	4.20	—	
Low-level input voltage	$V_{IL}$	—		2.0	—	0.50	V
				4.5	—	1.35	
				6.0	—	1.30	
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20\text{ }\mu\text{A}$	2.0	1.9	—	V
				4.5	4.4	—	
				6.0	5.9	—	
			$I_{OH} = -4\text{ mA}$	4.5	3.7	—	
			$I_{OH} = -5.2\text{ mA}$	6.0	5.2	—	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20\text{ }\mu\text{A}$	2.0	—	0.1	V
				4.5	—	0.1	
				6.0	—	0.1	
			$I_{OL} = 4\text{ mA}$	4.5	—	0.4	V
			$I_{OL} = 5.2\text{ mA}$	6.0	—	0.4	
Input leakage current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND		6.0	—	$\pm 1.0$	$\mu\text{A}$
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND		6.0	—	160.0	$\mu\text{A}$

## 13. Timing Requirements

(Unless otherwise specified,  $T_a = 25\text{ }^{\circ}\text{C}$ , Input:  $t_r = t_f = 6\text{ ns}$ )

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Limit	Unit
Minimum pulse width ( $\overline{G}$ )	$t_{w(L)}$	—	2.0	75	ns
			4.5	15	
			6.0	13	
Minimum pulse width (CLEAR)	$t_{w(L)}$	—	2.0	75	ns
			4.5	15	
			6.0	13	
Minimum setup time (DATA IN)	$t_s$	—	2.0	50	ns
			4.5	10	
			6.0	9	
Minimum setup time (A, B, C)	$t_s$	—	2.0	25	ns
			4.5	5	
			6.0	5	
Minimum hold time (DATA IN)	$t_h$	—	2.0	25	ns
			4.5	5	
			6.0	5	
Minimum hold time (A, B, C)	$t_h$	—	2.0	0	ns
			4.5	0	
			6.0	0	

## 13.1. Timing Requirements

(Unless otherwise specified,  $T_a = -40$  to  $85\text{ }^{\circ}\text{C}$ , Input:  $t_r = t_f = 6\text{ ns}$ )

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Limit	Unit
Minimum pulse width ( $\bar{G}$ )	$t_{w(L)}$	—	2.0	95	ns
			4.5	19	
			6.0	16	
Minimum pulse width (CLEAR)	$t_{w(L)}$	—	2.0	95	ns
			4.5	19	
			6.0	16	
Minimum setup time (DATA IN)	$t_s$	—	2.0	60	ns
			4.5	12	
			6.0	11	
Minimum setup time (A, B, C)	$t_s$	—	2.0	30	ns
			4.5	6	
			6.0	5	
Minimum hold time (DATA IN)	$t_h$	—	2.0	30	ns
			4.5	6	
			6.0	5	
Minimum hold time (A, B, C)	$t_h$	—	2.0	0	ns
			4.5	0	
			6.0	0	

## 13.2. Timing Requirements

(Unless otherwise specified,  $T_a = -40$  to  $125\text{ }^{\circ}\text{C}$ , Input:  $t_r = t_f = 6\text{ ns}$ )

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Limit	Unit
Minimum pulse width ( $\bar{G}$ )	$t_{w(L)}$	—	2.0	115	ns
			4.5	23	
			6.0	20	
Minimum pulse width (CLEAR)	$t_{w(L)}$	—	2.0	115	ns
			4.5	23	
			6.0	20	
Minimum setup time (DATA IN)	$t_s$	—	2.0	75	ns
			4.5	15	
			6.0	13	
Minimum setup time (A, B, C)	$t_s$	—	2.0	40	ns
			4.5	8	
			6.0	7	
Minimum hold time (DATA IN)	$t_h$	—	2.0	40	ns
			4.5	8	
			6.0	7	
Minimum hold time (A, B, C)	$t_h$	—	2.0	0	ns
			4.5	0	
			6.0	0	

**14. AC Characteristics**(Unless otherwise specified,  $C_L = 15 \text{ pF}$ ,  $V_{CC} = 5 \text{ V}$ ,  $T_a = 25 \text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	$t_{TLH}, t_{THL}$	—	—	4	8	ns
Propagation delay time (DATA IN - Q)	$t_{PLH}, t_{PHL}$	—	—	15	22	ns
Propagation delay time (A, B, C - Q)	$t_{PLH}, t_{PHL}$	—	—	21	32	ns
Propagation delay time ( $\overline{G}$ - Q)	$t_{PLH}, t_{PHL}$	—	—	16	28	ns
Propagation delay time (CLEAR - Q)	$t_{PHL}$	—	—	13	23	ns

**14.1. AC Characteristics**(Unless otherwise specified,  $C_L = 50 \text{ pF}$ ,  $T_a = 25 \text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Note	$V_{CC} \text{ (V)}$	Min	Typ.	Max	Unit
Output transition time	$t_{TLH}, t_{THL}$		2.0	—	30	75	ns
			4.5	—	8	15	
			6.0	—	7	13	
Propagation delay time (DATA IN - Q)	$t_{PLH}, t_{PHL}$		2.0	—	56	130	ns
			4.5	—	18	26	
			6.0	—	15	22	
Propagation delay time (A, B, C - Q)	$t_{PLH}, t_{PHL}$		2.0	—	83	185	ns
			4.5	—	25	37	
			6.0	—	21	31	
Propagation delay time ( $\overline{G}$ - Q)	$t_{PLH}, t_{PHL}$		2.0	—	67	165	ns
			4.5	—	20	33	
			6.0	—	17	28	
Propagation delay time (CLEAR - Q)	$t_{PHL}$		2.0	—	52	135	ns
			4.5	—	16	27	
			6.0	—	14	23	
Input capacitance	$C_{IN}$		—	—	3	—	pF
Power dissipation capacitance	$C_{PD}$	(Note 1)	—	—	8	—	pF

Note 1:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$$



## 14.2. AC Characteristics

(Unless otherwise specified,  $C_L = 50 \text{ pF}$ ,  $T_a = -40 \text{ to } 85 \text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 6 \text{ ns}$ )

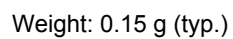
Characteristics	Symbol	$V_{CC} \text{ (V)}$	Min	Max	Unit
Output transition time	$t_{TLH}, t_{THL}$	2.0	—	95	ns
		4.5	—	19	
		6.0	—	16	
Propagation delay time (DATA IN - Q)	$t_{PLH}, t_{PHL}$	2.0	—	165	ns
		4.5	—	33	
		6.0	—	28	
Propagation delay time (A, B, C - Q)	$t_{PLH}, t_{PHL}$	2.0	—	230	ns
		4.5	—	46	
		6.0	—	39	
Propagation delay time ( $\bar{G}$ - Q)	$t_{PLH}, t_{PHL}$	2.0	—	205	ns
		4.5	—	41	
		6.0	—	35	
Propagation delay time (CLEAR - Q)	$t_{PHL}$	2.0	—	170	ns
		4.5	—	34	
		6.0	—	29	

## 14.3. AC Characteristics

(Unless otherwise specified,  $C_L = 50 \text{ pF}$ ,  $T_a = -40 \text{ to } 125 \text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	$V_{CC} \text{ (V)}$	Min	Max	Unit
Output transition time	$t_{TLH}, t_{THL}$	2.0	—	115	ns
		4.5	—	23	
		6.0	—	20	
Propagation delay time (DATA IN - Q)	$t_{PLH}, t_{PHL}$	2.0	—	195	ns
		4.5	—	39	
		6.0	—	33	
Propagation delay time (A, B, C - Q)	$t_{PLH}, t_{PHL}$	2.0	—	280	ns
		4.5	—	56	
		6.0	—	48	
Propagation delay time ( $\bar{G}$ - Q)	$t_{PLH}, t_{PHL}$	2.0	—	235	ns
		4.5	—	47	
		6.0	—	40	
Propagation delay time (CLEAR - Q)	$t_{PHL}$	2.0	—	205	ns
		4.5	—	41	
		6.0	—	35	

## Unit: mm



Package Name(s)
Nickname: SOIC16

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