

74HCT245D

1. Functional Description

- Octal Bus Transceiver

2. General

The 74HCT245D is high speed CMOS OCTAL BUS TRANSCEIVER fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Its inputs are compatible with TTL, NMOS, and CMOS output voltage levels.

It is intended for two-way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

The enable input (\overline{G}) can be used to disable the device so that the busses are effectively isolated.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

3. Features (Note)

- (1) High speed: $t_{pd} = 11 \text{ ns (typ.)}$ at $V_{CC} = 5.5 \text{ V}$
- (2) Low power dissipation: $I_{CC} = 4.0 \mu\text{A (max)}$ at $T_a = 25 \text{ }^\circ\text{C}$
- (3) Compatible with TTL outputs: $V_{IL} = 0.8 \text{ V(max)}$
 $V_{IH} = 2.0 \text{ V(min)}$

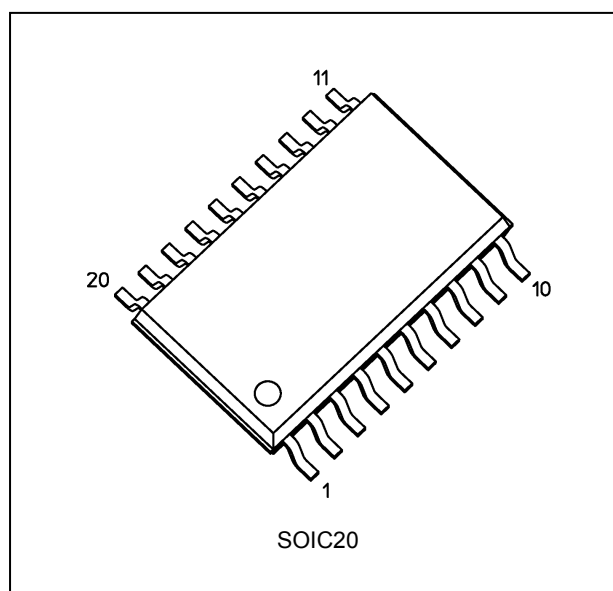
- (4) Wide interfacing ability: LSTTL, NMOS, CMOS

- (5) Balanced propagation delays: $t_{PLH} \approx t_{PHL}$

Note: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.

All floating (high impedance) bus pins must have their input levels fixed by means of pull-up or pull-down resistors.

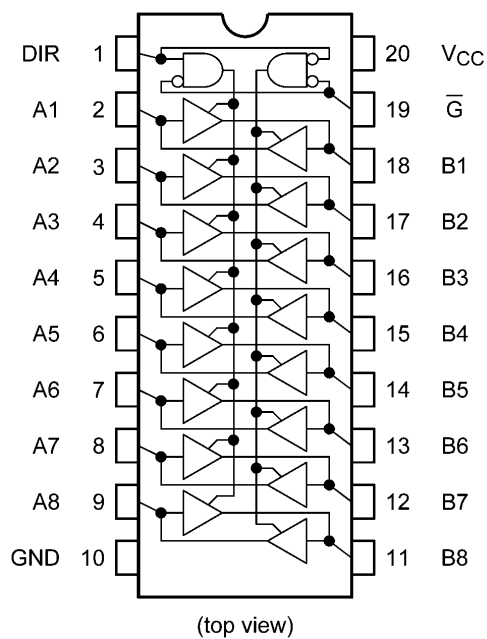
4. Packaging



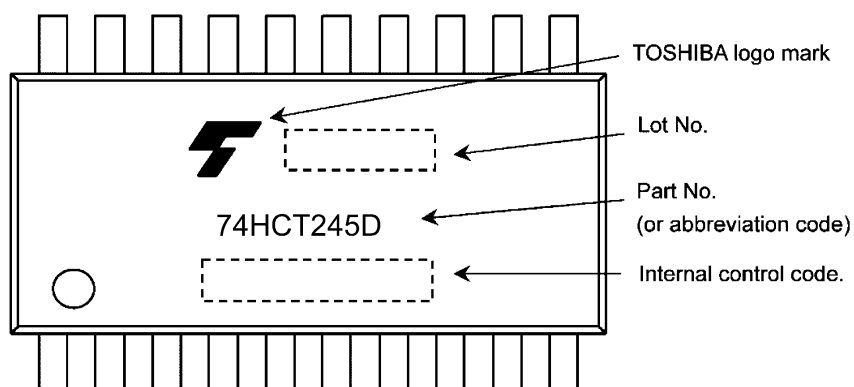
Start of commercial production

2016-04

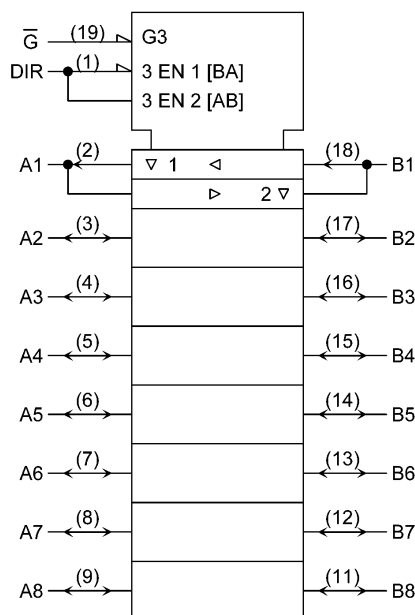
5. Pin Assignment



6. Marking



7. IEC Logic Symbol



8. Truth Table

Input \overline{G}	Input DIR	A Bus	B Bus	Output
L	L	Output	Input	A = B
L	H	Input	Output	B = A
H	X	Z	Z	Z

X: Don't care (L or H)

Z: High impedance

9. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CC}		-0.5 to 7.0	V
Input voltage	V_{IN}		-0.5 to $V_{CC} + 0.5$	V
Output voltage	V_{OUT}		-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}		± 20	mA
Output diode current	I_{OK}		± 20	mA
Output current	I_{OUT}		± 35	mA
V_{CC} /ground current	I_{CC}		± 75	mA
Power dissipation	P_D	(Note 1)	500	mW
Storage temperature	T_{stg}		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: P_D derates linearly with -8 mW/°C above 85 °C

10. Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	4.5 to 5.5	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 125	°C
Input rise and fall times	t_r, t_f	0 to 50	μs

Note: The operating ranges must be maintained to ensure the normal operation of the device.

Unused inputs must be tied to either V_{CC} or GND.

11. Electrical Characteristics

11.1. DC Characteristics (Unless otherwise specified, $T_a = 25\text{ °C}$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Typ.	Max	Unit
High-level input voltage	V_{IH}	—	4.5 to 5.5	2.0	—	—	V
Low-level input voltage	V_{IL}	—	4.5 to 5.5	—	—	0.8	V
High-level output voltage	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20\text{ }\mu\text{A}$	4.5	4.4	4.5	V
			$I_{OH} = -6\text{ mA}$	4.5	4.18	4.31	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20\text{ }\mu\text{A}$	4.5	—	0.0	V
			$I_{OL} = 6\text{ mA}$	4.5	—	0.17	
3-state output OFF-state leakage current	I_{OZ}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = V_{CC} \text{ or GND}$	5.5	—	—	± 0.5	μA
Input leakage current	I_{IN}	$V_{IN} = V_{CC} \text{ or GND}$	5.5	—	—	± 0.1	μA
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC} \text{ or GND}$	5.5	—	—	4.0	μA
	I_{CCT}	Per input: $V_{IN} = 0.5\text{ V or } 2.4\text{ V}$ Other input: $V_{CC} \text{ or GND}$	5.5	—	0.4	1.4	mA

11.2. DC Characteristics (Unless otherwise specified, $T_a = -40\text{ to }85\text{ °C}$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit
High-level input voltage	V_{IH}	—	4.5 to 5.5	2.0	—	V
Low-level input voltage	V_{IL}	—	4.5 to 5.5	—	0.8	V
High-level output voltage	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20\text{ }\mu\text{A}$	4.5	4.4	V
			$I_{OH} = -6\text{ mA}$	4.5	4.13	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20\text{ }\mu\text{A}$	4.5	—	V
			$I_{OL} = 6\text{ mA}$	4.5	—	
3-state output OFF-state leakage current	I_{OZ}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = V_{CC} \text{ or GND}$	5.5	—	± 5.0	μA
Input leakage current	I_{IN}	$V_{IN} = V_{CC} \text{ or GND}$	5.5	—	± 1.0	μA
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC} \text{ or GND}$	5.5	—	40.0	μA
	I_{CCT}	Per input: $V_{IN} = 0.5\text{ V or } 2.4\text{ V}$ Other input: $V_{CC} \text{ or GND}$	5.5	—	1.7	mA

12. DC Characteristics (Unless otherwise specified, $T_a = -40$ to $125\text{ }^{\circ}\text{C}$)

Characteristics	Symbol	Test Condition		V _{CC} (V)	Min	Max	Unit
High-level input voltage	V _{IH}	—		4.5 to 5.5	2.0	—	V
Low-level input voltage	V _{IL}	—		4.5 to 5.5	—	0.8	V
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20 μA	4.5	4.4	—	V
			I _{OH} = -6 mA	4.5	3.7	—	V
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20 μA	4.5	—	0.1	V
			I _{OL} = 6 mA	4.5	—	0.4	V
3-state output OFF-state leakage current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		5.5	—	±10.0	μA
Input leakage current	I _{IN}	V _{IN} = 5.5 V or GND		5.5	—	±1.0	μA
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND		5.5	—	160.0	μA
	I _{CCT}	Per input: V _{IN} = 0.5 V or 2.4 V Other input: V _{CC} or GND		5.5	—	1.9	mA

12.1. AC Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$, Input: $t_r = t_f = 6\text{ ns}$)

Characteristics	Symbol	Note	Test Condition	C _L (pF)	V _{CC} (V)	Min	Typ.	Max	Unit
Output transition time	t _{TLH} , t _{THL}		—	50	4.5	—	7	12	ns
					5.5	—	6	11	
Propagation delay time	t _{PLH} , t _{PHL}		—	50	4.5	—	13	22	ns
					5.5	—	11	20	
				150	4.5	—	18	30	
					5.5	—	16	27	
3-state output enable time	t _{PZL} , t _{PZH}		R _L = 1 kΩ	50	4.5	—	19	30	ns
					5.5	—	16	27	
				150	4.5	—	24	38	
					5.5	—	22	34	
3-state output disable time	t _{PLZ} , t _{PHZ}		R _L = 1 kΩ	50	4.5	—	17	30	ns
					5.5	—	16	27	
Input capacitance	C _{IN}		DIR, \overline{G}			—	3	—	pF
Output capacitance	C _{OUT}		An, Bn			—	4	—	pF
Power dissipation capacitance	C _{PD}	(Note 1)	—			—	12	—	pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8 \text{ (per bit)}$$

12.2. AC Characteristics

(Unless otherwise specified, $T_a = -40\text{ to }85\text{ }^\circ\text{C}$, Input: $t_r = t_f = 6\text{ ns}$)

Characteristics	Symbol	Test Condition	C_L (pF)	V_{CC} (V)	Min	Max	Unit
Output transition time	t_{TLH}, t_{THL}	—	50	4.5	—	15	ns
				5.5	—	14	
Propagation delay time	t_{PLH}, t_{PHL}	—	50	4.5	—	28	ns
				5.5	—	25	
			150	4.5	—	38	
				5.5	—	34	
3-state output enable time	t_{PZL}, t_{PZH}	$R_L = 1\text{ k}\Omega$	50	4.5	—	38	ns
				5.5	—	34	
			150	4.5	—	48	
				5.5	—	43	
3-state output disable time	t_{PLZ}, t_{PHZ}	$R_L = 1\text{ k}\Omega$	50	4.5	—	38	ns
				5.5	—	34	

13. AC Characteristics
 (Unless otherwise specified, $T_a = -40$ to $125\text{ }^{\circ}\text{C}$, Input: $t_r = t_f = 6\text{ ns}$)

Characteristics	Symbol	Test Condition	C_L (pF)	V_{CC} (V)	Min	Max	Unit
Output transition time	t_{TLH}, t_{THL}	—	50	4.5	—	18	ns
				5.5	—	17	
Propagation delay time	t_{PLH}, t_{PHL}	—	50	4.5	—	33	
				5.5	—	30	
			150	4.5	—	45	ns
				5.5	—	41	
3-state output enable time	t_{PZL}, t_{PZH}	$R_L = 1\text{ k}\Omega$	50	4.5	—	45	ns
				5.5	—	41	
			150	4.5	—	57	
				5.5	—	51	
3-state output disable time	t_{PLZ}, t_{PHZ}	$R_L = 1\text{ k}\Omega$	50	4.5	—	45	ns
				5.5	—	41	

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