TOSHIBA Field-Effect Transistor Silicon P-Channel MOS Type (U-MOSVI)

# SSM3J334R

## Power Management Switch Applications

Unit: mm

•	Low ON-resistance: $R_{DS(ON)} = 71 \text{ m}\Omega \text{ (max) } (@V_{GS} = -10 \text{ V})$
	$R_{DS(ON)} = 105 \text{ m}\Omega \text{ (max) (@V_{GS} = -4.5 V)}$
	$R_{DS(ON)} = 136 \text{ m}\Omega \text{ (max) } (@V_{GS} = -4.0 \text{ V})$

## Absolute Maximum Ratings (Ta = 25°C)

Characteristic			ymbol	Rating	Unit	
Drain-Source voltage			DSS	-30	V	
Gate-Source voltage			'gss	± 20	<b>V</b>	
Drain current	DC	ID	(Note 1)	-4	Α	
Diam current	Pulse	I <sub>DP</sub> (Note 1,2)		-16	A	
Power dissipation			(Note 3)	1	W	
Fower dissipation			t < 10s	2	\ \v	
Channel temperature			T <sub>ch</sub>	150	°C	
Storage temperature range			T <sub>stg</sub>	-55 to 150	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the

Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

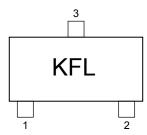
Note 1: The channel temperature should not exceed 150°C during use.

Note 2: PW ≤ 1ms, Duty ≤ 1%

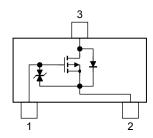
Note 3: Mounted on a FR4 board.

 $(25.4 \text{ mm} \times 25.4 \text{ mm} \times 1.6 \text{ mm}, \text{Cu Pad: } 645 \text{ mm}^2)$ 

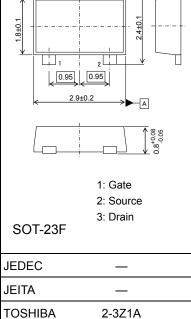
#### Marking



# **Equivalent Circuit (Top View)**



0.17 -0.08



Weight: 11 mg (typ.)

**⊕** 0.05 **M** A

Start of commercial production 2010-08

## **Electrical Characteristics (Ta = 25°C)**

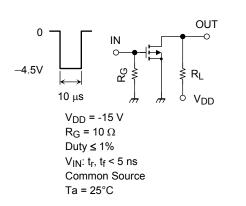
Chara	cteristic	Symbol	Test Conditions		Min	Тур.	Max	Unit
Drain-Source breakdown voltage		V <sub>(BR)DSS</sub>	I <sub>D</sub> = -10 mA, V <sub>GS</sub> = 0 V		-30	_	_	V
		V (BR) DSX	I <sub>D</sub> = -10 mA, V <sub>GS</sub> = 10 V	(Note 5)	-21	_	_	V
Drain cut-off curre	nt	I <sub>DSS</sub>	V <sub>DS</sub> = -30 V, V <sub>GS</sub> = 0 V		_	_	-1	μΑ
Gate leakage curr	ent	I <sub>GSS</sub>	V <sub>GS</sub> = ±16 V, V <sub>DS</sub> = 0 V		_	_	±10	μΑ
Gate threshold vo	Itage	V <sub>th</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -100 μA		-0.8	_	-2.0	V
Forward transfer a	admittance	Y <sub>fs</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1.0 A	(Note 4)	2.3	4.6	_	S
Drain-source ON-resistance		R <sub>DS</sub> (ON)	I <sub>D</sub> = -3.0 A, V <sub>GS</sub> = -10 V	(Note 4)	_	54	71	mΩ
			I <sub>D</sub> = -2.0 A, V <sub>GS</sub> = -4.5 V	(Note 4)	_	80	105	
			I <sub>D</sub> = -1.0 A, V <sub>GS</sub> = -4.0 V	(Note 4)	_	89	136	
Input capacitance		C <sub>iss</sub>			_	280	_	
Output capacitano	e	Coss	V <sub>DS</sub> = -15 V, V <sub>GS</sub> = 0 V f = 1 MHz		_	55	_	pF
Reverse transfer capacitance		C <sub>rss</sub>	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		_	40	_	
Custohing time	Turn-on time	t <sub>on</sub>	V <sub>DD</sub> = -15 V, I <sub>D</sub> = -1.0 A		_	13	_	20
Switching time	Turn-off time	t <sub>off</sub>	$V_{GS}$ = 0 to -4.5 V, $R_{G}$ = 10 $\Omega$		_	22	_	ns
Total Gate Charge		Qg			_	5.9	_	
Gate-Source Cha	rge	Q <sub>gs1</sub>	$V_{DD} = -15 \text{ V}, I_D = -4.0 \text{ A},$ $V_{GS} = -10 \text{ V}$		_	0.8	_	nC
Gate-Drain Charge		$Q_{gd}$	1 10 10 1		_	1.2	_	
Drain-Source forward voltage		$V_{DSF}$	I <sub>D</sub> = 4.0 A, V <sub>GS</sub> = 0 V	(Note 4)	_	0.9	1.2	V

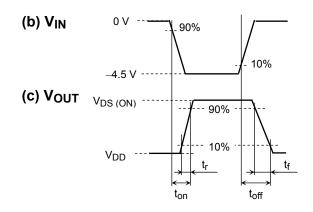
Note4: Pulse test

Note5: If a forward bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

# **Switching Time Test Circuit**

#### (a) Test Circuit





#### **Notice on Usage**

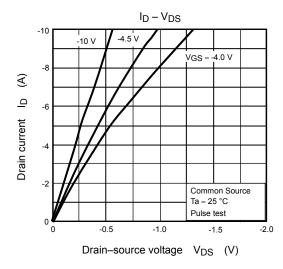
Let  $V_{th}$  be the voltage applied between gate and source that causes the drain current ( $I_D$ ) to be low (-100 $\mu$ A for the SSM3J334R). Then, for normal switching operation,  $V_{GS(on)}$  must be higher than  $V_{th}$ , and  $V_{GS(off)}$  must be lower than  $V_{th}$ . This relationship can be expressed as:  $V_{GS(off)} < V_{th} < V_{GS(on)}$ .

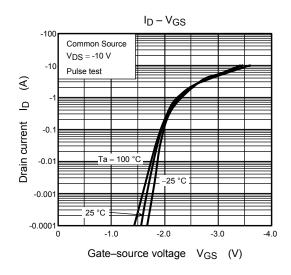
Take this into consideration when using the device.

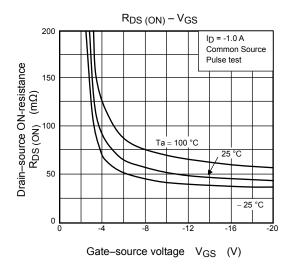
### **Handling Precaution**

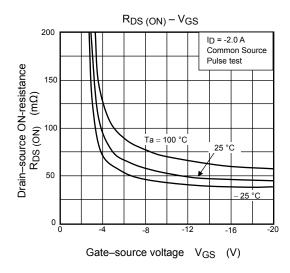
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

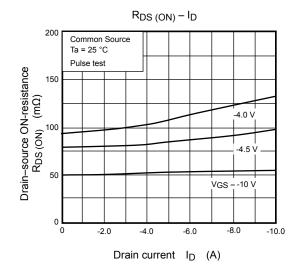
Thermal resistance  $R_{th\ (ch-a)}$  and power dissipation  $P_D$  vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration

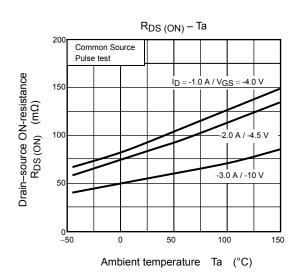


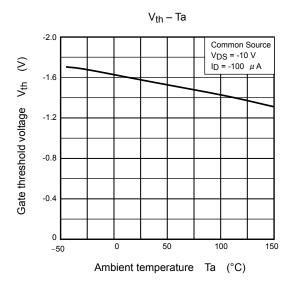


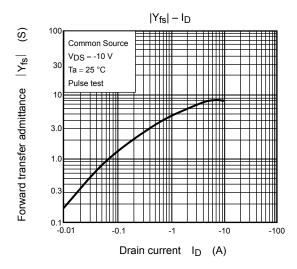


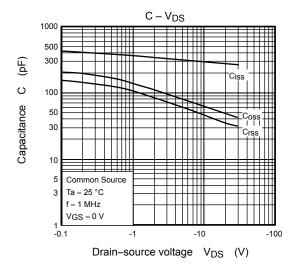


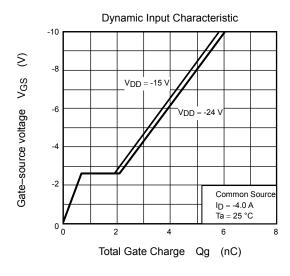


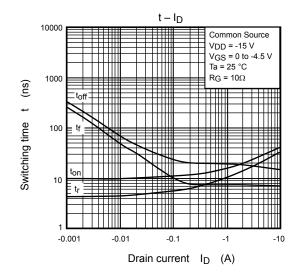


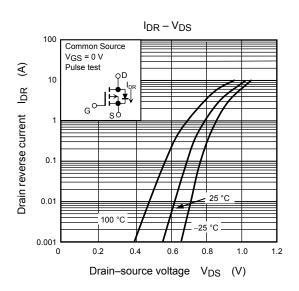




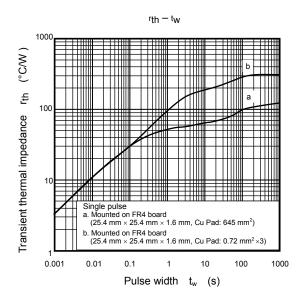


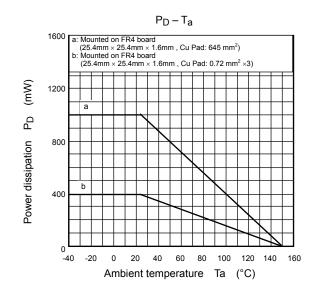






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