# 74ALVC164245

## 16-bit dual supply translating transceiver; 3-state

Rev. 05 — 13 April 2010 Product data sheet

## 1. General description

The 74ALVC164245 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74ALVC164245 is a 16-bit (dual octal) dual supply translating transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. It is designed to interface between a 3 V and 5 V bus in a mixed 3 V and 5 V supply environment.

This device can be used as two 8-bit transceivers or one 16-bit transceiver.

The direction control inputs (1DIR and 2DIR) determine the direction of the data flow. nDIR (active HIGH) enables data from nAn ports to nBn ports. nDIR (active LOW) enables data from nBn ports to nAn ports. The output enable inputs ($1\overline{OE}$ and $2\overline{OE}$), when HIGH, disable both nAn and nBn ports by placing them in a high-impedance OFF-state. Pins nAn, $n\overline{OE}$ and nDIR are referenced to $V_{CC(A)}$ and pins nBn are referenced to $V_{CC(B)}$.

In suspend mode, when one of the supply voltages is zero, there will be no current flow from the non-zero supply towards the zero supply. The nAn-outputs must be set 3-state and the voltage on the A-bus must be smaller than $V_{diode}$ (typical 0.7 V). $V_{CC(B)} \geq V_{CC(A)}$ (except in suspend mode).

## 2. Features and benefits

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range:
  - 3 V port ($V_{CC(A)}$): 1.5 V to 3.6 V
  - 5 V port ($V_{CC(B)}$): 1.5 V to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Control inputs voltage range from 2.7 V to 5.5 V
- Inputs accept voltages up to 5.5 V
- High-impedance outputs when $V_{CC(A)}$ or $V_{CC(B)}$ = 0 V
- Complies with JEDEC standard JESD8-B/JESD36
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from −40 °C to +85 °C and −40 °C to +125 °C

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Temperature range | Package | | |
|---|---|---|---|---|
| | | Name | Description | Version |
| 74ALVC164245DL | –40 °C to +125 °C | SSOP48 | plastic shrink small outline package; 48 leads; body width 7.5 mm | SOT370-1 |
| 74ALVC164245DGG | –40 °C to +125 °C | TSSOP48 | plastic thin shrink small outline package; 48 leads; body width 6.1 mm | SOT362-1 |
| 74ALVC164245BQ | –40 °C to +125 °C | HXQFN60U | plastic thermal enhanced extremely thin quad flat package; no leads; 60 terminals; UTLP based; body 4 × 6 × 0.5 mm | SOT1134-1 |

## 4. Functional diagram

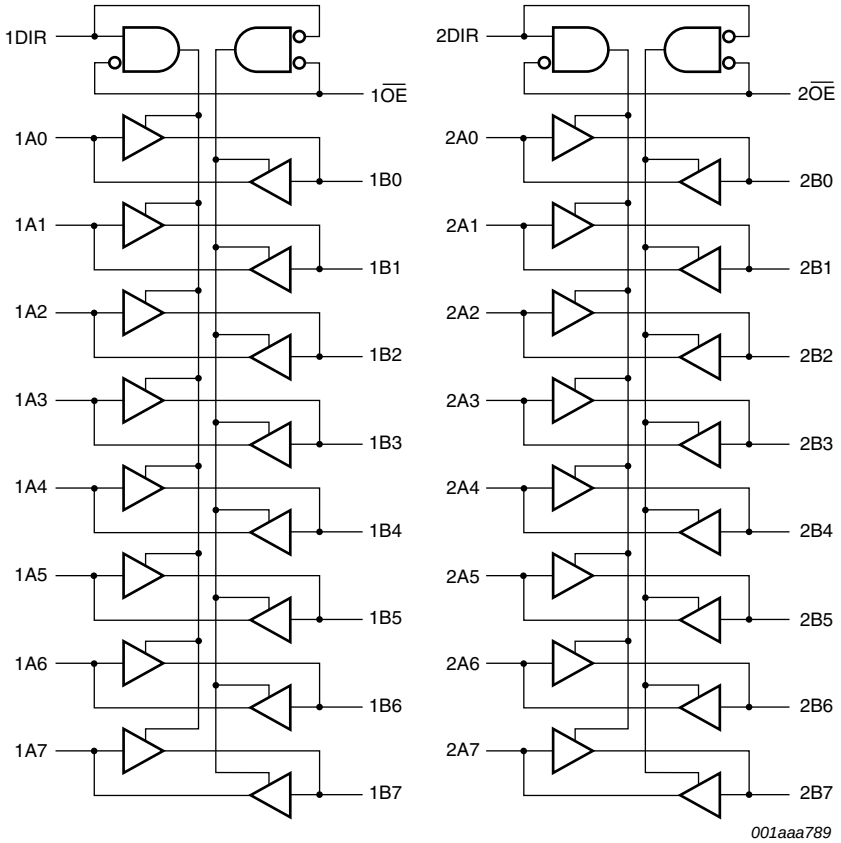



**Fig 1. Logic symbol**

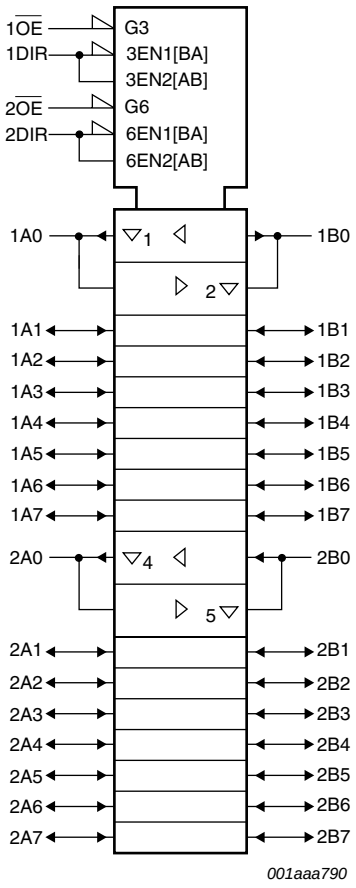



**Fig 2. IEC logic symbol**

# 5. Pinning information

## 5.1 Pinning

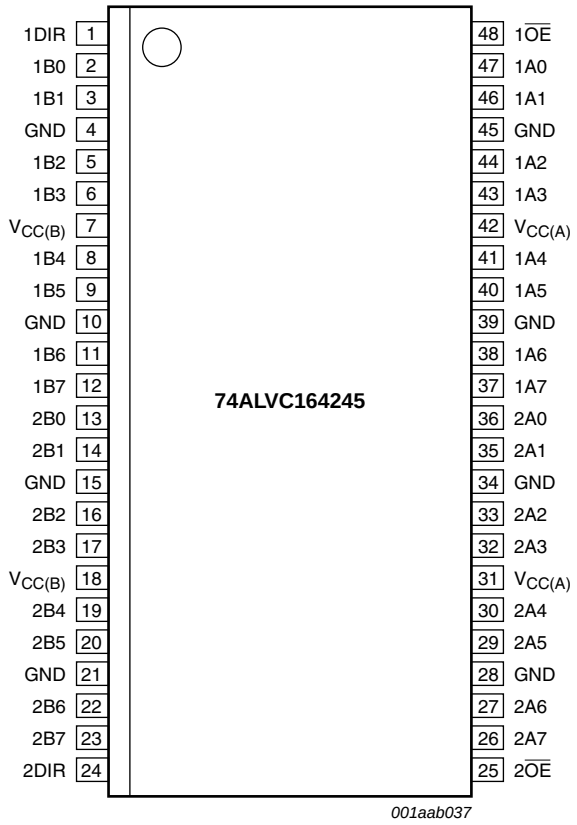
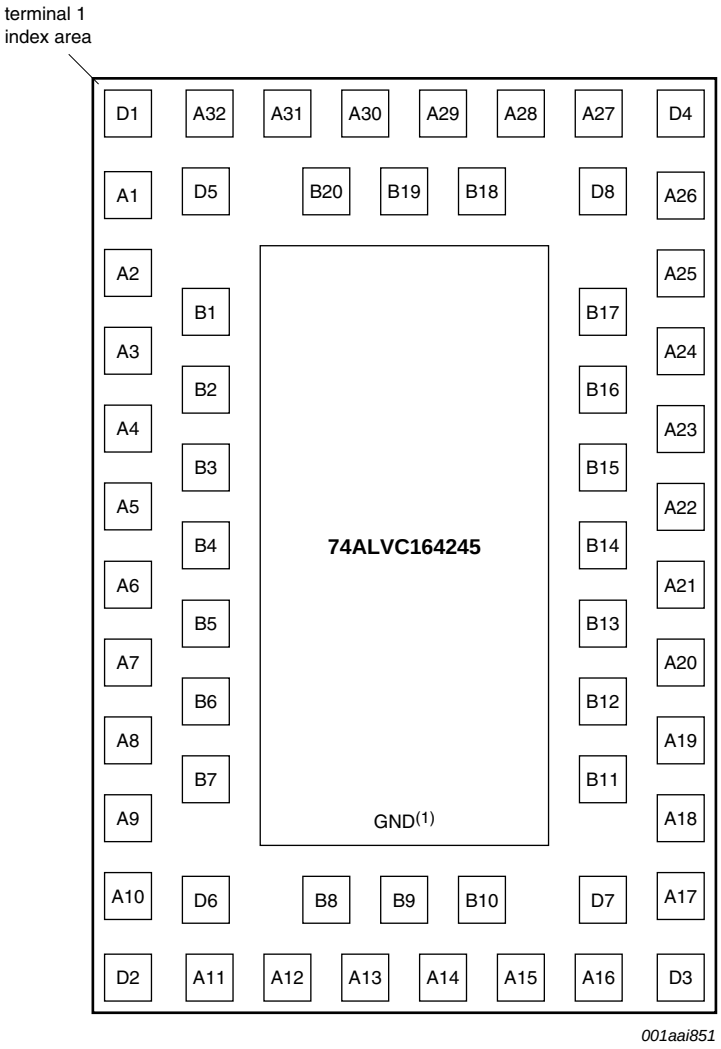



**Fig 3. Pin configuration SOT370-1 (SSOP48) and SOT362-1 (TSSOP48)**




Transparent top view

(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

**Fig 4. Pin configuration SOT1134-1 (HXQFN60U)**

### 5.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | | Description |
|---|---|---|---|
| | SOT370-1 and SOT362-1 | SOT1134-1 | |
| 1DIR, 2DIR | 1, 24 | A30, A13 | direction control input |
| 1B0 to 1B7 | 2, 3, 5, 6, 8, 9, 11, 12 | B20, A31, D5, D1, A2, B2, B3, A5 | data input/output |
| 2B0 to 2B7 | 13, 14, 16, 17, 19, 20, 22, 23 | A6, B5, B6, A9, D2, D6, A12, B8 | data input/output |
| GND | 4, 10, 15, 21, 28, 34, 39, 45 | A32, A3, A8, A11, A16, A19, A24, A27 | ground (0 V) |
| $V_{CC(B)}$ | 7, 18 | A1, A10, | supply voltage B (5 V bus) |
| $1\overline{OE}$, $2\overline{OE}$ | 48, 25 | A29, A14 | output enable input (active LOW) |
| 1A0 to 1A7 | 47, 46, 44, 43, 41, 40, 38, 37 | B18, A28, D8, D4, A25, B16, B15, A22 | data input/output |
| 2A0 to 2A7 | 36, 35, 33, 32, 30, 29, 27, 26 | A21, B13, B12, A18, D3, D7, A15, B10 | data input/output |
| $V_{CC(A)}$ | 31, 42 | A17, A26 | supply voltage A (3 V bus) |
| n.c. | - | A4, A7, A20, A23, B1, B4, B7, B9, B11, B14, B17, B19 | not connected |

## 6. Functional description

**Table 3. Function table[1]**

| Inputs | | Outputs | |
|---|---|---|---|
| $n\overline{OE}$ | nDIR | nAn | nBn |
| L | L | nAn = nBn | inputs |
| L | H | inputs | nBn = nAn |
| H | X | Z | Z |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V). See [1].*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC(B)}$ | supply voltage B | $V_{CC(B)} \geq V_{CC(A)}$ | | –0.5 | +6.0 | V |
| $V_{CC(A)}$ | supply voltage A | $V_{CC(B)} \geq V_{CC(A)}$ | | –0.5 | +4.6 | V |
| $I_{IK}$ | input clamping current | $V_I < 0$ V | | –50 | - | mA |
| $V_I$ | input voltage | | [2] | –0.5 | +6.0 | V |
| $V_{I/O}$ | input/output voltage | | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{OK}$ | output clamping current | $V_O > V_{CC}$ or $V_O < 0$ V | | - | ±50 | mA |
| $V_O$ | output voltage | output HIGH or LOW | [2] | –0.5 | $V_{CC}$ + 0.5 | V |
| | | output 3-state | [2] | –0.5 | +6.0 | V |
| $I_{O(sink/source)}$ | output sink or source current | $V_O$ = 0 V to $V_{CC}$ | | - | ±50 | mA |
| $I_{CC}$ | supply current | | | - | 100 | mA |

**Table 4. Limiting values** *...continued*

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V). See [1].*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{GND}$ | ground current | | | −100 | - | mA |
| $T_{stg}$ | storage temperature | | | −65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = −40 °C to +125 °C | | | | |
| | | (T)SSOP48 package | [3] | - | 500 | mW |
| | | HXQFN60U package | [4] | - | 1000 | mW |

[1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

[2] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[3] Above 60 °C the value of $P_{tot}$ derates linearly with 5.5 mW/K.

[4] Above 70 °C the value of $P_{tot}$ derates linearly with 1.8 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC(B)}$ | supply voltage B | $V_{CC(B)} \geq V_{CC(A)}$ | | | | |
| | | maximum speed performance | 2.7 | - | 5.5 | V |
| | | low-voltage applications | 1.5 | - | 5.5 | V |
| $V_{CC(A)}$ | supply voltage A | $V_{CC(B)} \geq V_{CC(A)}$ | | | | |
| | | maximum speed performance | 2.7 | - | 3.6 | V |
| | | low-voltage applications | 1.5 | - | 3.6 | V |
| $V_I$ | input voltage | control inputs: $n\overline{OE}$ and nDIR | 0 | - | 5.5 | V |
| $V_{I/O}$ | input/output voltage | nAn port | 0 | - | $V_{CC(A)}$ | V |
| | | nBn port | 0 | - | $V_{CC(B)}$ | V |
| $V_O$ | output voltage | nAn port | 0 | - | $V_{CC(A)}$ | V |
| | | nBn port | 0 | - | $V_{CC(B)}$ | V |
| $T_{amb}$ | ambient temperature | | −40 | - | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC(A)}$ = 2.7 V to 3.0 V | 0 | - | 20 | ns/V |
| | | $V_{CC(A)}$ = 3.0 V to 3.6 V | 0 | - | 10 | ns/V |
| | | $V_{CC(B)}$ = 3.0 V to 4.5 V | 0 | - | 20 | ns/V |
| | | $V_{CC(B)}$ = 4.5 V to 5.5 V | 0 | - | 10 | ns/V |

## 9. Static characteristics

**Table 6. Static characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | $T_{amb}$ = −40 °C to +85 °C | | | $T_{amb}$ = −40 °C to +125 °C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | Min | Typ[1] | Max | |
| $V_{IH}$ | HIGH-level input voltage | nBn port | | | | | | | | |
| | | $V_{CC(B)}$ = 3.0 V to 5.5 V | [2] | 2.0 | - | - | 2.0 | - | - | V |
| | | nAn port, $n\overline{OE}$ and nDIR | | | | | | | | |
| | | $V_{CC(A)}$ = 3.0 V to 3.6 V | | 2.0 | - | - | 2.0 | - | - | V |
| | | $V_{CC(A)}$ = 2.3 V to 2.7 V | [2] | 1.7 | - | - | 1.7 | - | - | V |
| $V_{IL}$ | LOW-level input voltage | nBn port | | | | | | | | |
| | | $V_{CC(B)}$ = 4.5 V to 5.5 V | [2] | - | - | 0.8 | - | - | 0.8 | V |
| | | $V_{CC(B)}$ = 3.0 V to 3.6 V | [2] | - | - | 0.7 | - | - | 0.7 | V |
| | | nAn port, $n\overline{OE}$ and nDIR | | | | | | | | |
| | | $V_{CC(A)}$ = 3.0 V to 3.6 V | | - | - | 0.8 | - | - | 0.8 | V |
| | | $V_{CC(A)}$ = 2.3 V to 2.7 V | [2] | - | - | 0.7 | - | - | 0.7 | V |
| $V_{OH}$ | HIGH-level output voltage | nBn port; $V_I = V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = −24 mA; $V_{CC(B)}$ = 4.5 V | | $V_{CC(B)}$ − 0.8 | - | - | $V_{CC(B)}$ − 1.2 | - | - | V |
| | | $I_O$ = −12 mA; $V_{CC(B)}$ = 4.5 V | | $V_{CC(B)}$ − 0.5 | - | - | $V_{CC(B)}$ − 0.8 | - | - | V |
| | | $I_O$ = −18 mA; $V_{CC(B)}$ = 3.0 V | | $V_{CC(B)}$ − 0.8 | - | - | $V_{CC(B)}$ − 1.0 | - | - | V |
| | | $I_O$ = −100 µA; $V_{CC(B)}$ = 3.0 V | | $V_{CC(B)}$ − 0.2 | $V_{CC(B)}$ | - | $V_{CC(B)}$ − 0.3 | $V_{CC(B)}$ | - | V |
| | | nAn port; $V_I = V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = −24 mA; $V_{CC(A)}$ = 3.0 V | | $V_{CC(A)}$ − 0.7 | - | - | $V_{CC(A)}$ − 1.0 | - | - | V |
| | | $I_O$ = −100 µA; $V_{CC(A)}$ = 3.0 V | | $V_{CC(A)}$ − 0.2 | - | - | $V_{CC(A)}$ − 0.3 | - | - | V |
| | | $I_O$ = −12 mA; $V_{CC(A)}$ = 2.7 V | | $V_{CC(A)}$ − 0.5 | - | - | $V_{CC(A)}$ − 0.8 | - | - | V |
| | | $I_O$ = −8 mA; $V_{CC(A)}$ = 2.3 V | | $V_{CC(A)}$ − 0.6 | - | - | $V_{CC(A)}$ − 0.6 | - | - | V |
| | | $I_O$ = −100 µA; $V_{CC(A)}$ = 2.3 V | | $V_{CC(A)}$ − 0.2 | $V_{CC(A)}$ | - | $V_{CC(A)}$ − 0.3 | $V_{CC(A)}$ | - | V |
| $V_{OL}$ | LOW-level output voltage | nBn port; $V_I = V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = 24 mA; $V_{CC(B)}$ = 4.5 V | | - | - | 0.55 | - | - | 0.60 | V |
| | | $I_O$ = 12 mA; $V_{CC(B)}$ = 4.5 V | | - | - | 0.40 | - | - | 0.80 | V |
| | | $I_O$ = 100 µA; $V_{CC(B)}$ = 4.5 V | | - | - | 0.20 | - | - | 0.30 | V |
| | | $I_O$ = 18 mA; $V_{CC(B)}$ = 3.0 V | | - | - | 0.55 | - | - | 0.80 | V |
| | | $I_O$ = 100 µA; $V_{CC(B)}$ = 3.0 V | | - | - | 0.20 | - | - | 0.30 | V |
| | | nAn port; $V_I = V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = 24 mA; $V_{CC(A)}$ = 3.0 V | | - | - | 0.55 | - | - | 0.80 | V |
| | | $I_O$ = 100 µA; $V_{CC(A)}$ = 3.0 V | | - | - | 0.20 | - | - | 0.30 | V |
| | | $I_O$ = 12 mA; $V_{CC(A)}$ = 2.7 V | | - | - | 0.40 | - | - | 0.60 | V |
| | | $I_O$ = 12 mA; $V_{CC(A)}$ = 2.3 V | | - | - | 0.60 | - | - | 0.60 | V |
| | | $I_O$ = 100 µA; $V_{CC(A)}$ = 2.3 V | | - | - | 0.20 | - | - | 0.20 | V |
| $I_I$ | input leakage current | $V_I$ = 5.5 V or GND | | - | ±0.1 | ±5 | - | ±0.1 | ±10 | µA |
| $I_{OZ}$ | OFF-state output current | $V_I = V_{IH}$ or $V_{IL}$; $V_O = V_{CC}$ or GND | [3] | - | ±0.1 | ±10 | - | ±0.1 | ±20 | µA |

**Table 6. Static characteristics** *...continued*

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | $T_{amb}$ = −40 °C to +85 °C | | | $T_{amb}$ = −40 °C to +125 °C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Typ[1] | Max | |
| $I_{CC}$ | supply current | $V_I = V_{CC}$ or GND; $I_O$ = 0 A | - | 0.1 | 40 | - | 0.1 | 80 | μA |
| $\Delta I_{CC}$ | additional supply current | per control pin; $V_I = V_{CC} - 0.6$ V; $I_O$ = 0 A [4] | - | 5 | 500 | - | 5 | 5000 | μA |
| $C_I$ | input capacitance | | - | 4.0 | - | - | - | - | pF |
| $C_{I/O}$ | input/output capacitance | nAn and nBn port | - | 5.0 | - | - | - | - | pF |

[1] All typical values are measured at $V_{CC(B)}$ = 5.0 V, $V_{CC(A)}$ = 3.3 V and $T_{amb}$ = 25 °C.

[2] If $V_{CC(A)}$ < 2.7 V, the switching levels at all inputs are not TTL compatible.

[3] For transceivers, the parameter $I_{OZ}$ includes the input leakage current.

[4] $V_{CC(A)}$ = 2.7 V to 3.6 V: other inputs at $V_{CC(A)}$ or GND; $V_{CC(B)}$ = 4.5 V to 5.5 V: other inputs at $V_{CC(B)}$ or GND.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L$ = 50 pF; for test circuit see Figure 7.*

| Symbol | Parameter | Conditions | $T_{amb}$ = −40 °C to +85 °C | | | $T_{amb}$ = −40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $t_{pd}$ | propagation delay | nAn to nBn; see Figure 5 [2] | | | | | | |
| | | $V_{CC(A)}$ = 2.3 V to 2.7 V; $V_{CC(B)}$ = 3.0 V to 3.6 V | 1.5 | 3.3 | 7.6 | 1.5 | 9.5 | ns |
| | | $V_{CC(A)}$ = 2.7 V; $V_{CC(B)}$ = 4.5 V to 5.5 V | 1.0 | 3.0 | 5.9 | 1.0 | 7.5 | ns |
| | | $V_{CC(A)}$ = 3.0 V to 3.6 V; $V_{CC(B)}$ = 4.5 V to 5.5 V | 1.0 | 2.9 | 5.8 | 1.0 | 7.5 | ns |
| | | nBn to nAn; see Figure 5 [2] | | | | | | |
| | | $V_{CC(A)}$ = 2.3 V to 2.7 V; $V_{CC(B)}$ = 3.0 V to 3.6 V | 1.0 | 3.0 | 7.6 | 1.0 | 9.5 | ns |
| | | $V_{CC(A)}$ = 2.7 V; $V_{CC(B)}$ = 4.5 V to 5.5 V | 1.0 | 4.3 | 6.7 | 1.0 | 8.5 | ns |
| | | $V_{CC(A)}$ = 3.0 V to 3.6 V; $V_{CC(B)}$ = 4.5 V to 5.5 V | 1.2 | 2.5 | 5.8 | 1.2 | 7.5 | ns |

**Table 7. Dynamic characteristics** *...continued*

*GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; for test circuit see Figure 7.*

| Symbol | Parameter | Conditions | | $T_{amb}$ = −40 °C to +85 °C | | | $T_{amb}$ = −40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | Min | Max | |
| $t_{en}$ | enable time | $n\overline{OE}$ to nBn; see Figure 6 | [2] | | | | | | |
| | | $V_{CC(A)}$ = 2.3 V to 2.7 V; $V_{CC(B)}$ = 3.0 V to 3.6 V | | 1.5 | 4.1 | 11.5 | 1.5 | 14.5 | ns |
| | | $V_{CC(A)}$ = 2.7 V; $V_{CC(B)}$ = 4.5 V to 5.5 V | | 1.5 | 3.6 | 9.2 | 1.5 | 11.5 | ns |
| | | $V_{CC(A)}$ = 3.0 V to 3.6 V; $V_{CC(B)}$ = 4.5 V to 5.5 V | | 1.0 | 3.2 | 8.9 | 1.0 | 12.0 | ns |
| | | $n\overline{OE}$ to nAn; see Figure 6 | [2] | | | | | | |
| | | $V_{CC(A)}$ = 2.3 V to 2.7 V; $V_{CC(B)}$ = 3.0 V to 3.6 V | | 1.5 | 4.6 | 12.3 | 1.5 | 15.5 | ns |
| | | $V_{CC(A)}$ = 2.7 V; $V_{CC(B)}$ = 4.5 V to 5.5 V | | 1.5 | 4.3 | 9.3 | 1.5 | 12.0 | ns |
| | | $V_{CC(A)}$ = 3.0 V to 3.6 V; $V_{CC(B)}$ = 4.5 V to 5.5 V | | 1.0 | 3.2 | 8.9 | 1.0 | 11.5 | ns |
| $t_{dis}$ | disable time | $n\overline{OE}$ to nBn; see Figure 6 | [2] | | | | | | |
| | | $V_{CC(A)}$ = 2.3 V to 2.7 V; $V_{CC(B)}$ = 3.0 V to 3.6 V | | 2.0 | 2.7 | 10.5 | 2.0 | 13.5 | ns |
| | | $V_{CC(A)}$ = 2.7 V; $V_{CC(B)}$ = 4.5 V to 5.5 V | | 2.5 | 4.6 | 9.0 | 2.5 | 11.5 | ns |
| | | $V_{CC(A)}$ = 3.0 V to 3.6 V; $V_{CC(B)}$ = 4.5 V to 5.5 V | | 2.1 | 4.9 | 8.6 | 2.1 | 11.0 | ns |
| | | $n\overline{OE}$ to nAn; see Figure 6 | [2] | | | | | | |
| | | $V_{CC(A)}$ = 2.3 V to 2.7 V; $V_{CC(B)}$ = 3.0 V to 3.6 V | | 1.0 | 2.7 | 9.3 | 1.0 | 12.0 | ns |
| | | $V_{CC(A)}$ = 2.7 V; $V_{CC(B)}$ = 4.5 V to 5.5 V | | 1.5 | 3.5 | 9.0 | 1.5 | 11.5 | ns |
| | | $V_{CC(A)}$ = 3.0 V to 3.6 V; $V_{CC(B)}$ = 4.5 V to 5.5 V | | 2.0 | 3.2 | 8.6 | 2.0 | 11.0 | ns |

**Table 7. Dynamic characteristics** *...continued*

*GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L$ = 50 pF; for test circuit see Figure 7.*

| Symbol | Parameter | Conditions | $T_{amb}$ = −40 °C to +85 °C | | | $T_{amb}$ = −40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $C_{PD}$ | power dissipation capacitance | 5 V port: nAn to nBn; $V_{CC(B)}$ = 5 V; $V_{CC(A)}$ = 3.3 V [3][4] | | | | | | |
| | | outputs enabled | - | 30 | - | - | - | pF |
| | | outputs disabled | - | 15 | - | - | - | pF |
| | | 3 V port: nBn to nAn; $V_{CC(B)}$ = 5 V; $V_{CC(A)}$ = 3.3 V [3][4] | | | | | | |
| | | outputs enabled | - | 40 | - | - | - | pF |
| | | outputs disabled | - | 5 | - | - | - | pF |

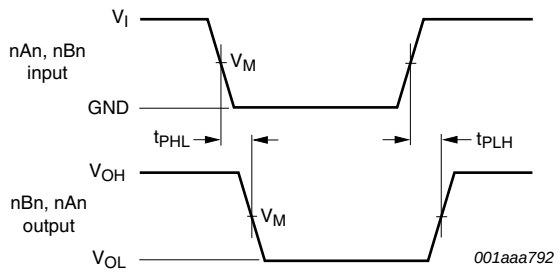
[1] All typical values are measured at nominal voltage for $V_{CC(B)}$ and $V_{CC(A)}$ and at $T_{amb}$ = 25 °C.

[2] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.
$t_{en}$ is the same as $t_{PZL}$ and $t_{PZH}$.
$t_{dis}$ is the same as $t_{PLZ}$ and $t_{PHZ}$.

[3] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz;
$f_o$ = output frequency in MHz;
$C_L$ = output load capacitance in pF;
$V_{CC}$ = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

[4] The condition is $V_I$ = GND to $V_{CC}$.

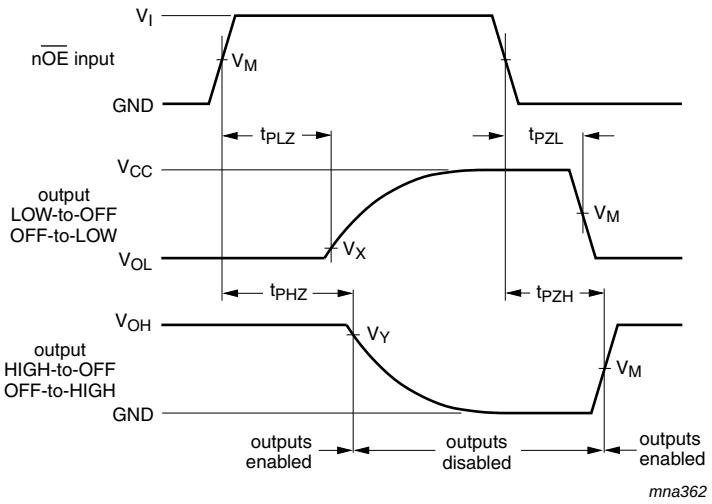
## 11. AC waveforms




Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig 5. Input (nAn, nBn) to output (nBn, nAn) propagation delays**



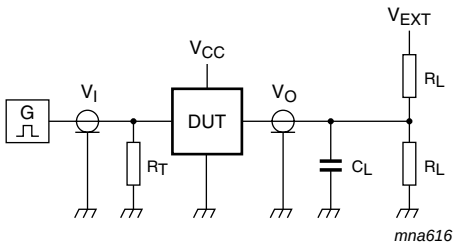

Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with output load.

**Fig 6. 3-state enable and disable times**

**Table 8. Measurement points**

| Direction | Supply voltage | | Input | | Output | | |
|---|---|---|---|---|---|---|---|
| | $V_{CC(A)}$ | $V_{CC(B)}$ | $V_I$ | $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| nAn port to nBn port | 2.3 V to 2.7 V | 2.7 V to 3.6 V | $V_{CC(A)}$ | $0.5 \times V_{CC(A)}$ | 1.5 V | $V_{OL(B)}$ + 0.3 V | $V_{OH(B)}$ − 0.3 V |
| nBn port to nAn port | 2.3 V to 2.7 V | 2.7 V to 3.6 V | 2.7 V | 1.5 V | $0.5 \times V_{CC(A)}$ | $V_{OL(A)}$ + 0.15 V | $V_{OH(A)}$ − 0.15 V |
| nAn port to nBn port | 2.7 V to 3.6 V | 4.5 V to 5.5 V | 2.7 V | 1.5 V | $0.5 \times V_{CC(B)}$ | $0.2 \times V_{CC(B)}$ | $0.8 \times V_{CC(B)}$ |
| nBn port to nAn port | 2.7 V to 3.6 V | 4.5 V to 5.5 V | 3.0 V | 1.5 V | 1.5 V | $V_{OL(A)}$ + 0.3 V | $V_{OH(A)}$ − 0.3 V |




Test data is given in Table 9.

Definitions for test circuit:

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_L$ = Load resistance.

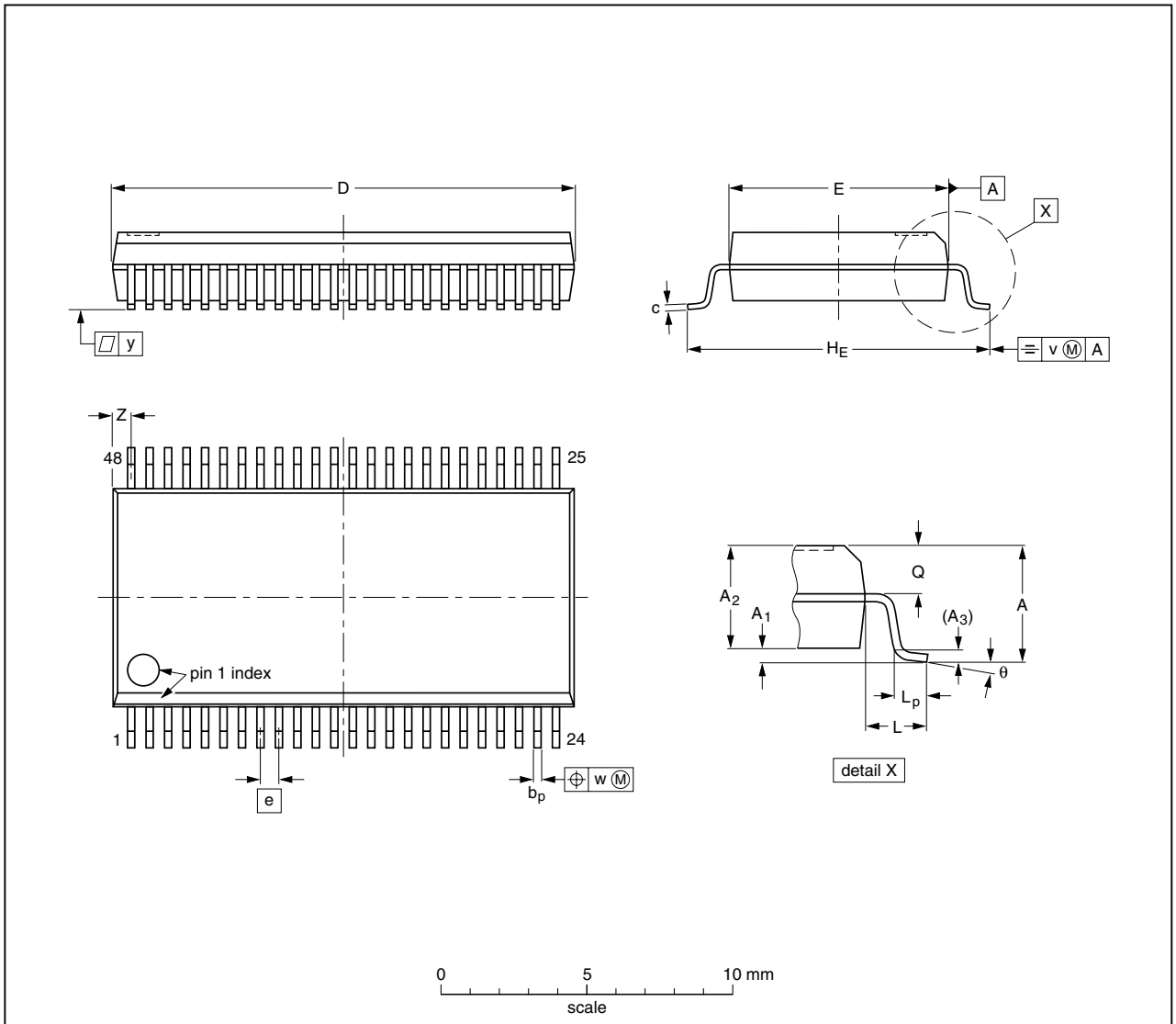
**Fig 7. Load circuitry for switching times**

**Table 9. Test data**

| Direction | Supply voltage | | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|
| | $V_{CC(A)}$ | $V_{CC(B)}$ | $C_L$ | $R_L$ | $t_{PLH}$, $t_{PHL}$ | $t_{PZH}$, $t_{PHZ}$ | $t_{PZL}$, $t_{PLZ}$ |
| nAn port to nBn port | 2.3 V to 2.7 V | 2.7 V to 3.6 V | 50 pF | 500 Ω | open | GND | $2 \times V_{CC}$ |
| nBn port to nAn port | 2.3 V to 2.7 V | 2.7 V to 3.6 V | 50 pF | 500 Ω | open | GND | 6.0 V |
| nAn port to nBn port | 2.7 V to 3.6 V | 4.5 V to 5.5 V | 50 pF | 500 Ω | open | GND | $2 \times V_{CC}$ |
| nBn port to nAn port | 2.7 V to 3.6 V | 4.5 V to 5.5 V | 50 pF | 500 Ω | open | GND | 6.0 V |

## 12. Package outline

**SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm** **SOT370-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.8 | 0.4<br>0.2 | 2.35<br>2.20 | 0.25 | 0.3<br>0.2 | 0.22<br>0.13 | 16.00<br>15.75 | 7.6<br>7.4 | 0.635 | 10.4<br>10.1 | 1.4 | 1.0<br>0.6 | 1.2<br>1.0 | 0.25 | 0.18 | 0.1 | 0.85<br>0.40 | 8°<br>0° |

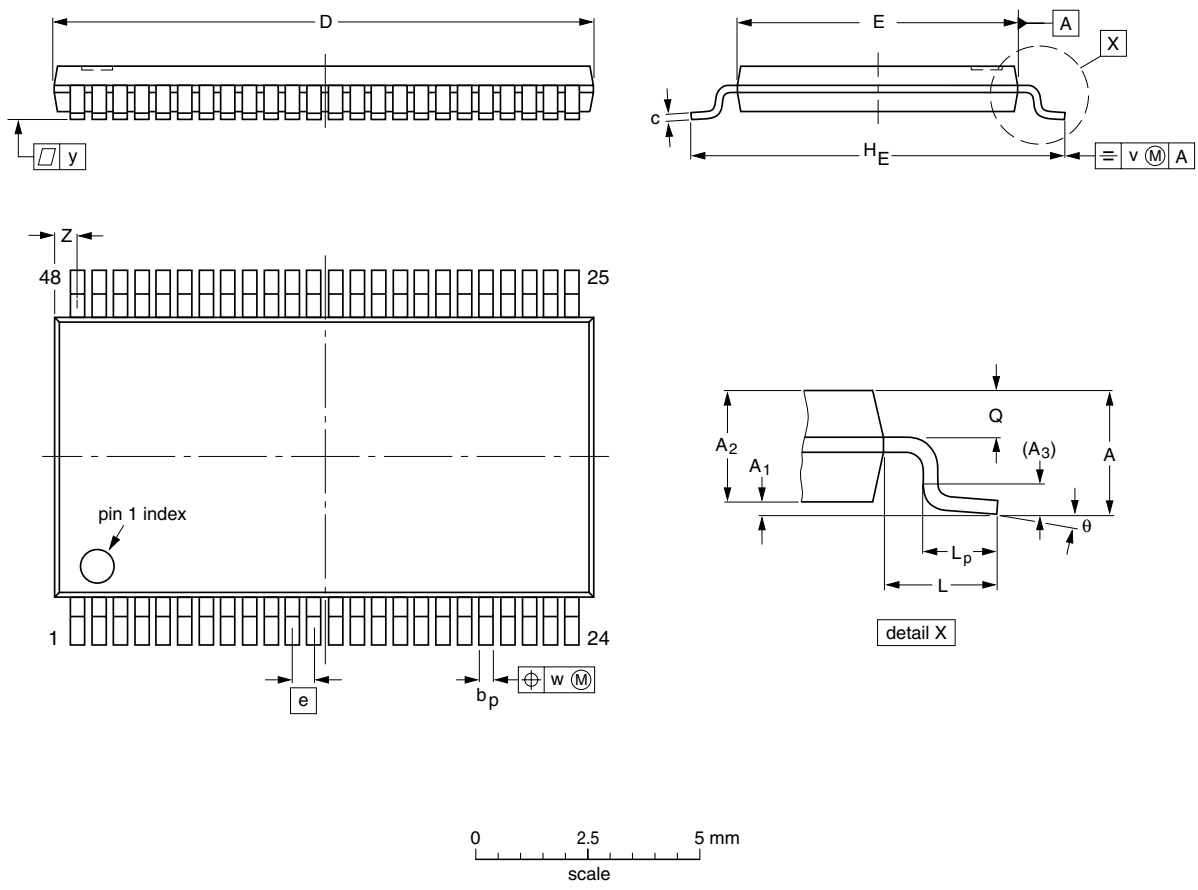
**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT370-1 | | MO-118 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 8. Package outline SOT370-1 (SSOP48)**

**TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm** **SOT362-1**




**DIMENSIONS (mm are the original dimensions).**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.2 | 0.15<br>0.05 | 1.05<br>0.85 | 0.25 | 0.28<br>0.17 | 0.2<br>0.1 | 12.6<br>12.4 | 6.2<br>6.0 | 0.5 | 8.3<br>7.9 | 1 | 0.8<br>0.4 | 0.50<br>0.35 | 0.25 | 0.08 | 0.1 | 0.8<br>0.4 | $8^{o}$<br>$0^{o}$ |

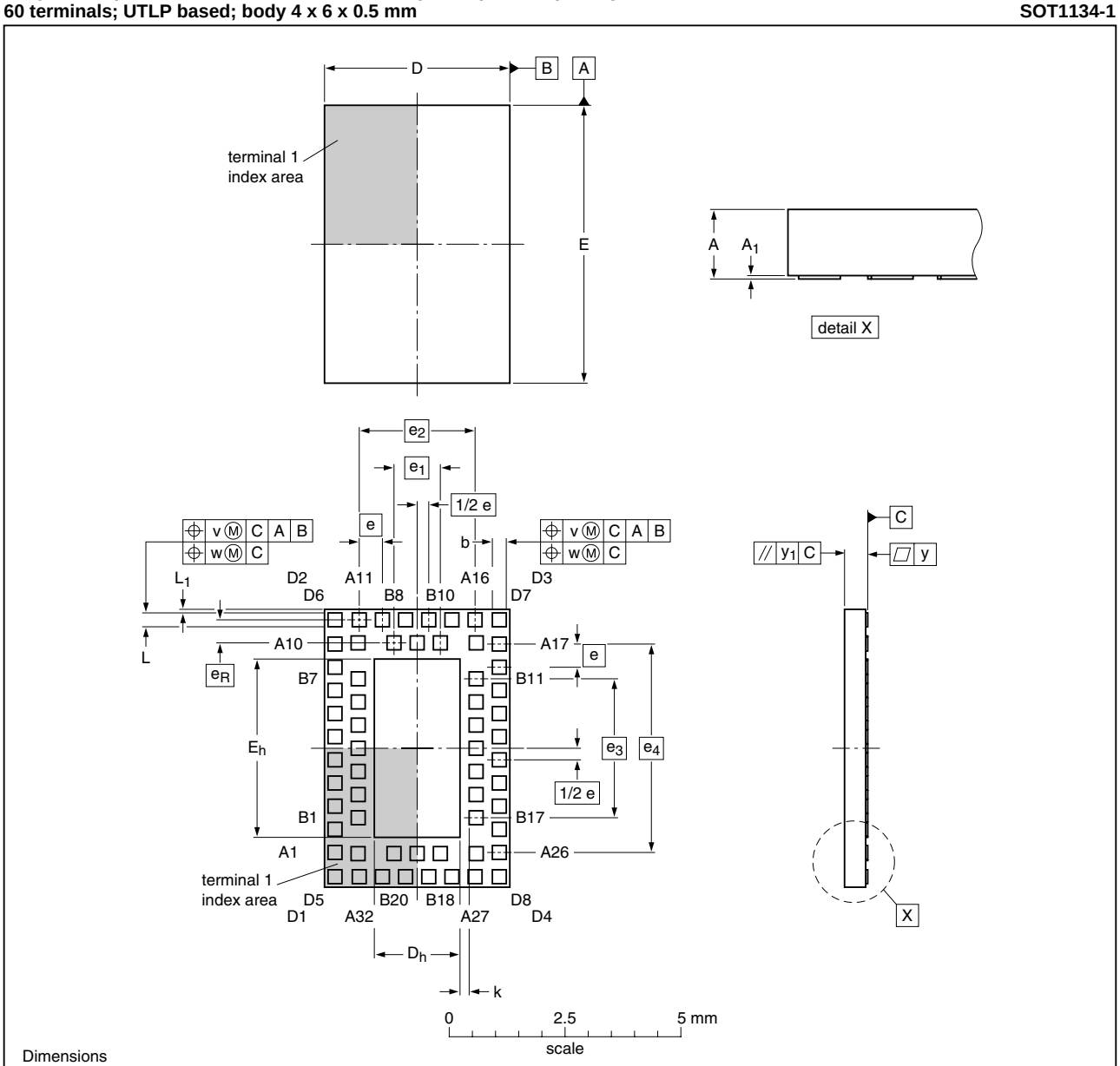
**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT362-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 9. Package outline SOT362-1 (TSSOP48)**

**HXQFN60U: plastic thermal enhanced extremely thin quad flat package; no leads; 60 terminals; UTLP based; body 4 x 6 x 0.5 mm** **SOT1134-1**




Dimensions

| Unit | | A | $A_1$ | b | D | $D_h$ | E | $E_h$ | e | $e_1$ | $e_2$ | $e_3$ | $e_4$ | eR | k | L | $L_1$ | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | max | 0.50 | 0.05 | 0.35 | 4.1 | 1.90 | 6.1 | 3.90 | | | | | | | 0.25 | 0.35 | 0.125 | | | | |
| mm | nom | 0.48 | 0.02 | 0.30 | 4.0 | 1.85 | 6.0 | 3.85 | 0.5 | 1 | 2.5 | 3 | 4.5 | 0.5 | 0.20 | 0.30 | 0.075 | 0.07 | 0.05 | 0.08 | 0.1 |
| | min | 0.46 | 0.00 | 0.25 | 3.9 | 1.80 | 5.9 | 3.80 | | | | | | | 0.15 | 0.25 | 0.025 | | | | |

*sot1134-1_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1134-1 | - - - | - - - | - - - | | | ~~08-12-17~~ 09-01-22 |

**Fig 10. Package outline SOT1134-1 (HXQFN60U)**

## 13. Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

## 14. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74ALVC164245_5 | 20100413 | Product data sheet | - | 74ALVC164245_4 |
| Modifications: | • 74ALVC164245BQ changed from HUQFN60U (SOT1025-1) to HXQFN60U (SOT1134-1) package. | | | |
| 74ALVC164245_4 | 20081111 | Product data sheet | - | 74ALVC164245_3 |
| Modifications: | • Added type number 74ALVC164245 (HUQFN60U package) | | | |
| 74ALVC164245_3 | 20040914 | Product data sheet | - | 74ALVC164245_2 |
| 74ALVC164245_2 | 20040601 | Product data sheet | - | 74ALVC164245_1 |
| 74ALVC164245_1 | 19980826 | Product specification | - | - |

# 15. Legal information

## 15.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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**Document identifier: 74ALVC164245_5**