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Kind regards,

Team Nexperia

# DATA SHEET

## **74ALVCH16543**

**16-bit D-type registered  
transceiver; 3-state**

Product specification  
Supersedes data of 1998 Aug 31  
File under Integrated Circuits, IC24

1999 Nov 23

**16-bit D-type registered transceiver; 3-state****74ALVCH16543****FEATURES**

- In accordance with JEDEC standard no 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- MULTIBYTE™ flow-through pin-out architecture
- 16-bit transceiver with D-type latch
- Combines 16245 and 16373 type functions in one chip
- Back-to-back registers for storage
- Output drive capability 50  $\Omega$  transmission lines at 85 °C
- Separate controls for data flow in each direction
- All data inputs have bus hold
- 3-state non-inverting outputs for bus oriented applications
- Current drive  $\pm 24$  mA at 3.0 V.

Separate latch enable ( $n\overline{LE}_{AB}$ ,  $n\overline{LE}_{BA}$ ) and output enable ( $n\overline{OE}_{AB}$ ,  $n\overline{OE}_{BA}$ ) inputs are provided for each register to permit independent control in either direction of the data flow.

The '16543' contains two sections each consisting of two sets of eight D-type latches with separate inputs and controls for each set. For data flow from A to B, for example, the A-to-B enable ( $n\overline{E}_{AB}$ , where n equals 1 or 2) inputs must be LOW in order to enter data from  $nA_0$  to  $nA_7$ , or take data from  $nB_0$  to  $nB_7$ , as indicated in the function table. With  $n\overline{E}_{AB}$  LOW, a LOW signal on the A-to-B latch enable ( $n\overline{LE}_{AB}$ ) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the  $n\overline{LE}_{AB}$  signal stores the A data into the latches. With  $n\overline{E}_{AB}$  and  $n\overline{OE}_{AB}$  both LOW, the 3-state B output buffers are active and display the data present at the output of the A latches. Similarly, the  $n\overline{E}_{BA}$ ,  $n\overline{LE}_{BA}$  and  $n\overline{OE}_{BA}$  signals control the data flow from B-to-A.

Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

**DESCRIPTION**

The 74ALVCH16543 is a dual octal registered transceiver. Each section contains two sets of D-type latches for temporary storage of the data flow in either direction.

**FUNCTION TABLE**

See note 1.

INPUTS				OUTPUTS	STATUS
$n\overline{OE}_{XX}$	$n\overline{E}_{XX}$	$n\overline{LE}_{XX}$	$nB_n, nA_n$		
H	X	X	X	Z	disabled
X	H	X	X	Z	disabled
L	$\uparrow$	L	h	Z	disabled and latch
L	$\uparrow$	L	l	Z	
L	L	$\uparrow$	h	H	latch and display
L	L	$\uparrow$	l	L	
L	L	L	H	H	transparent
L	L	L	L	L	
L	L	H	X	NC	hold

**Note**

1. XX = AB for A-to-B direction, BA for B-to-A direction;  
H = HIGH voltage level; L = LOW voltage level;  
h = HIGH state must be present one set-up time before the LOW-to-HIGH transition of  $n\overline{LE}_{AB}$ ,  $n\overline{LE}_{BA}$ ,  $n\overline{E}_{AB}$  or  $n\overline{E}_{BA}$ ;  
l = LOW state must be present one set-up time before the LOW-to-HIGH transition of  $n\overline{LE}_{AB}$ ,  $n\overline{LE}_{BA}$ ,  $n\overline{E}_{AB}$  or  $n\overline{E}_{BA}$ ;  
X = don't care; NC = no change;  
 $\uparrow$  = LOW-to-HIGH level transition;  
Z = high-impedance OFF-state.

## 16-bit D-type registered transceiver; 3-state

74ALVCH16543

## QUICK REFERENCE DATA

Ground = 0;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 2.5\text{ ns}$ 

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	propagation delay $nA_n$ , $nB_n$ to $nB_n$ , $nA_n$	$C_L = 50\text{ pF}$ ; $V_{CC} = 3.3\text{ V}$	3.8	ns
$C_I$	input capacitance		4.0	pF
$C_{PD}$	power dissipation capacitance per latch	notes 1 and 2		
		outputs enabled	44	pF
		outputs disabled	14	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$
 $f_i$  = input frequency in MHz;

 $C_L$  = output load capacitance in pF;

 $f_o$  = output frequency in MHz;

 $V_{CC}$  = supply voltage in Volts;

 $\Sigma (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

2. The condition is  $V_I = \text{GND to } V_{CC}$ .

## ORDERING INFORMATION

OUTSIDE NORTH AMERICA	NORTH AMERICA	PACKAGE				
		TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74ALVCH16543DGG	ACH16543 DGG	-40 to +85 $^{\circ}\text{C}$	56	TSSOP	plastic	SOT364-1

## PINNING

PIN	SYMBOL	DESCRIPTION
1 and 28	$1\overline{OE}_{AB}$ , $2\overline{OE}_{AB}$	output enable A-to-B for register 1 or 2
2 and 27	$1\overline{LE}_{AB}$ , $2\overline{LE}_{AB}$	latch enable A-to-B for register 1 or 2
3 and 26	$1\overline{E}_{AB}$ , $2\overline{E}_{AB}$	A-to-B enable for register 1 or 2
4, 11, 18, 25, 32, 39, 46 and 53	GND	ground (0 V)
5, 6, 8, 9, 10, 12, 13 and 14	$1A_0$ to $1A_7$	data inputs/outputs
7, 22, 35 and 50	$V_{CC}$	DC supply voltage
15, 16, 17, 19, 20, 21, 23 and 24	$2A_0$ to $2A_7$	data inputs/outputs
29 and 56	$2\overline{OE}_{BA}$ , $1\overline{OE}_{BA}$	output enable B-to-A for register 1 or 2
30 and 55	$2\overline{LE}_{BA}$ , $1\overline{LE}_{BA}$	latch enable B-to-A for register 1 or 2
31 and 54	$2\overline{E}_{BA}$ , $1\overline{E}_{BA}$	B-to-A enable for register 1 or 2
33, 34, 36, 37, 38, 40, 41 and 42	$2B_7$ to $2B_0$	data inputs/outputs
43, 44, 45, 47, 48, 49, 51 and 52	$1B_7$ to $1B_0$	data inputs/outputs

16-bit D-type registered transceiver; 3-state

74ALVCH16543

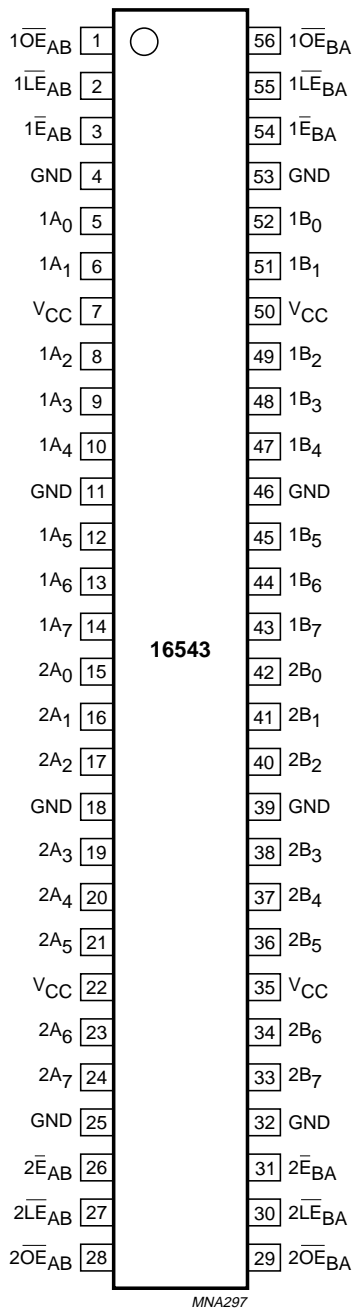


Fig.1 Pin configuration.

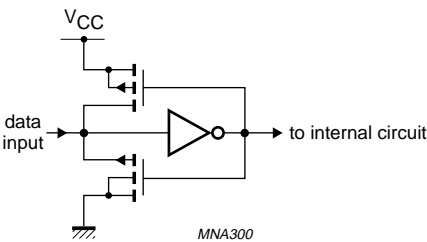
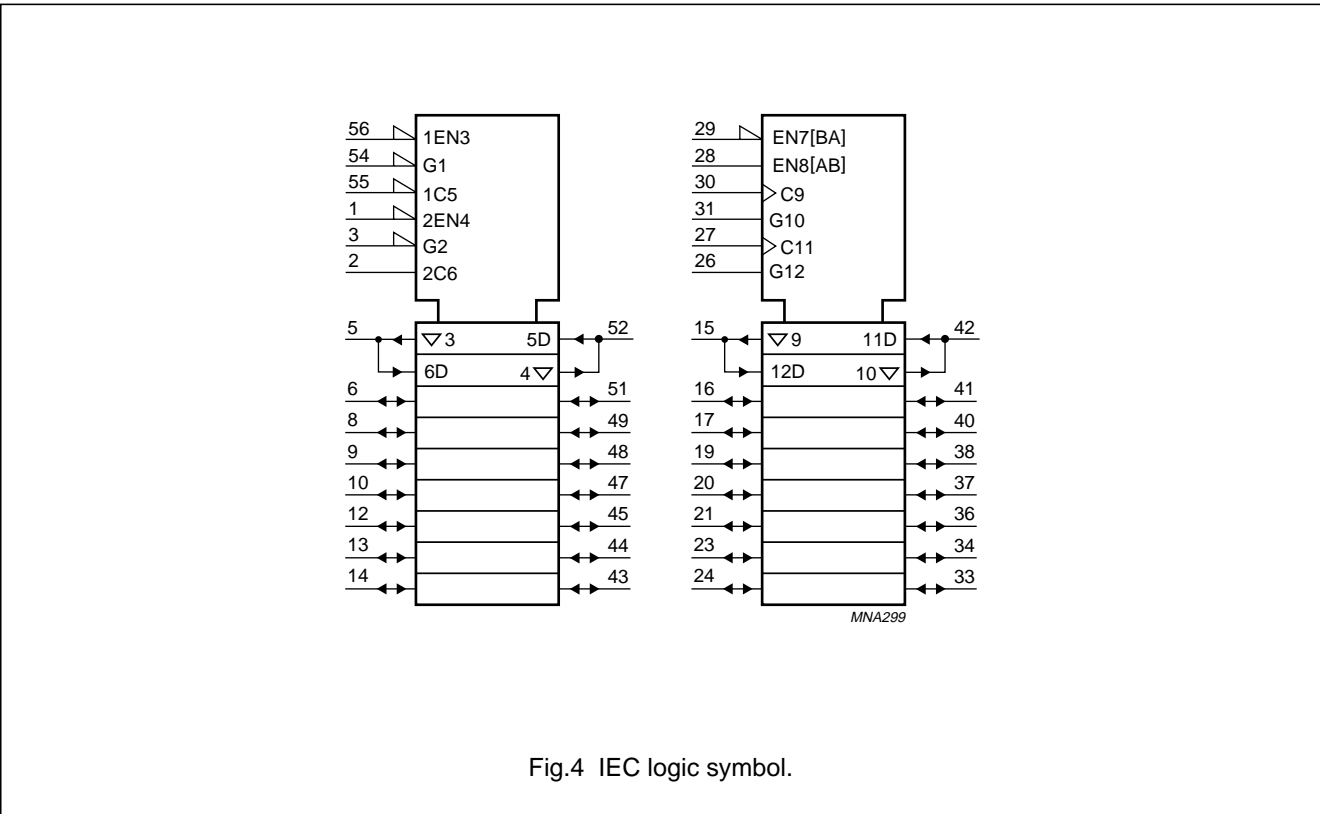
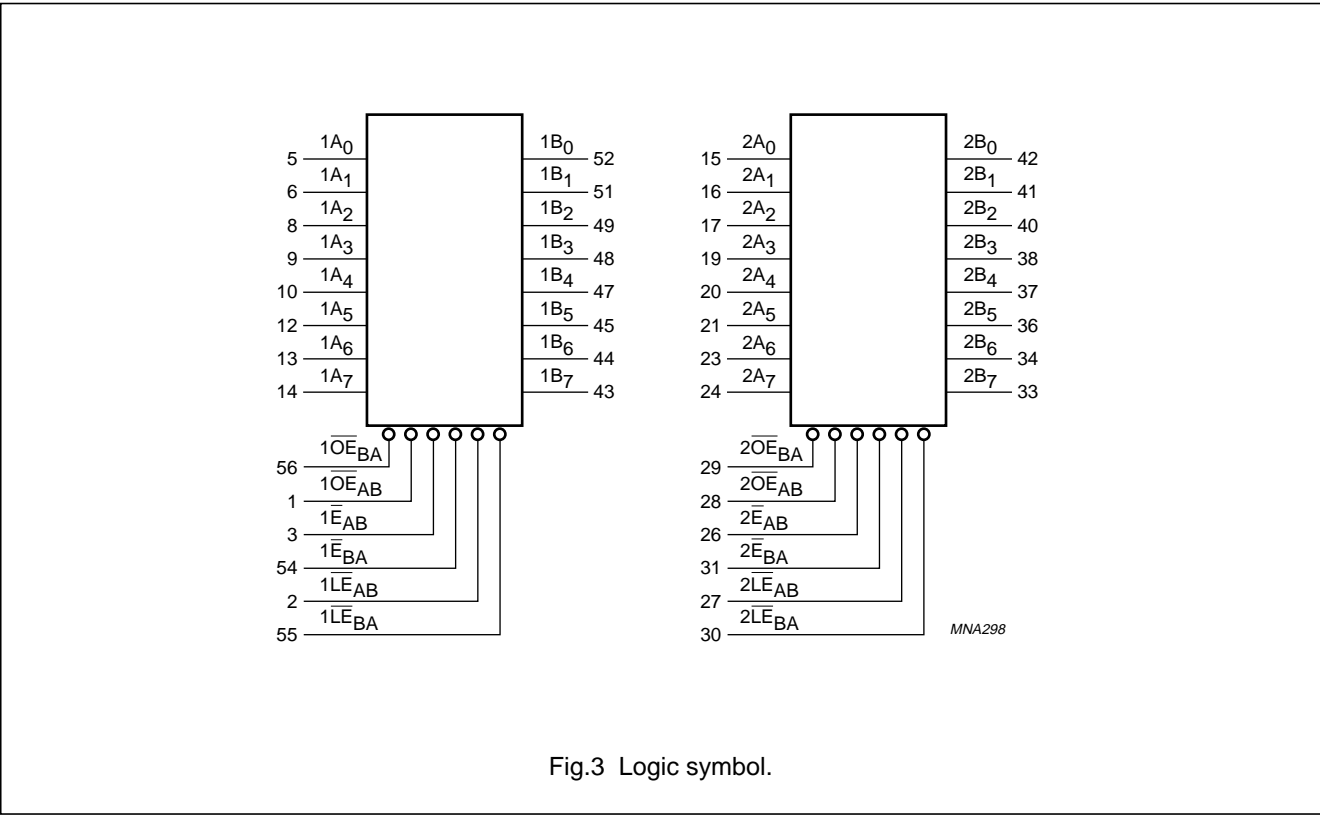


Fig.2 Bus hold circuit.

16-bit D-type registered transceiver; 3-state

74ALVCH16543



## 16-bit D-type registered transceiver; 3-state

74ALVCH16543

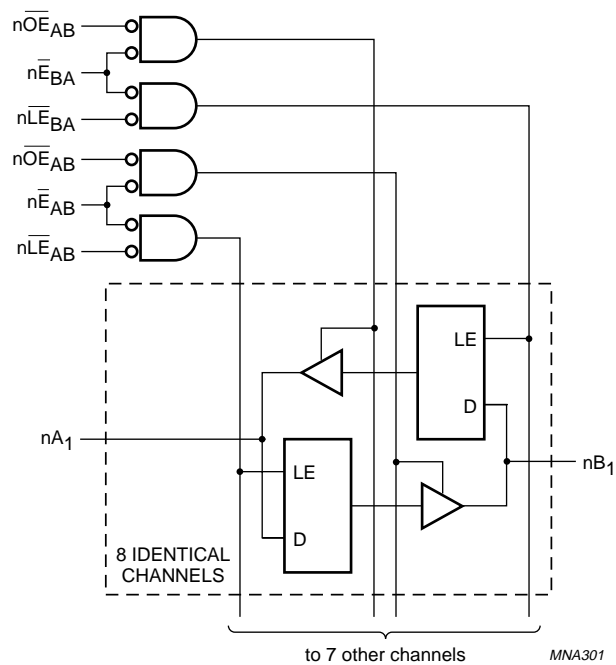


Fig.5 Logic diagram (one section).

## 16-bit D-type registered transceiver; 3-state

## 74ALVCH16543

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CC}$	DC supply voltage					
	for maximum speed performance	$C_L = 30 \text{ pF}$	2.3	2.5	2.7	V
	for maximum speed performance	$C_L = 50 \text{ pF}$	3.0	3.3	3.6	V
	for low-voltage applications		1.2	2.4	3.6	V
$V_I$	DC input voltage		0	–	$V_{CC}$	V
$V_O$	DC output voltage		0	–	$V_{CC}$	V
$T_{amb}$	operating ambient temperature	in free air	–40	–	+85	°C
$t_r, t_f$	input rise and fall times	$V_{CC} = 2.3 \text{ to } 3.0 \text{ V}$	0	–	20	ns/V
		$V_{CC} = 3.0 \text{ to } 3.6 \text{ V}$	0	–	10	ns/V

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	DC supply voltage		–0.5	+4.6	V
$I_{IK}$	DC input diode current	$V_I < 0$	–	–50	mA
$V_I$	DC input voltage	note 1	–0.5	+4.6	V
$I_{OK}$	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	–	±50	mA
$V_O$	DC output voltage	note 1	–0.5	$V_{CC} + 0.5$	V
$I_O$	DC output source or sink current	$V_O = 0 \text{ to } V_{CC}$	–	±50	mA
$I_{CC}, I_{GND}$	DC $V_{CC}$ or GND current		–	±100	mA
$T_{stg}$	storage temperature		–65	+150	°C
$P_{tot}$	power dissipation	for temperature range: –40 to +125 °C; note 2	–	600	mW

## Note

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 55 °C the value of  $P_{tot}$  derates linearly with 8 mW/K.



## 16-bit D-type registered transceiver; 3-state

## 74ALVCH16543

## DC CHARACTERISTICS

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS			$T_{amb} = -40 \text{ TO } +85 \text{ }^{\circ}\text{C}$			UNIT
		$V_I$ (V)	OTHER	$V_{CC}$ (V)	MIN.	TYP. <sup>(1)</sup>	MAX.	
$V_{IH}$	HIGH-level input voltage			2.3 to 2.7	1.7	1.2	–	V
				2.7 to 3.6	2.0	1.5	–	V
$V_{IL}$	LOW-level input voltage			2.3 to 2.7	–	1.2	0.7	V
				2.7 to 3.6	–	1.5	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_{IH}$ or $V_{IL}$	$I_O = -100 \mu\text{A}$	2.3 to 3.6	$V_{CC} - 0.2$	$V_{CC}$	–	V
			$I_O = -6 \text{ mA}$	2.3	$V_{CC} - 0.3$	$V_{CC} - 0.08$	–	V
			$I_O = -12 \text{ mA}$	2.3	$V_{CC} - 0.6$	$V_{CC} - 0.26$	–	V
			$I_O = -12 \text{ mA}$	2.7	$V_{CC} - 0.5$	$V_{CC} - 0.14$	–	V
			$I_O = -12 \text{ mA}$	3.0	$V_{CC} - 0.6$	$V_{CC} - 0.09$	–	V
			$I_O = -24 \text{ mA}$	3.0	$V_{CC} - 1.0$	$V_{CC} - 0.28$	–	V
$V_{OL}$	LOW-level output voltage	$V_{IH}$ or $V_{IL}$	$I_O = 100 \mu\text{A}$	2.3 to 3.6	–	GND	0.20	V
			$I_O = 6 \text{ mA}$	2.3	–	0.07	0.40	V
			$I_O = 12 \text{ mA}$	2.3	–	0.15	0.70	V
			$I_O = 12 \text{ mA}$	2.7	–	0.14	0.40	V
			$I_O = 24 \text{ mA}$	3.0	–	0.27	0.55	V
$I_I$	input leakage current	$V_{CC}$ or GND		2.3 to 3.6	–	0.1	5	$\mu\text{A}$
$I_{OZ}$	3-state output OFF-state current	$V_{IH}$ or $V_{IL}$	$V_O = V_{CC}$ or GND	2.3 to 3.6	–	0.1	10	$\mu\text{A}$
$I_{CC}$	quiescent supply voltage	$V_{CC}$ or GND	$I_O = 0$	2.3 to 3.6	–	0.2	40	$\mu\text{A}$
$\Delta I_{CC}$	additional quiescent supply current given per data I/O pin with bus hold	$V_{CC} - 0.6$	$I_O = 0$	2.3 to 3.6	–	150	750	$\mu\text{A}$
$I_{BHL}$	bus hold LOW sustaining current	0.7 <sup>(2)</sup>		2.3 <sup>(2)</sup>	45	–		$\mu\text{A}$
		0.8 <sup>(2)</sup>		3.0 <sup>(2)</sup>	75	150		
$I_{BHH}$	bus hold HIGH sustaining current	1.7 <sup>(2)</sup>		2.3 <sup>(2)</sup>	–45			$\mu\text{A}$
		2.0 <sup>(2)</sup>		3.0 <sup>(2)</sup>	–75	–175		
$I_{BHLO}$	bus hold LOW overdrive current			3.6 <sup>(2)</sup>	500			$\mu\text{A}$
$I_{BHHO}$	bus hold LOW overdrive current			3.6 <sup>(2)</sup>	–500			$\mu\text{A}$

## Notes

1. All typical values are measured at  $T_{amb} = 25 \text{ }^{\circ}\text{C}$ .
2. Valid for data inputs of bus hold parts.

## 16-bit D-type registered transceiver; 3-state

## 74ALVCH16543

**AC CHARACTERISTICS FOR  $V_{CC} = 2.3$  TO  $2.7$  V**Ground = 0 V;  $t_r = t_f \leq 2.0$  ns;  $C_L = 30$  pF.

SYMBOL	PARAMETER	TEST CONDITIONS		$T_{amb} = -40$ TO $+85$ °C			UNIT
		WAVEFORMS	$V_{CC}$ (V)	MIN.	TYP. <sup>(1)</sup>	MAX.	
$t_{PHL}/t_{PLH}$	propagation delay $nA_n, nB_n$ to $nB_n, nA_n$	see Figs 6 and 10	2.3 to 2.7	1.0	3.4	5.1	ns
	propagation delay $n\overline{LE}_{AB}, n\overline{LE}_{BA}$ to $nB_n, nA_n$	see Figs 7 and 10	2.3 to 2.7	1.0	3.3	6.5	ns
$t_{PZH}/t_{PZL}$	3-state output enable time $n\overline{OE}_{BA}, n\overline{OE}_{AB}$ to $nA_n, nB_n$	see Figs 8 and 10	2.3 to 2.7	1.0	3.3	6.8	ns
$t_{PHZ}/t_{PLZ}$	3-state output disable time $n\overline{OE}_{BA}, n\overline{OE}_{AB}$ to $nA_n, nB_n$	see Figs 8 and 10	2.3 to 2.7	1.0	2.9	5.7	ns
$t_{PZH}/t_{PZL}$	3-state output enable time $n\overline{E}_{BA}, n\overline{E}_{AB}$ to $nA_n, nB_n$	see Figs 8 and 10	2.3 to 2.7	1.0	3.3	7.2	ns
$t_{PHZ}/t_{PLZ}$	3-state output disable time $n\overline{E}_{BA}, n\overline{E}_{AB}$ to $nA_n, nB_n$	see Figs 8 and 10	2.3 to 2.7	1.3	3.3	6.1	ns
$t_W$	$n\overline{LE}_{XX}$ pulse width LOW	see Figs 7 and 10	2.3 to 2.7	3.3	1.2	—	ns
$t_{su}$	set-up time $nA_n, nB_n$ to $n\overline{LE}_{XX}, n\overline{E}_{XX}$	see Figs 9 and 10	2.3 to 2.7	1.2	0.2	—	ns
$t_h$	hold time $nA_n, nB_n$ to $n\overline{LE}_{XX}, n\overline{E}_{XX}$	see Figs 9 and 10	2.3 to 2.7	1.2	0.2	—	ns

**Note**

1. All typical values are measured at  $T_{amb} = 25$  °C and  $V_{CC} = 2.5$  V.

## 16-bit D-type registered transceiver; 3-state

## 74ALVCH16543

**AC CHARACTERISTICS FOR  $V_{CC} = 2.7\text{ V}$  AND  $V_{CC} = 3.0\text{ V TO } 3.6\text{ V}$** Ground = 0 V;  $t_r = t_f \leq 2.5\text{ ns}$ ;  $C_L = 50\text{ pF}$ .

SYMBOL	PARAMETER	TEST CONDITIONS		$T_{amb} = -40\text{ TO } +85\text{ °C}$			UNIT
		WAVEFORMS	$V_{CC}\text{ (V)}$	MIN.	TYP. <sup>(1)</sup>	MAX.	
$t_{PHL}/t_{PLH}$	propagation delay $nA_n, nB_n$ to $nB_n, nA_n$	see Figs 6 and 10	2.7	–	2.9	4.8	ns
			3.0 to 3.6	1.0	3.8 <sup>(2)</sup>	4.3	ns
	propagation delay $n\overline{LE}_{AB}, n\overline{LE}_{BA}$ to $nB_n, nA_n$	see Figs 7 and 10	2.7	–	3.6	6.2	ns
			3.0 to 3.6	1.4	3.1 <sup>(2)</sup>	5.0	ns
$t_{PZH}/t_{PZL}$	3-state output enable time $n\overline{OE}_{BA}, n\overline{OE}_{AB}$ to $nA_n, nB_n$	see Figs 8 and 10	2.7	–	3.4	6.3	ns
			3.0 to 3.6	1.0	2.9 <sup>(2)</sup>	5.3	ns
$t_{PHZ}/t_{PLZ}$	3-state output disable time $n\overline{OE}_{BA}, n\overline{OE}_{AB}$ to $nA_n, nB_n$	see Figs 8 and 10	2.7	–	3.3	4.8	ns
			3.0 to 3.6	1.0	3.2 <sup>(2)</sup>	4.6	ns
$t_{PZH}/t_{PZL}$	3-state output enable time $nE_{BA}, nE_{AB}$ to $nA_n, nB_n$	see Figs 8 and 10	2.7	–	3.5	6.9	ns
			3.0 to 3.6	1.0	3.0 <sup>(2)</sup>	5.6	ns
$t_{PHZ}/t_{PLZ}$	3-state output disable time $n\overline{E}_{BA}, n\overline{E}_{AB}$ to $nA_n, nB_n$	see Figs 8 and 10	2.7	–	3.5	6.2	ns
			3.0 to 3.6	1.1	3.3 <sup>(2)</sup>	5.1	ns
$t_W$	$n\overline{LE}_{XX}$ pulse width LOW	see Figs 7 and 10	2.7	3.3	1.3	–	ns
			3.0 to 3.6	3.3	0.9 <sup>(2)</sup>	–	ns
$t_{su}$	set-up time $nA_n, nB_n$ to $n\overline{LE}_{XX}, n\overline{E}_{XX}$	see Figs 9 and 10	2.7	0.8	0.2	–	ns
			3.0 to 3.6	1.3	0.1 <sup>(2)</sup>	–	ns
$t_h$	hold time $nA_n, nB_n$ to $n\overline{LE}_{XX}, n\overline{E}_{XX}$	see Figs 9 and 10	2.7	0.4	0.1	–	ns
			3.0 to 3.6	0.7	0.2 <sup>(2)</sup>	–	ns

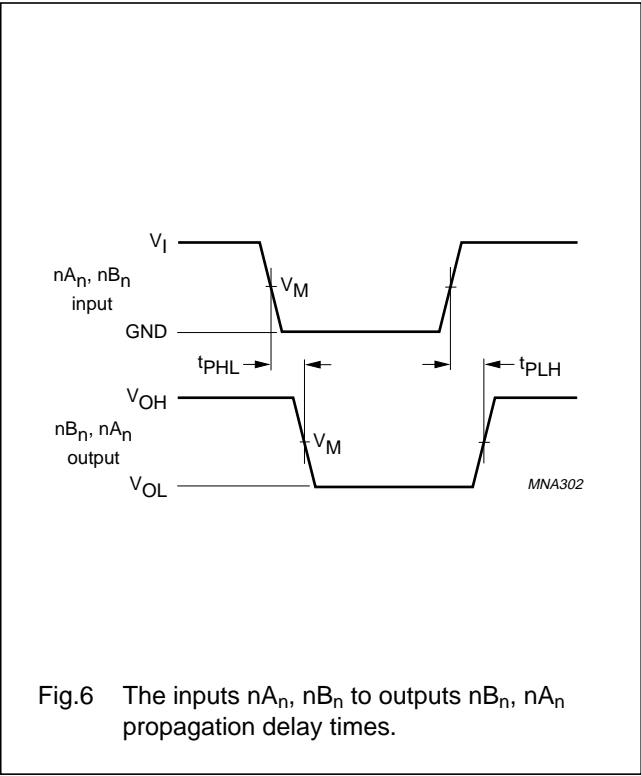
**Notes**

1. All typical values are measured at  $T_{amb} = 25\text{ °C}$ .
2. Typical values at  $V_{CC} = 3.0\text{ V}$ .

16-bit D-type registered transceiver; 3-state

74ALVCH16543

AC WAVEFORMS

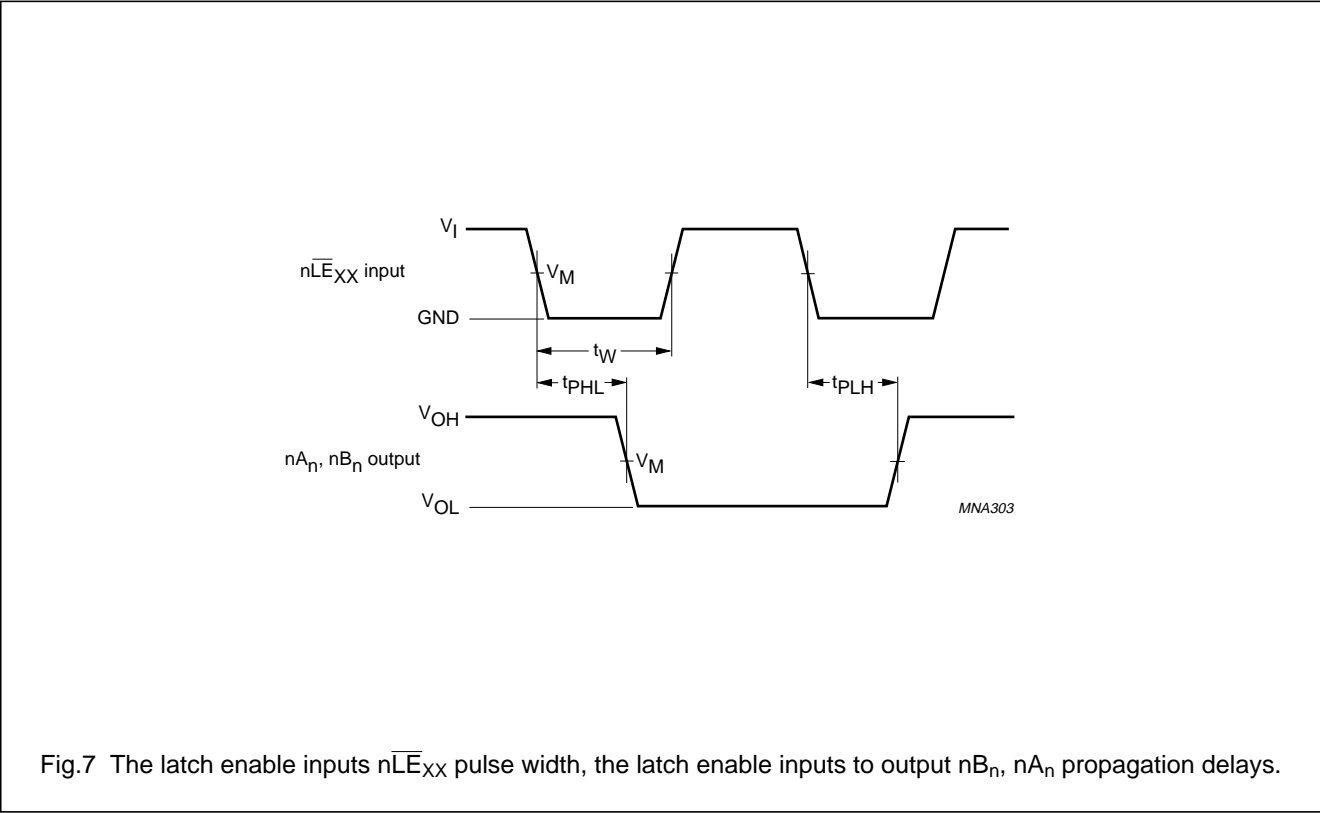


Notes:  $V_{CC} = 2.3$  to  $2.7$  V

- $V_M = 0.5V_{CC}$ ;
- $V_X = V_{OL} + 150$  mV;
- $V_Y = V_{OH} - 150$  mV;
- $V_I = V_{CC}$ ;
- $V_{OL}$  and  $V_{OH}$  are typical output voltage drop that occur with the output load.

Notes:  $V_{CC} = 3.0$  to  $3.6$  V and  $V_{CC} = 2.7$  V

- $V_M = 1.5$  V;
- $V_X = V_{OL} + 300$  mV;
- $V_Y = V_{OH} - 300$  mV;
- $V_I = 2.7$  V;
- $V_{OL}$  and  $V_{OH}$  are typical output voltage drop that occur with the output load.



16-bit D-type registered transceiver; 3-state

74ALVCH16543

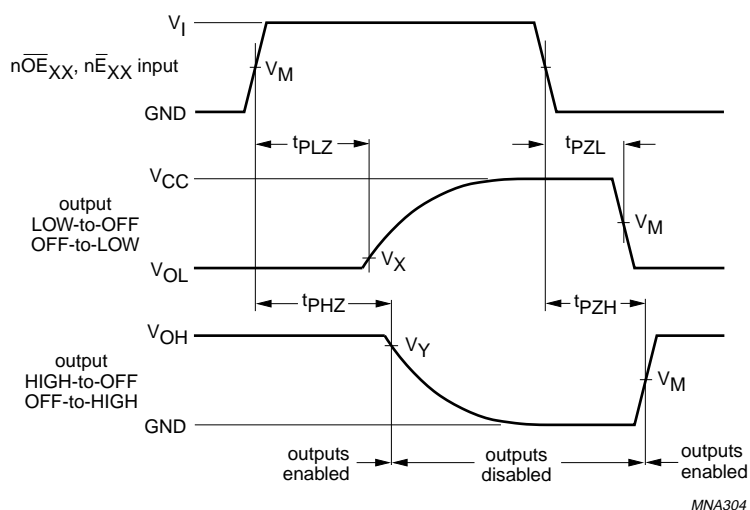


Fig.8 The 3-state enable and disable times.

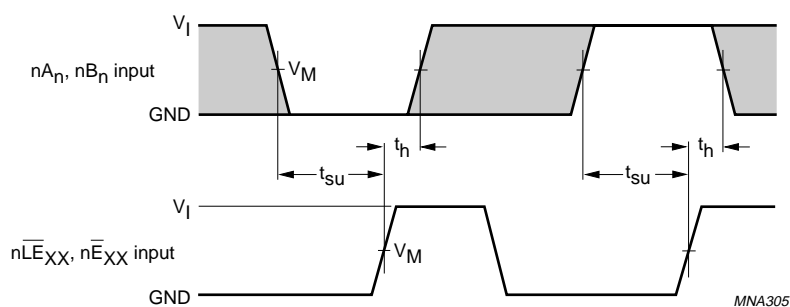
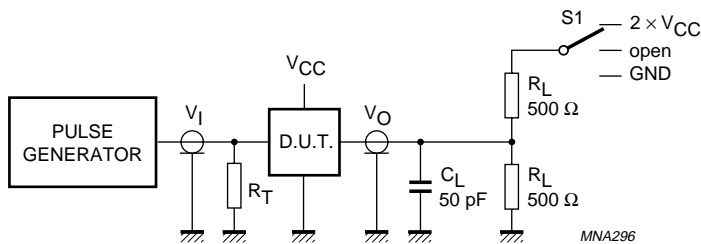


Fig.9 The data set-up and hold times for the  $nA_n$ ,  $nB_n$  input to the  $n\overline{LE}_{XX}$  input.

16-bit D-type registered transceiver; 3-state

74ALVCH16543



TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	open
t <sub>PLZ</sub> /t <sub>PZL</sub>	2 × V <sub>CC</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

V <sub>CC</sub>	V <sub>I</sub>
<2.7 V	V <sub>CC</sub>
2.7 to 3.6 V	2.7 V

Definitions for test circuit.  
C<sub>L</sub> = load capacitance including jig and probe capacitance (See Chapter “AC characteristics”)  
R<sub>L</sub> = load resistance.  
R<sub>T</sub> = termination resistance should be equal to the output impedance Z<sub>o</sub> of the pulse generator.

Fig.10 Test circuitry for switching times.

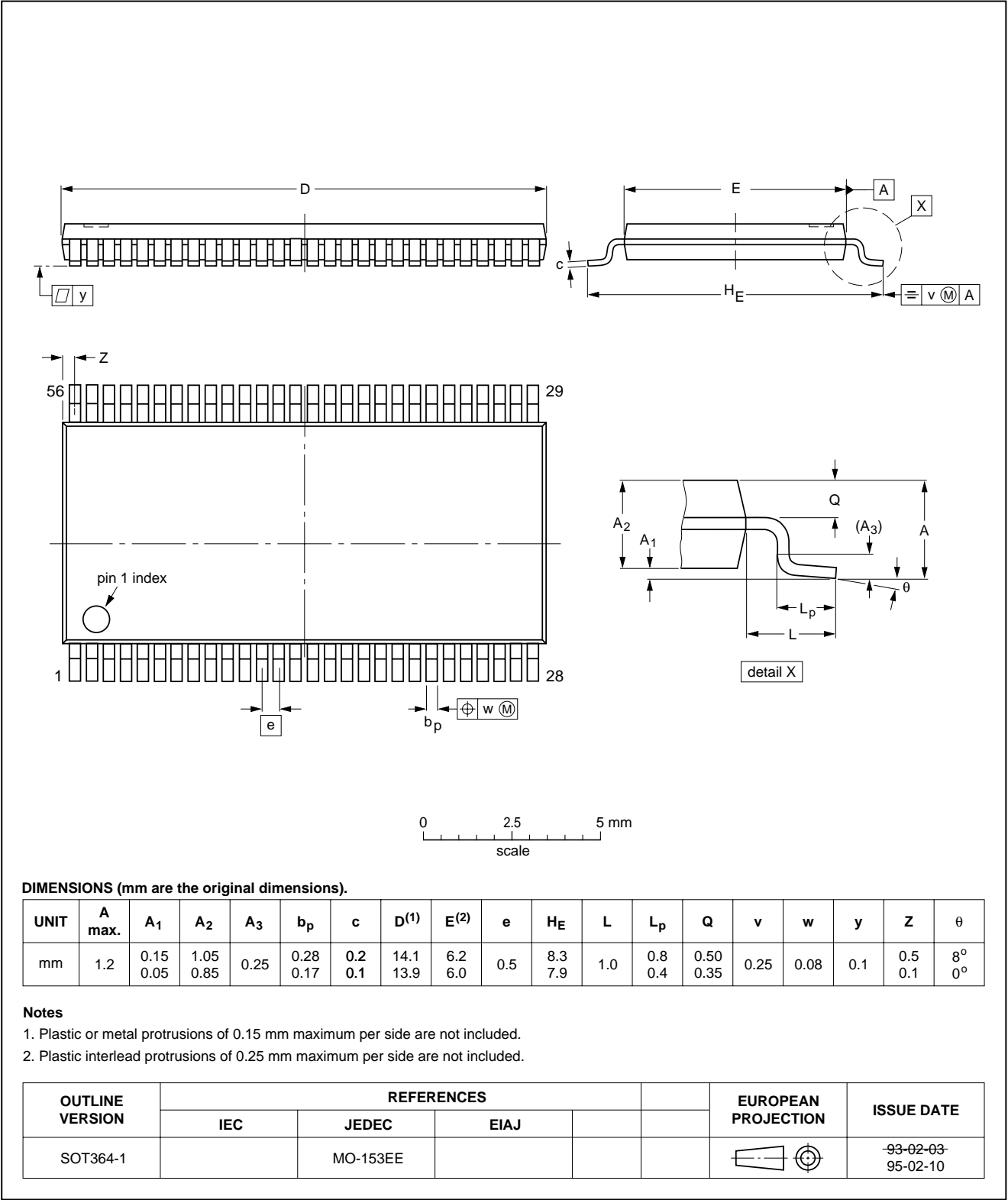
16-bit D-type registered transceiver; 3-state

74ALVCH16543

PACKAGE OUTLINE

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1



## 16-bit D-type registered transceiver; 3-state

## 74ALVCH16543

**SOLDERING****Introduction to soldering surface mount packages**

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

**Reflow soldering**

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

**Wave soldering**

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

**Manual soldering**

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.



## 16-bit D-type registered transceiver; 3-state

74ALVCH16543

## Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW <sup>(1)</sup>
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable <sup>(2)</sup>	suitable
PLCC <sup>(3)</sup> , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended <sup>(3)(4)</sup>	suitable
SSOP, TSSOP, VSO	not recommended <sup>(5)</sup>	suitable

## Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

## DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
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