DATA SHEET

74ALVCH16832

7-bit to 28-bit address register/driver with 3-state outputs

Product data

2001 Dec 14

File under Integrated Circuits — ICL03

Philips Semiconductors

PHILIPS

7-bit to 28-bit address register/driver with 3-state outputs 74ALVCH16832

FEATURES

- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA
- Bus hold on data inputs eliminates the need for external pullup/pulldown resistors

DESCRIPTION

This 7 channel 1-bit to 4-bit address register/driver is designed for 2.3 V to 3.6 V V_{CC} operation. This device is ideal for use in applications in which a single address bus is driving four separate memory locations. The 74ALVCH16832 can be used as a buffer or a register, depending on the logic level of the select (SEL) input.

When $\overline{SEL}$ is a logic high, the device is in the buffer mode. The outputs follow the inputs and are controlled by the two output-enable ($\overline{OE}$) inputs. Each $\overline{OE}$ controls two groups of seven outputs.

When $\overline{SEL}$ is a logic low, the device is in the register mode. The register is an edge-triggered D-type flip-flop. On the positive transition of the clock ($\overline{CLK}$) input, data at the A inputs is stored in the internal registers. $\overline{OE}$ operates the same as in the buffer mode.

When $\overline{OE}$ is a logic low, the outputs are in a normal logic state, (high or low logic level). When $\overline{OE}$ is a logic high, the outputs are in the high-impedance state.

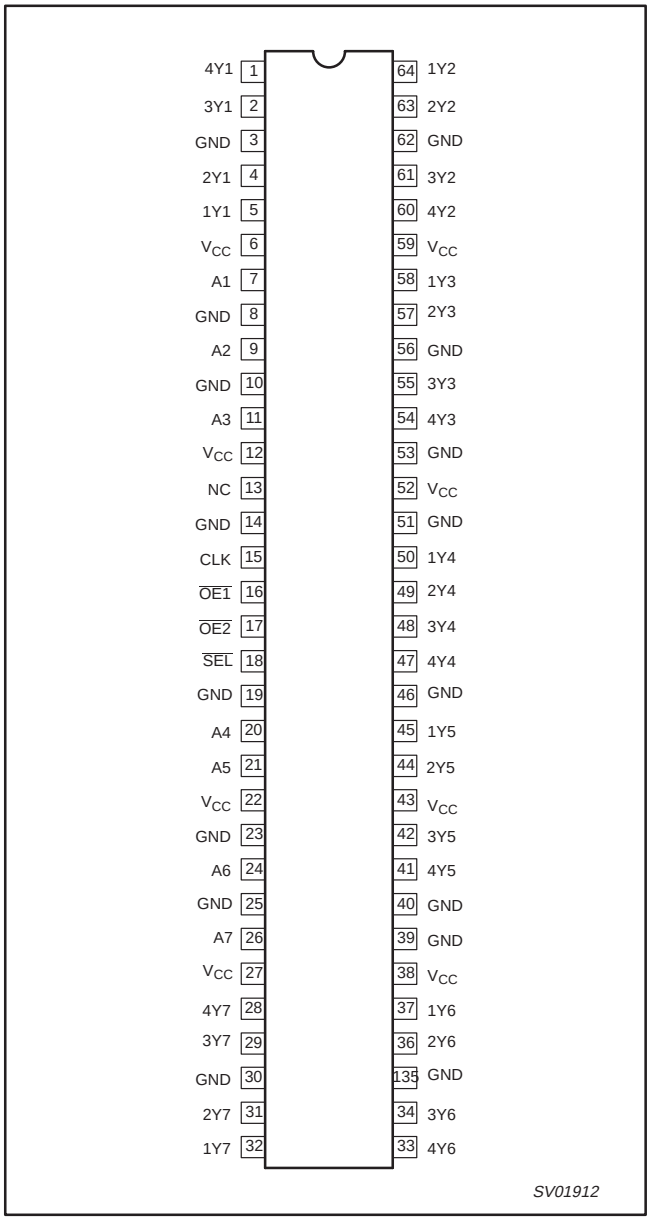
Neither $\overline{SEL}$ of $\overline{OE}$ affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active buss-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The 74ALVCH16832 is characterized for operation from –40 to +85° C.

PIN CONFIGURATION



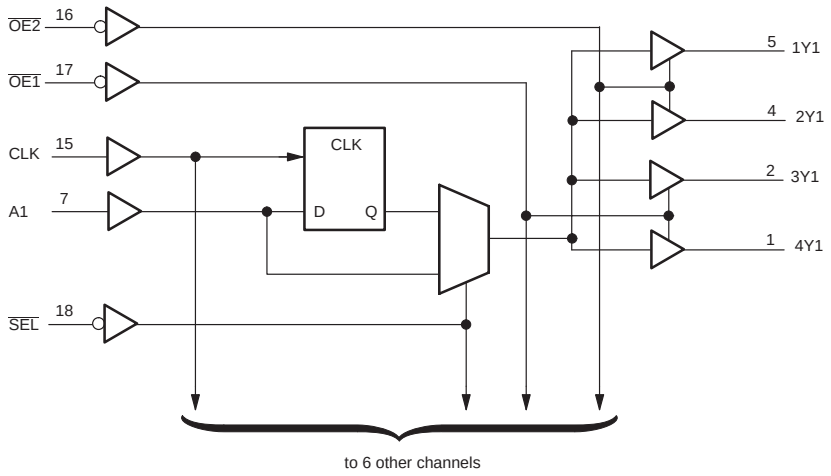
PIN DESCRIPTION

PIN(S)	SYMBOL	FUNCTION
1, 2, 4, 5, 28. 29, 31, 32, 33, 34, 36, 37, 41, 42, 44, 45, 47, 48, 49, 50, 54, 55, 57, 58, 60, 61, 63, 64	1Yn, 2Yn, 3Yn, 4Yn	Outputs
3, 8, 10, 14, 19, 23, 25, 30, 35, 39, 40, 46, 51, 53, 56, 62	GND	Ground
6, 12, 22, 27, 38, 43, 52, 59	V_{CC}	Supply voltage
7, 9, 11, 20, 21, 24, 26	An	Inputs
16, 17	$\overline{OE1}$, $\overline{OE2}$	Output enable
15	CLK	Clock
$\overline{18}$	$\overline{SEL}$	Select

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
64-pin Plastic TSSOP	–40 to +85 °C	74ALVCH16832DGG	SOT646-1

LOGIC DIAGRAM (POSITIVE LOGIC)



FUNCTION TABLE

Inputs				Output
$\overline{OE}$	$\overline{SEL}$	$\overline{CLK}$	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H

ABSOLUTE MAXIMUM RATINGS

Over recommended operating free-air temperature range (unless otherwise noted).[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	Supply voltage range		–0.5 to +4.6	V
V_I	Input voltage range	See Note 2	–0.5 to +4.6	V
V_O	Output voltage range	See Notes 2 and 3	–0.5 to V_{CC} +0.5	V
I_{IK}	Input clamp current	$V_I < 0$	–50	mA
I_{OK}	Output clamp current	$V_O < 0$	–50	mA
I_O	Continuous output current		±50	mA
I_{CC}, I_{GND}	Continuous current through each V_{CC} or GND		±100	mA
Θ_{JA}	Package thermal impedance	See Note 4	106	°C/W
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:

1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under ”recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
3. This value is limited to 4.6 V maximum.
4. The package thermal impedance is calculated in accordance with JESD 51.

RECOMMENDED OPERATING CONDITIONS

All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	—	V
		V_{CC} = 2.7 V to 3.6 V	2	—	
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V	—	$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V	—	0.7	
		V_{CC} = 2.7 V to 3.6 V	—	0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V	—	–12	mA
		V_{CC} = 2.7 V	—	–12	
		V_{CC} = 3 V	—	–24	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		12	mA
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_{amb}	Operating free-air temperature		–40	+85	°C

ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range (unless otherwise noted).

SYMBOL	PARAMETER	TEST CONDITIONS	V_{CC}	LIMITS			UNIT
				MIN	TYP[1]	MAX	
V_{OH}		I_{OH} = –100 μA	2.3 V to 3.6 V	V_{CC}–0.2	—	—	V
		I_{OH} = –4 mA	2.3 V	1.2	—	—	
		I_{OH} = –6 mA	2.3 V	2.0	—	—	
		I_{OH} = –12 mA	2.3 V	1.7	—	—	
			2.7 V	2.2	—	—	
			3 V	2.4	—	—	
		I_{OH} = –24 mA	3 V	2	—	—	
V_{OL}		I_{OL} = 100 μA	2.3 V to 3.6 V	—	—	0.2	V
		I_{OL} = 4 mA	2.3 V	—	—	0.45	
		I_{OL} = 6 mA	2.3 V	—	—	0.4	
		I_{OL} = 12 mA	2.3 V	—	—	0.7	
			2.7 V	—	—	0.4	
		I_{OL} = 24 mA	3 V	—	—	0.55	
I_I		$V_I = V_{CC}$ or GND	3.6 V	—	—	±5	μA
$I_{I(hold)}$		V_I = 0.7 V	2.3 V	45	—	—	μA
		V_I = 1.7 V	2.3 V	–45	—	—	
		V_I = 0.8 V	3 V	75	—	—	
		V_I = 2 V	3 V	–75	—	—	
		V_I = 0 to 3.6 V[2]	3.6 V	—	—	±500	
I_{OZ}		$V_O = V_{CC}$ or GND	3.6 V	—	—	±10	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	3.6 V	—	—	40	μA
ΔI_{CC}		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V	—	—	750	μA
C_i	Control inputs	$V_I = V_{CC}$ or GND	3.3 V	—	4.5	—	pF
	Data inputs			—	5	—	
C_o	Outputs	$V_O = V_{CC}$ or GND	3.3 V	—	7.5	—	pF

NOTES:

1. All typical values are at V_{CC} = 3.3 V, T_{amb} = 25°C.
2. This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

TIMING REQUIREMENTS

Over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3).

		V_{CC} = 1.8 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{CLK}	Clock frequency	—	—	—	150	—	150	—	150	MHz
t_W	Pulse duration, CLK high or low	—	—	3.3	—	3.3	—	3.3	—	ns
t_{SU}	Setup time, A data before CLK ↑	—	—	2	—	2	—	1.6	—	ns
t_h	Hold time, A data after CLK ↑	—	—	0.7	—	0.5	—	1.1	—	ns

SWITCHING CHARACTERISTICS

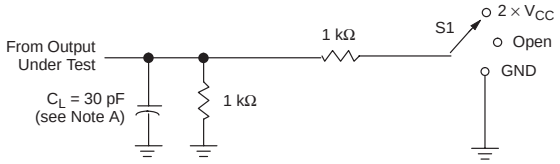
Over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3).

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{MAX}			—	—	150	—	150	—	150	—	MHz
t_{pd}	A	Y	—	—	1.2	4	—	4.1	1.6	3.6	ns
	CLK		—	—	1.1	4.5	—	4.4	1.5	3.9	
	$\overline{SEL}$		—	—	1.3	5.2	—	5.2	1.7	4.4	
t_{en}	$\overline{OE}$	Y	—	—	1.1	5.1	—	5	1.2	4.3	ns
t_{dis}	$\overline{OE}$	Y	—	—	1.4	5.5	—	4.7	1.6	4.5	ns

OPERATING CHARACTERISTICS, T_{amb} = 25 °C

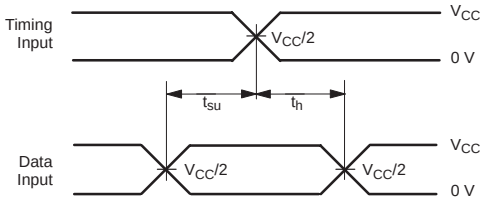
SYMBOL	PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per driver	All outputs enabled	C_L = 0, f = 10 MHz	—	119	132	pF
		All outputs disabled		—	22	25	

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 1.8 V

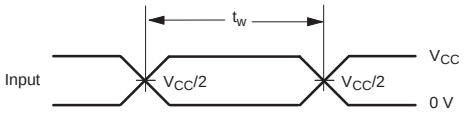


Load Circuit

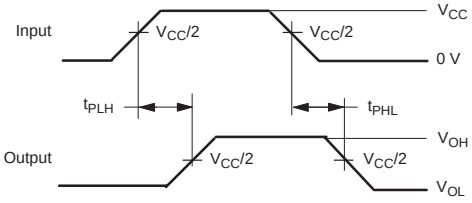
TEST	S_1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



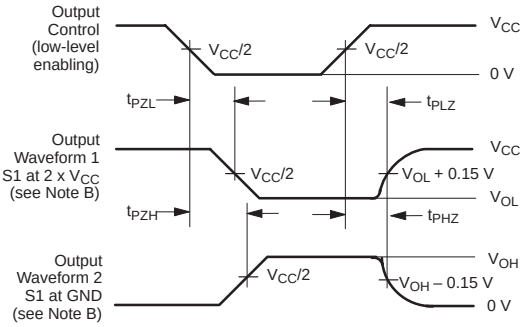
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



Voltage Waveforms
Enable and Disable Times

SV01911

NOTES:

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.

D. The outputs are measured one at a time with one transition per measurement.

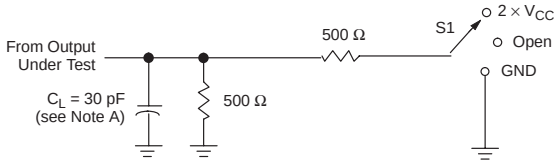
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}.

G. t_{PLH} and t_{PHL} are the same as t_{pd}.

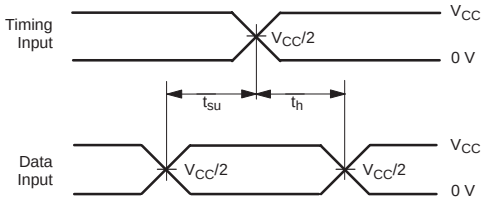
Figure 1. Load circuit and voltage waveforms

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

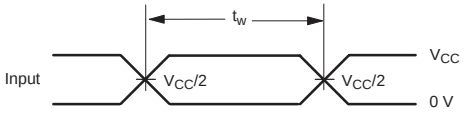


Load Circuit

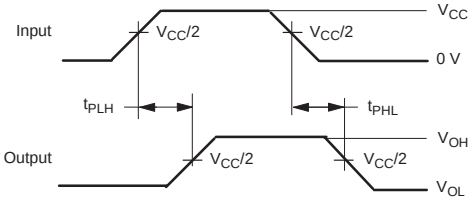
TEST	S_1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



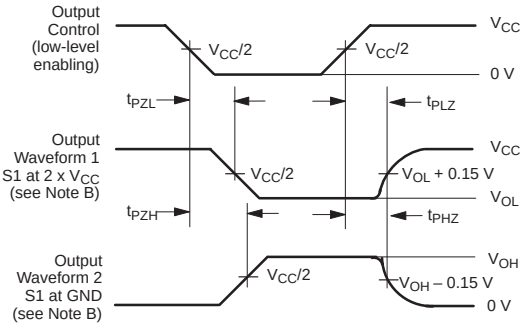
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



Voltage Waveforms
Enable and Disable Times

SV01849

Figure 2. Load circuit and voltage waveforms

NOTES:

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.

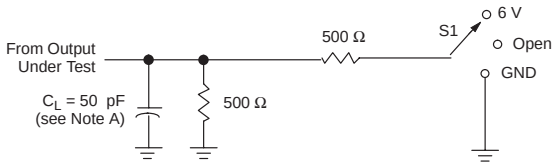
D. The outputs are measured one at a time with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}.

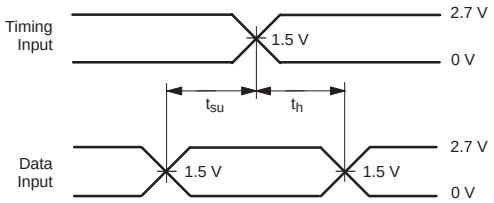
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V and 3.3 V ± 0.3 V

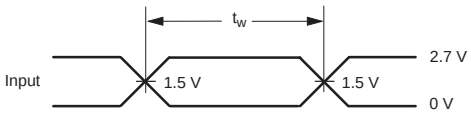


Load Circuit

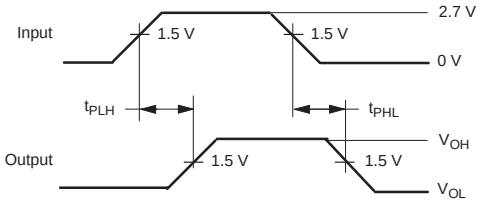
TEST	S_1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



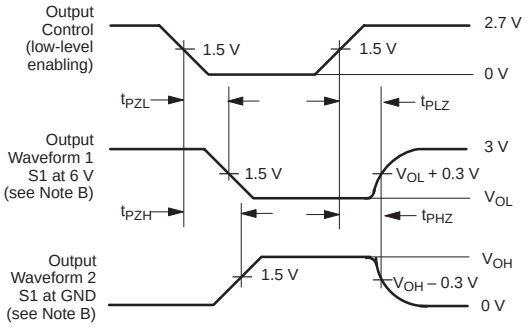
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



Voltage Waveforms
Enable and Disable Times

SV01850

NOTES:

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

D. The outputs are measured one at a time with one transition per measurement.

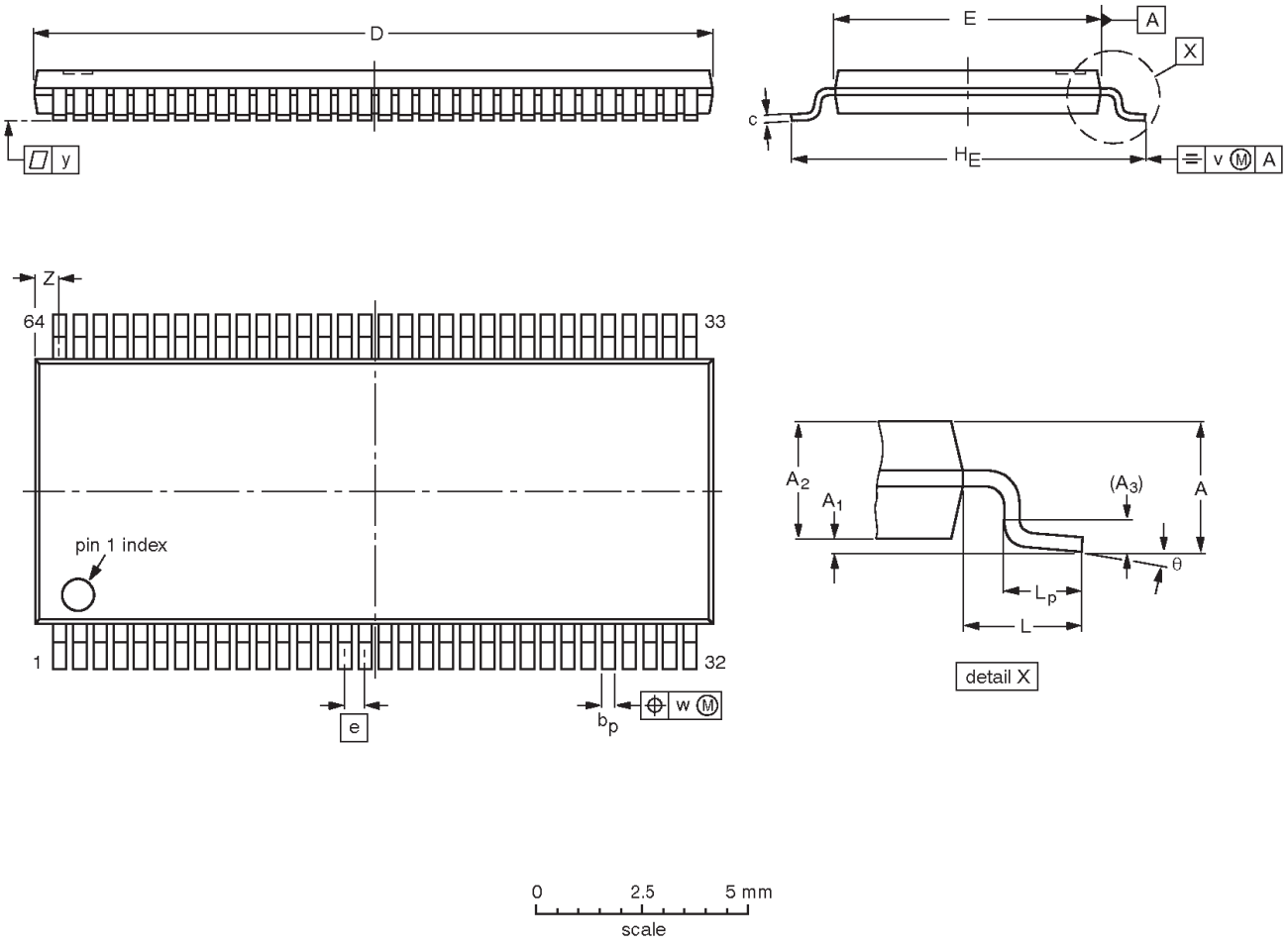
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}.

G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 3. Load circuit and voltage waveforms

TSSOP64: plastic thin shrink small outline package; 64 leads; body width 6.1 mm SOT646-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.27 0.17	0.2 0.1	17.1 16.9	6.2 6.0	0.5	8.3 7.9	1.0	0.75 0.45	0.2	0.08	0.1	0.89 0.61	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT646-1		MO-153					00-08-21

NOTES

Data sheet status

Data sheet status [1]	Product status [2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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