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Kind regards,

Team Nexperia

# DATA SHEET

**74ALVCH16843**

**18-bit bus-interface D-type latch (3-State)**

Product specification

1998 Aug 04

IC24 Data Handbook

## 18-bit bus interface D-type latch (3-State)

## 74ALVCH16843

## FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive  $\pm 24$  mA at 3.0 V
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple  $V_{CC}$  and GND pins for minimum noise and ground bounce
- All data inputs have bus hold
- Output drive capability 50 $\Omega$  transmission lines @ 85°C

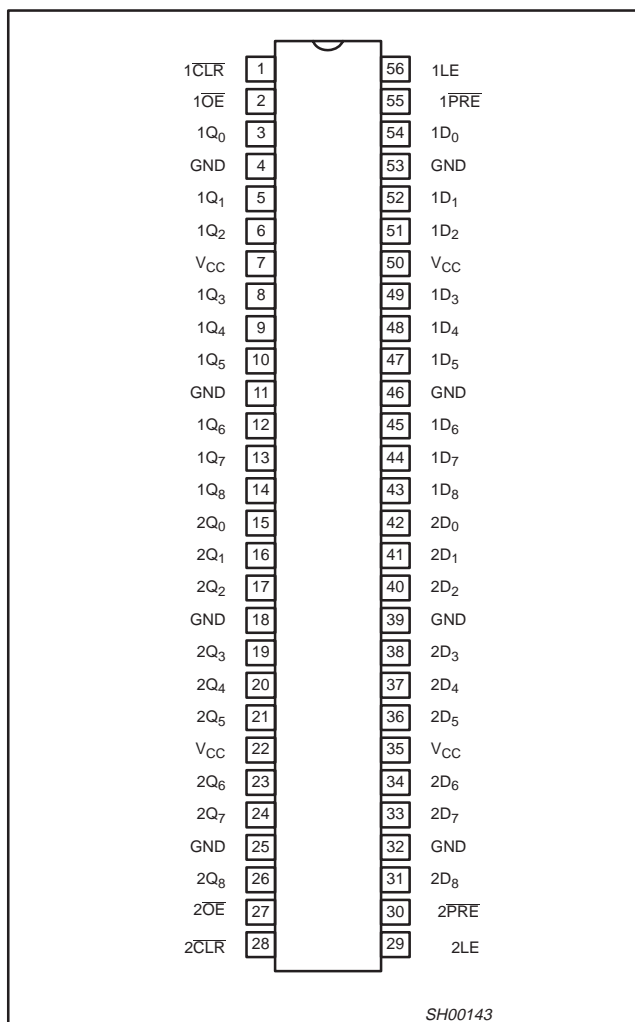
## DESCRIPTION

The 74ALVCH16843 has two 9-bit D-type latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. The two sections of each register are controlled independently by the latch enable ( $\overline{nLE}$ ), clear ( $\overline{nCLR}$ ), preset ( $\overline{nPRE}$ ) and output enable ( $\overline{nOE}$ ) control gates.

When  $\overline{nOE}$  is LOW, the data in the registers appear at the outputs. When  $\overline{nOE}$  is HIGH, the outputs are in the high impedance OFF state. Operation of the  $\overline{nOE}$  input does not affect the state of the flip-flops.

The 74ALVCH16843 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

## PIN CONFIGURATION



SH00143

## QUICK REFERENCE DATA

GND = 0V;  $T_{amb} = 25^{\circ}\text{C}$ ;  $t_r = t_f \leq 2.5\text{ns}$

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	Propagation delay nDn to nQn	$V_{CC} = 2.5\text{V}$ , $C_L = 30\text{pF}$ $V_{CC} = 3.3\text{V}$ , $C_L = 50\text{pF}$		2.2 2.1	ns
	Propagation delay nLE to nQn	$V_{CC} = 2.5\text{V}$ , $C_L = 30\text{pF}$ $V_{CC} = 3.3\text{V}$ , $C_L = 50\text{pF}$		2.3 2.0	ns
$C_I$	Input capacitance			5.0	pF
$C_{PD}$	Power dissipation capacitance per buffer	$V_I = \text{GND to } V_{CC}^1$	transparent mode Output enabled Output disabled	17 3	pF
			Clocked mode Output enabled Output disabled	19 9	

## NOTES:

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  $f_i$  = input frequency in MHz;  $C_L$  = output load capacitance in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DRAWING NUMBER
56-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	74ALVCH16843 DGG	ACH16843 DGG	SOT364-1

18-bit bus interface D-type latch (3-State)

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PIN DESCRIPTION

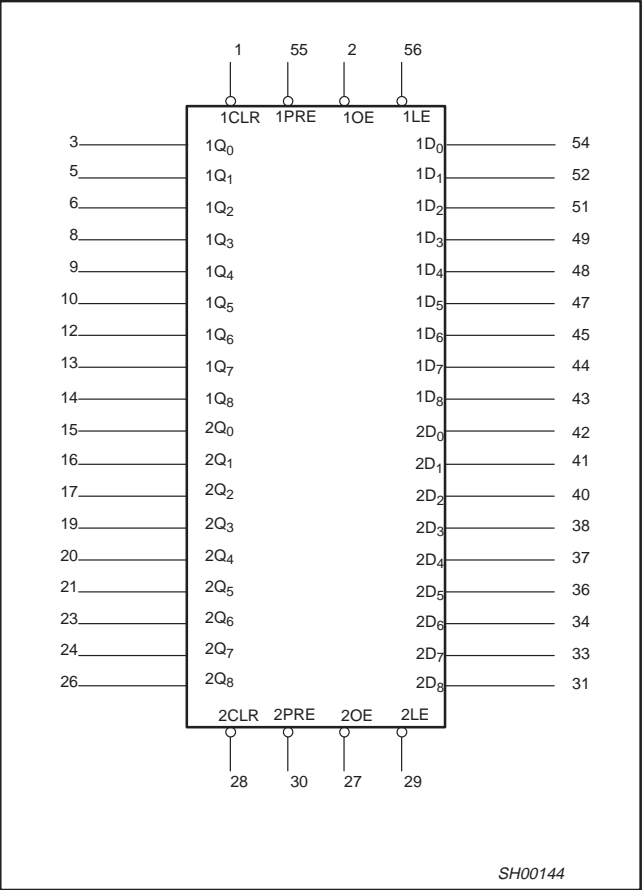
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	1 $\overline{\text{CLR}}$	Clear input (active LOW)
2	1 $\overline{\text{OE}}$	Output enable input (active LOW)
55	1 $\overline{\text{PRE}}$	Preset input (active LOW)
56	1LE	Latch enable input (active HIGH)
54, 52, 51, 49, 48, 47, 45, 44, 43	1D0 to 1D8	Data inputs
3, 5, 6, 8, 9, 10, 12, 13, 14	1Q0 to 1Q8	Data outputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V <sub>CC</sub>	Positive supply voltage
27	2 $\overline{\text{OE}}$	Output enable input (active LOW)
28	2 $\overline{\text{CLR}}$	Clear input (active LOW)
29	2LE	Latch enable input (active HIGH)
30	2 $\overline{\text{PRE}}$	Preset input (active LOW)
42, 41, 40, 38, 37, 36, 34, 33, 31	2D0 to 2D8	Data inputs
15, 16, 17, 19, 20, 21, 23, 24, 26	2Q0 to 2Q8	Data outputs

FUNCTION TABLE

INPUTS					OUTPUT
nPRE	nCLR	nOE	LE	D <sub>x</sub>	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	H	X	Q <sub>0</sub>
X	X	H	H	X	Z

H = HIGH voltage level  
L = LOW voltage level  
X = Don't care  
Z = High impedance "off" state

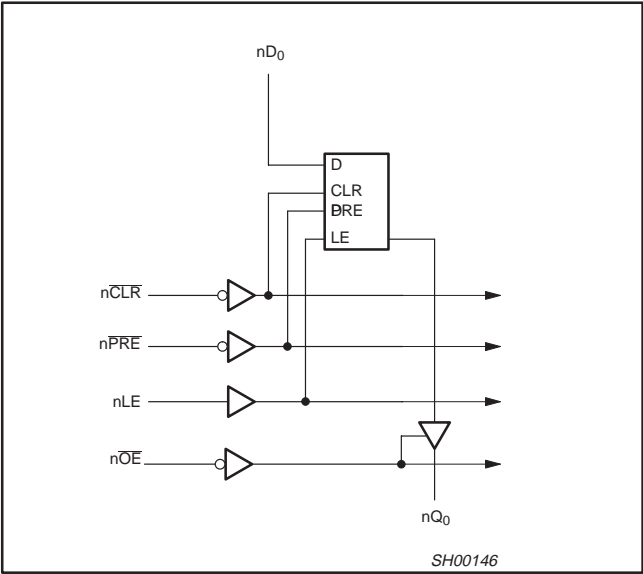
LOGIC SYMBOL



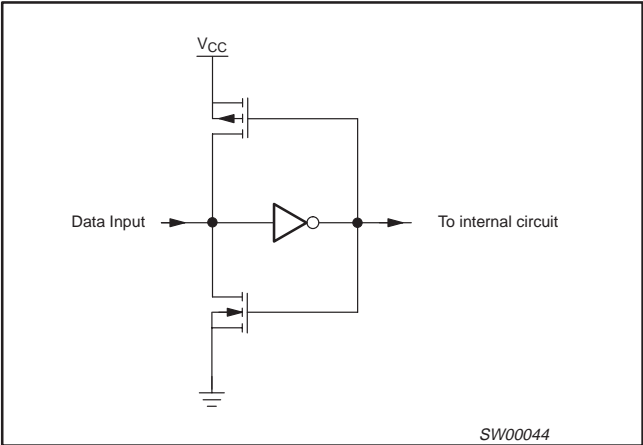
18-bit bus interface D-type latch (3-State)

74ALVCH16843

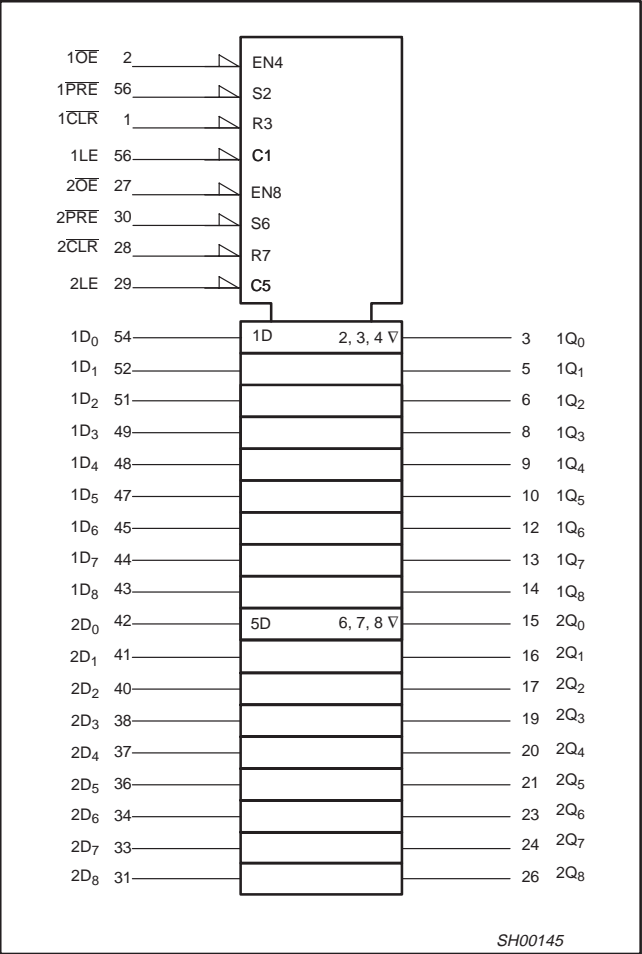
LOGIC DIAGRAM



BUS HOLD CIRCUIT



LOGIC SYMBOL (IEEE/IEC)



## 18-bit bus interface D-type latch (3-State)

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
$V_{CC}$	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
$V_I$	DC Input voltage range		0	$V_{CC}$	V
$V_O$	DC output voltage range		0	$V_{CC}$	V
$T_{amb}$	Operating free-air temperature range		-40	+85	°C
$t_r, t_f$	Input rise and fall times	$V_{CC} = 2.3$ to $3.0$ V $V_{CC} = 3.0$ to $3.6$ V	0 0	20 10	ns/V

## ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +4.6	V
$I_{IK}$	DC input diode current	$V_I < 0$	-50	mA
$V_I$	DC input voltage	For control pins <sup>2</sup>	-0.5 to +4.6	V
		For data inputs <sup>2</sup>	-0.5 to $V_{CC} + 0.5$	
$I_{OK}$	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
$V_O$	DC output voltage	Note 2	-0.5 to $V_{CC} + 0.5$	V
$I_O$	DC output source or sink current	$V_O = 0$ to $V_{CC}$	±50	mA
$I_{GND}, I_{CC}$	DC $V_{CC}$ or GND current		±100	mA
$T_{stg}$	Storage temperature range		-65 to +150	°C
$P_{TOT}$	Power dissipation per package	For temperature range: -40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	850 600	mW
	-plastic medium-shrink (SSOP)			
	-plastic thin-medium-shrink (TSSOP)			

## NOTE:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 18-bit bus interface D-type latch (3-State)

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## DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
V <sub>IH</sub>	HIGH level Input voltage	V <sub>CC</sub> = 2.3 to 2.7V	1.7	1.2		V
		V <sub>CC</sub> = 2.7 to 3.6V	2.0	1.5		
V <sub>IL</sub>	LOW level Input voltage	V <sub>CC</sub> = 2.3 to 2.7V		1.2	0.7	V
		V <sub>CC</sub> = 2.7 to 3.6V		1.5	0.8	
V <sub>OH</sub>	HIGH level output voltage	V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -100μA	V <sub>CC</sub> - 0.2	V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -6mA	V <sub>CC</sub> - 0.3	V <sub>CC</sub> - 0.08		
		V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.26		
		V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA	V <sub>CC</sub> - 0.5	V <sub>CC</sub> - 0.14		
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.09		
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -24mA	V <sub>CC</sub> - 1.0	V <sub>CC</sub> - 0.28		
V <sub>OL</sub>	LOW level output voltage	V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100μA		GND	0.20	V
		V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 6mA		0.07	0.40	V
		V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA		0.15	0.70	V
		V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA		0.14	0.40	
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 24mA		0.27	0.55	
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND		0.1	5	μA
I <sub>OZ</sub>	3-State output OFF-state current	V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND		0.1	10	μA
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0		0.2	40	μA
ΔI <sub>CC</sub>	Additional quiescent supply current	V <sub>CC</sub> = 2.3V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V; I <sub>O</sub> = 0		150	750	μA
I <sub>BHL</sub> <sup>2</sup>	Bus hold LOW sustaining current	V <sub>CC</sub> = 2.3V; V <sub>I</sub> = 0.7V	45	—		μA
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 0.8V	75	150		
I <sub>BHH</sub> <sup>2</sup>	Bus hold HIGH sustaining current	V <sub>CC</sub> = 2.3V; V <sub>I</sub> = 1.7V	-45			μA
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 2.0V	-75	-175		
I <sub>BHLO</sub> <sup>2</sup>	Bus hold LOW overdrive current	V <sub>CC</sub> = 3.6V	500			μA
I <sub>BHHO</sub> <sup>2</sup>	Bus hold HIGH overdrive current	V <sub>CC</sub> = 3.6V	-500			μA

## NOTES:

1. All typical values are at T<sub>amb</sub> = 25°C.
2. Valid for data inputs of bus hold parts.

## 18-bit bus interface D-type latch (3-State)

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**AC CHARACTERISTICS FOR  $V_{CC} = 2.3V$  TO  $2.7V$  RANGE**GND = 0V;  $t_r = t_f \leq 2.0ns$ ;  $C_L = 30pF$ 

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V <sub>CC</sub> = 2.3 to 2.7V			
			MIN	TYP <sup>1</sup>	MAX	
t <sub>PHL</sub> /t <sub>PLH</sub>	Propagation delay nDn to nQn	1, 6	1.0	2.2	4.3	ns
	Propagation delay nLE to nQn	2, 6	1.0	2.3	4.6	
	Propagation delay nPRE to nQn	1, 6	1.0	2.5	4.8	
	Propagation delay nCLR to nQn	1, 6	1.0	2.5	4.8	
t <sub>PZH</sub> /t <sub>PZL</sub>	3-State output enable time nOE to nQn	5, 6	1.0	2.8	5.8	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-State output disable time nOE to nQn	5, 6	1.1	2.2	4.3	ns
t <sub>SU</sub>	Set-up time nDn to nLE	3, 6	0.5	−0.1	−	ns
t <sub>H</sub>	Hold time nDn to nLE	3, 6	0.9	0.5	−	ns
t <sub>W</sub>	nLE pulse width HIGH	2, 6	1.5	0.5	−	ns
	nPRE pulse width LOW	4, 6	1.5	0.5	−	
	nCLR pulse width LOW	4, 6	1.5	0.5	−	
t <sub>REM</sub>	Recovery time nPRE to nLE	4, 6	0.5	1.1	−	ns
	Recovery time nCLR to nLE	4, 6	0.5	1.0	−	

**NOTE:**1. All typical values are at  $V_{CC} = 3.3V$  and  $T_{amb} = 25^\circ C$ .**AC CHARACTERISTICS FOR  $V_{CC} = 3.0V$  TO  $3.6V$  RANGE AND  $V_{CC} = 2.7V$** GND = 0V;  $t_r = t_f \leq 2.5ns$ ;  $C_L = 50pF$ 

SYMBOL	PARAMETER	WAVEFORM	LIMITS			LIMITS			UNIT
			V <sub>CC</sub> = 3.3 ± 0.3V			V <sub>CC</sub> = 2.7V			
			MIN	TYP <sup>1, 2</sup>	MAX	MIN	TYP <sup>1</sup>	MAX	
t <sub>PHL</sub> /t <sub>PLH</sub>	Propagation delay nDn to nQn	1, 6	1.0	2.1	3.5	1.0	2.3	4.0	ns
	Propagation delay nLE to nQn	2, 6	1.0	2.0	3.5	1.0	2.1	3.9	
	Propagation delay nPRE to nQn	1, 6	1.0	2.2	3.8	1.0	2.6	4.5	
	Propagation delay nCLR to nQn	1, 6	1.0	2.3	3.9	1.0	2.5	4.3	
t <sub>PZH</sub> /t <sub>PZL</sub>	3-State output enable time nOE to nQn	5, 6	1.0	2.5	4.4	1.0	3.0	5.3	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-State output disable time nOE to nQn	5, 6	1.3	2.6	4.0	1.3	2.8	4.4	ns
t <sub>SU</sub>	Set-up time nDn to nLE	3, 6	0.5	0.0	—	0.5	−0.3	—	ns
t <sub>h</sub>	Hold time nDn to nLE	3, 6	0.9	0.5	—	0.9	0.5	—	ns
t <sub>W</sub>	nLE pulse width HIGH	2, 6	1.5	0.5	—	1.5	0.5	—	ns
	nPRE pulse width LOW	4, 6	1.5	0.5	—	1.5	0.6	—	
	nCLR pulse width LOW	4, 6	1.5	0.5	—	1.5	0.5	—	
t <sub>REM</sub>	Recovery time nPRE to nLE	4, 6	1.0	0.4	—	0.8	−0.2	—	ns
	Recovery time nCLR to nLE	4, 6	0.8	0.2	—	0.6	−0.4	—	

**NOTES:**

1. All typical values are measured  $T_{amb} = 25^\circ C$ .
2. Typical value is measured at  $V_{CC} = 3.3V$



## 18-bit bus interface D-type latch (3-State)

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**AC WAVEFORMS FOR  $V_{CC} = 2.3V$  TO  $2.7V$  AND  $V_{CC} < 2.3V$  RANGE**

$$V_M = 0.5 V$$

$$V_X = V_{OL} + 0.15V$$

$$V_Y = V_{OH} - 0.15V$$

$V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.

$$V_I = V_{CC}$$

**AC WAVEFORMS FOR  $V_{CC} = 3.0V$  TO  $3.6V$  AND  $V_{CC} = 2.7V$  RANGE**

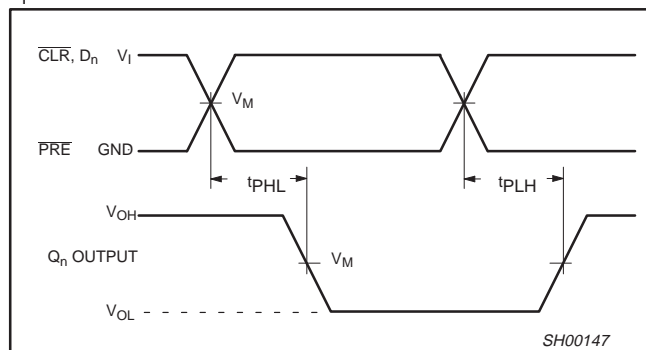
$$V_M = 1.5 V$$

$$V_X = V_{OL} + 0.3V$$

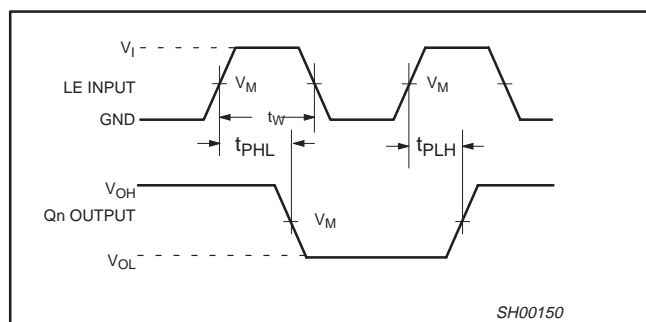
$$V_Y = V_{OH} - 0.3V$$

$V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.

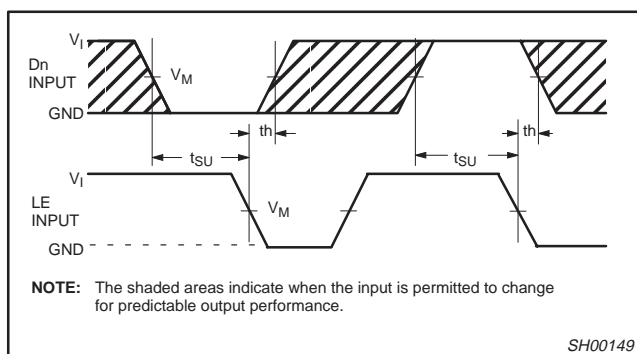
$$V_I = 2.7V$$



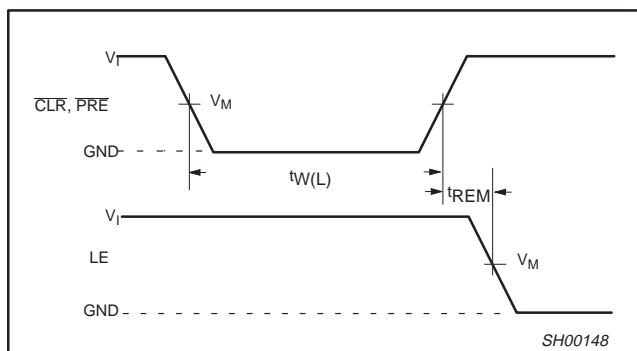
**Waveform 1.** Data input (Dn) to output (Qn), clear input (CLR) to output (Qn) and preset input (PRE) to output (Qn) propagation delay



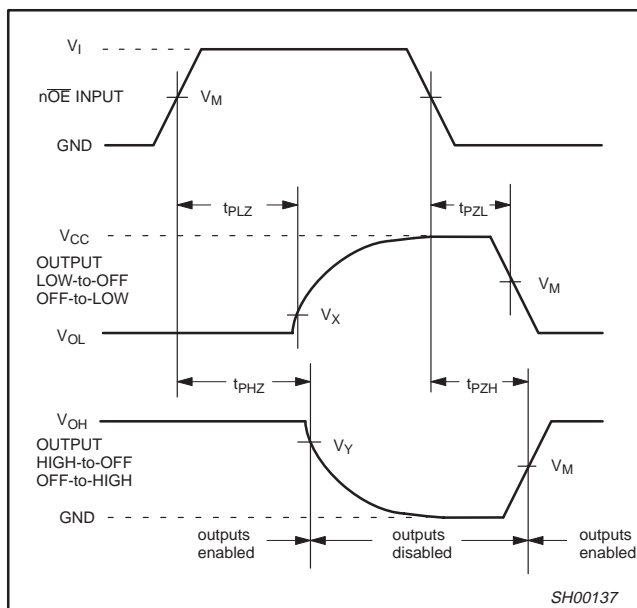
**Waveform 2.** Latch enable input (LE) pulse width, the latch enable input to output (Qn) propagation delay



**Waveform 3.** Data set-up and hold times for the Dn input to the LE input



**Waveform 4.** Clear (CLR) and preset (PRE) pulse width, the clear (CLR) and preset (PRE) to latch (LE) removal time

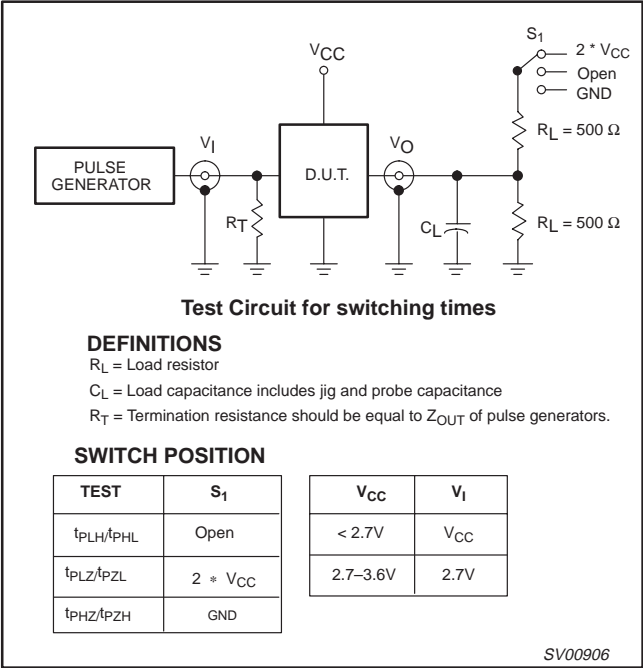


**Waveform 5.** 3-State enable and disable times

18-bit bus interface D-type latch (3-State)

74ALVCH16843

TEST CIRCUIT



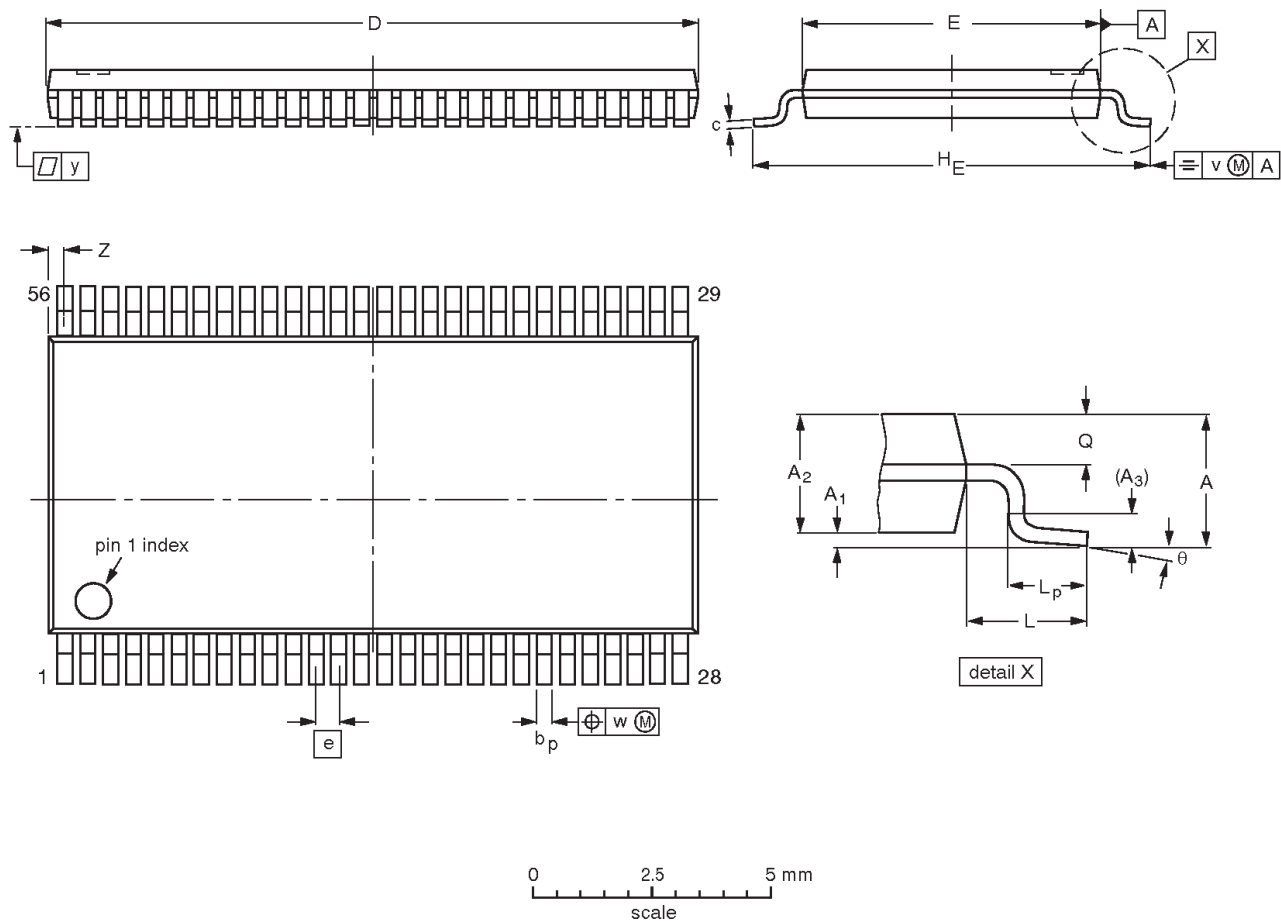
Waveform 6. Load circuitry for switching times

18-bit bus interface D-type latch (3-State)

74ALVCH16843

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT364-1		MO-153EE				<del>93-02-03</del> 95-02-10

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**18-bit bus interface D-type latch (3-State)****74ALVCH16843**

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**NOTES**

## 18-bit bus interface D-type latch (3-State)

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

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print code

Date of release: 07-98

Document order number:

9397-750-04562

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