

DATA SHEET

74F193

Up/down binary counter with separate
up/down clocks

Product specification

1995 Jul 17

IC15 Data Handbook

Up/down binary counter with separate up/down clocks

74F193

FEATURES

- Synchronous reversible 4-bit counting
- Asynchronous parallel load capability
- Asynchronous reset (clear)
- Cascadable without external logic

DESCRIPTION

The 74F193 is a 4-bit synchronous up/down counter in the binary mode. Separate up/down clocks, CP_U and CP_D respectively, simplify operation. The outputs change state synchronously with the Low-to-High transition of either clock input. If the CP_U clock is pulsed while CP_D is held High, the device will count up. If CP_D clock is pulsed while CP_U is held High, the device will count down. The device can be cleared at any time by the asynchronous reset pin. It may also be loaded in parallel by activating the asynchronous parallel load pin.

Inside the device are four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, asynchronous preset, load, and synchronous count up and count down functions.

Each flip-flop contains JK feedback from slave to master, such that a Low-to-High transition on the CP_D input will decrease the count by one, while a similar transition on the CP_U input will advance the count by one.

One clock should be held High while counting with the other, because the circuit will either count by twos or not at all, depending on the state of the first JK flip-flop, which cannot toggle as long as either clock input is Low. Applications requiring reversible operation must make the reversing decision while the activating clock is High to avoid erroneous counts.

The Terminal Count Up (\overline{TC}_U) and Terminal Count Down (\overline{TC}_D) outputs are normally High. When the circuit has reached the maximum count state of 15, the next High-to-Low transition of CP_U will cause \overline{TC}_U to go Low. \overline{TC}_U will stay Low until CP_U goes High again, duplicating the count up clock, although delayed by two gate delays. Likewise, the \overline{TC}_D output will go Low when the circuit is in the zero state and the CP_D goes Low. The \overline{TC} outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms.

Multistage counters will not be fully synchronous since there is a two-gate delay time difference added for each stage that is added.

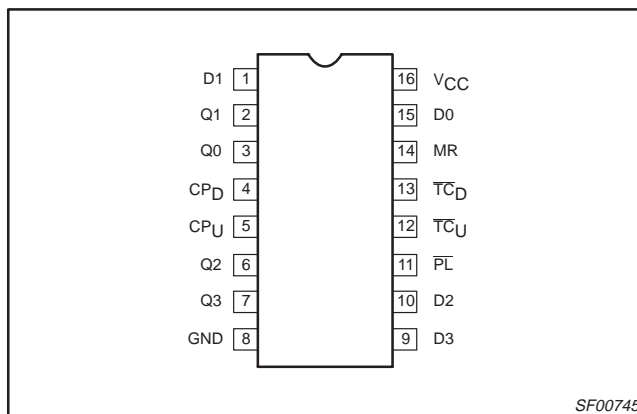
The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel Data inputs (D0 - D3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs when the Parallel Load (\overline{PL}) input is Low. A High level on the Master Reset (\overline{MR}) input will disable the parallel load gates, override both clock inputs, and set all Q outputs Low. If one of the clock inputs is Low during and after a reset or load operation, the next Low-to-High transition of the clock will be interpreted as a legitimate signal and will be counted.

| TYPE | TYPICAL f_{MAX} | TYPICAL SUPPLY CURRENT (TOTAL) |
|--------|-------------------|--------------------------------|
| 74F193 | 125MHz | 32mA |

ORDERING INFORMATION

| DESCRIPTION | COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^\circ C$ to $+70^\circ C$ | PKG DWG # |
|--------------------|--|-----------|
| 16-pin plastic DIP | N74F193N | SOT38-4 |
| 16-pin plastic SO | N74F193D | SOT109-1 |

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

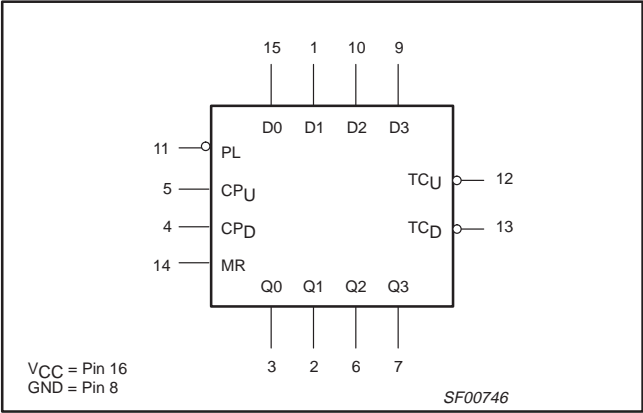
| PINS | DESCRIPTION | 74F(U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|-------------------|---|--------------------|---------------------|
| D0 - D3 | Data inputs | 1.0/1.0 | 20 μ A/0.6mA |
| CP_U | Count up clock input (active rising edge) | 1.0/3.0 | 20 μ A/1.8mA |
| CP_D | Count down clock input (active rising edge) | 1.0/3.0 | 20 μ A/1.8mA |
| \overline{PL} | Asynchronous parallel load control input (active Low) | 1.0/1.0 | 20 μ A/0.6mA |
| MR | Asynchronous master reset input | 1.0/1.0 | 20 μ A/0.6mA |
| Q0 - Q3 | Flip-flop outputs | 50/33 | 1.0mA/20mA |
| \overline{TC}_U | Terminal count up (carry) output (active Low) | 50/33 | 1.0mA/20mA |
| \overline{TC}_D | Terminal count down (borrow) output (active Low) | 50/33 | 1.0mA/20mA |

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20 μ A in the High state and 0.6mA in the Low state.

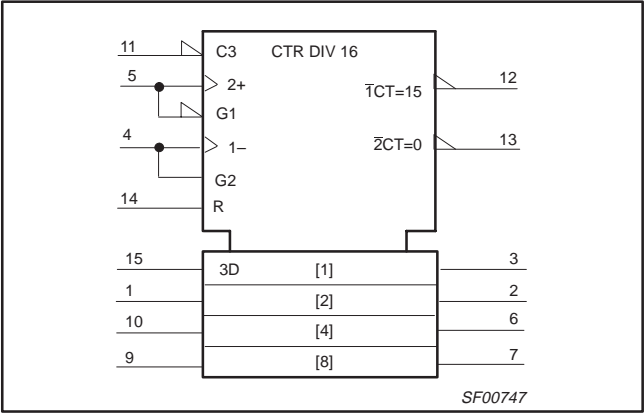
Up/down binary counter with separate up/down clocks

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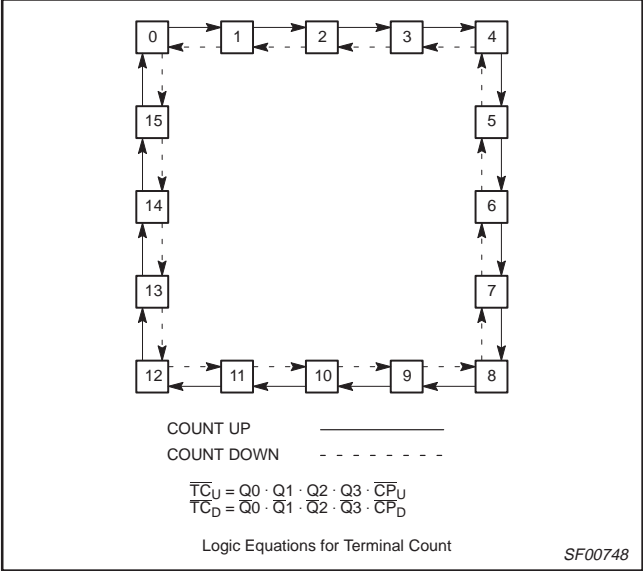
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



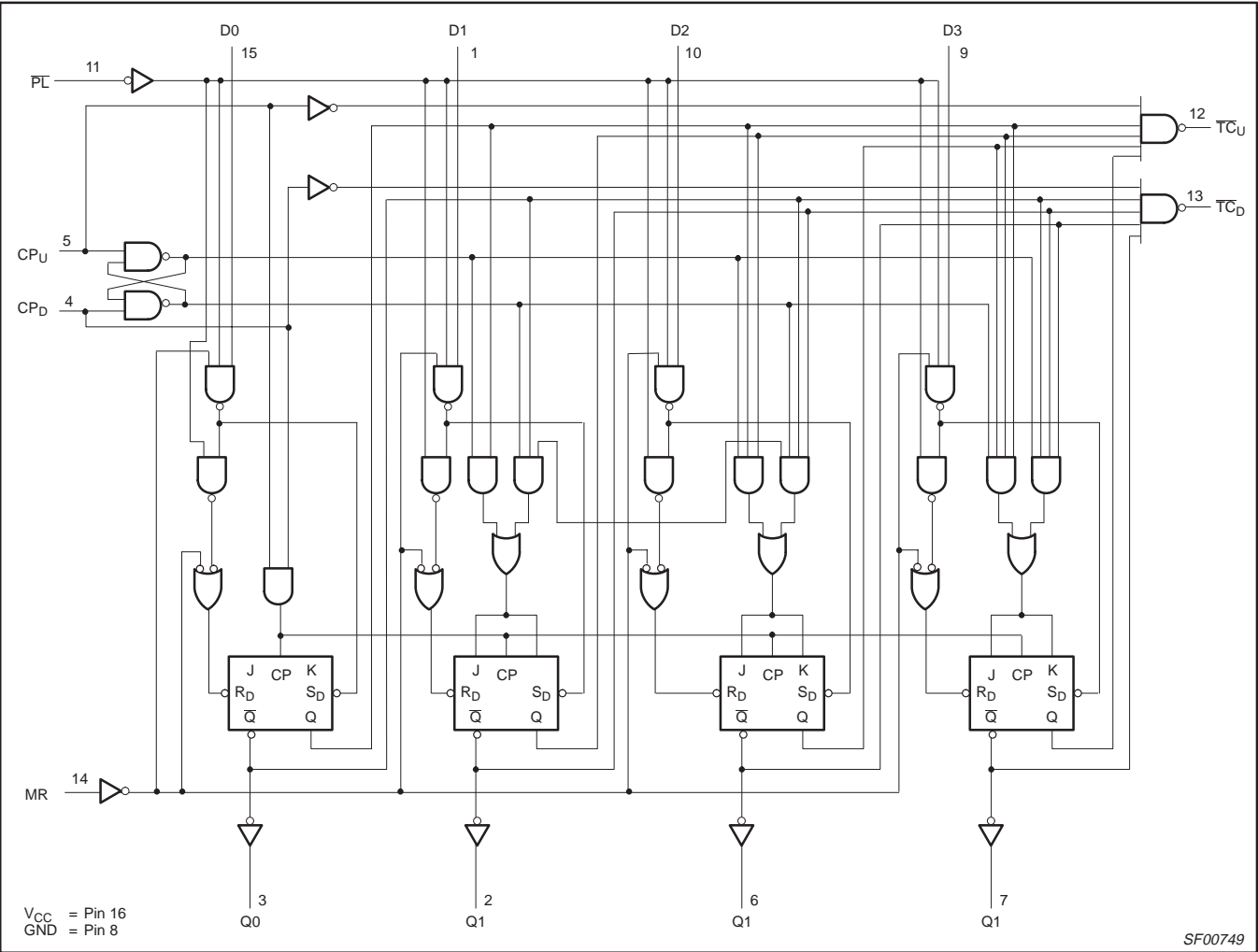
STATE DIAGRAM



Up/down binary counter with separate up/down clocks

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LOGIC DIAGRAM



FUNCTION TABLE

| INPUTS | | | | | | | | OUTPUTS | | | | | | OPERATING MODE | |
|------------------|------------------------|------------------------|------------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|-----------------------------------|-----------------------------------|-------------------|---------------|
| MR | $\overline{\text{PL}}$ | CP_{U} | CP_{D} | D0 | D1 | D2 | D3 | Q0 | Q1 | Q2 | Q3 | $\overline{\text{TC}}_{\text{U}}$ | $\overline{\text{TC}}_{\text{D}}$ | | |
| H H | X X | X X | L H | X X | X X | X X | X X | L L | L L | L L | L L | H H | L H | Reset (clear) | |
| L L L L | L L L L | X X L H | L H X X | L L H H | L L H H | L L H H | L L H H | L L H H | L L H H | L L H H | L L H H | H H L H | L H H H | | Parallel load |
| L | H | ↑ | H | X | X | X | X | Count up | | | | H ¹ | H | Count up | |
| L | H | H | ↑ | X | X | X | X | Count down | | | | H | H ² | Count down | |

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

NOTES:
TC_U=CP_U at terminal count up (HHHH)
TC_D=CP_D at terminal count down (LLLL)

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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

| SYMBOL | PARAMETER | RATING | UNIT |
|-----------|--|------------------|------|
| V_{CC} | Supply voltage | -0.5 to +7.0 | V |
| V_{IN} | Input voltage | -0.5 to +7.0 | V |
| I_{IN} | Input current | -30 to +5.0 | mA |
| V_{OUT} | Voltage applied to output in High output state | -0.5 to V_{CC} | V |
| I_{OUT} | Current applied to output in Low output state | 40 | mA |
| T_{amb} | Operating free-air temperature range | 0 to +70 | °C |
| T_{stg} | Storage temperature | -65 to +150 | °C |

RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|-----------|--------------------------------------|--------|-----|-----|------|
| | | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| V_{IH} | High-level input voltage | 2.0 | | | V |
| V_{IL} | Low-level input voltage | | | 0.8 | V |
| I_{IK} | Input clamp current | | | -18 | mA |
| I_{OH} | High-level output current | | | -1 | mA |
| I_{OL} | Low-level output current | | | 20 | mA |
| T_{amb} | Operating free-air temperature range | 0 | | +70 | °C |

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | | TEST CONDITIONS ^{NO TAG} | LIMITS | | | UNIT |
|----------|--|-----------------------------------|--|------------------|---------------|------|---------------|
| | | | | MIN | TYP NO TAG | MAX | |
| V_{OH} | High-level output voltage | | $V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = \text{MAX}, V_{IH} = \text{MIN}$ | $\pm 10\%V_{CC}$ | 2.5 | | V |
| | | | | $\pm 5\%V_{CC}$ | 2.7 | 3.4 | V |
| V_{OL} | Low-level output voltage | | $V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OL} = \text{MAX}, V_{IH} = \text{MIN}$ | $\pm 10\%V_{CC}$ | | 0.35 | V |
| | | | | $\pm 5\%V_{CC}$ | | 0.35 | V |
| V_{IK} | Input clamp voltage | | $V_{CC} = \text{MIN}, I_I = I_{IK}$ | | -0.73 | -1.2 | V |
| I_I | Input current at maximum input voltage | | $V_{CC} = \text{MAX}, V_I = 7.0\text{V}$ | | | 100 | μA |
| I_{IH} | High-level input current | | $V_{CC} = \text{MAX}, V_I = 2.7\text{V}$ | | | 20 | μA |
| I_{IL} | Low-level input current | CP _U , CP _D | $V_{CC} = \text{MAX}, V_I = 0.5\text{V}$ | | | -1.8 | mA |
| | | Others | | | | -0.6 | mA |
| I_{OS} | Short-circuit output current ^{NO TAG} | | $V_{CC} = \text{MAX}$ | -60 | | -150 | mA |
| I_{CC} | Supply current (total) ⁴ | | $V_{CC} = \text{MAX}$ | | 32 | 50 | mA |

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_{amb} = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- Measure I_{CC} with parallel load and Master reset inputs grounded, all other inputs at 4.5V and all outputs open.

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AC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | | | UNIT |
|--------------------------------------|---|-----------------|---|------------|--------------|--|--------------|----------|
| | | | T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω | | | T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω | | |
| | | | MIN | TYP | MAX | MIN | MAX | |
| f _{MAX} | Maximum clock frequency | Waveform 1 | 100 | 125 | | 90 | | MHz |
| t _{PLH} t _{PHL} | Propagation delay CP _U or CP _D to \overline{TC}_U or \overline{TC}_D | Waveform 2 | 2.5 3.0 | 5.5 5.0 | 8.5 8.0 | 2.5 3.0 | 9.0 9.0 | ns ns |
| t _{PLH} t _{PHL} | Propagation delay CP _U or CP _D to Q _n | Waveform 1 | 2.5 5.0 | 5.5 8.5 | 8.5 12.0 | 2.5 5.0 | 9.0 13.0 | ns ns |
| t _{PLH} t _{PHL} | Propagation delay D _n to Q _n | Waveform 4 | 2.0 6.0 | 4.0 9.5 | 7.0 13.5 | 1.5 6.0 | 8.0 15.0 | ns ns |
| t _{PLH} t _{PHL} | Propagation delay \overline{PL} to Q _n | Waveform 3 | 4.5 5.5 | 6.5 8.5 | 10.0 12.0 | 4.0 5.0 | 11.0 13.0 | ns ns |
| t _{PHL} | Propagation delay MR to Q _n | Waveform 5 | 5.0 | 7.5 | 11.0 | 5.0 | 12.0 | ns |
| t _{PLH} | Propagation delay MR to \overline{TC}_U | Waveform 5 | 6.0 | 8.5 | 12.0 | 5.5 | 13.0 | ns |
| t _{PHL} | Propagation delay MR to \overline{TC}_D | Waveform 5 | 5.0 | 7.5 | 11.0 | 5.0 | 12.0 | ns |
| t _{PLH} t _{PHL} | Propagation delay \overline{PL} to \overline{TC}_U or \overline{TC}_D | Waveform 3 | 6.0 6.0 | 9.5 9.0 | 13.5 12.0 | 6.0 6.0 | 15.0 13.0 | ns ns |
| t _{PLH} t _{PHL} | Propagation delay D _n to \overline{TC}_U or \overline{TC}_D | Waveform 4 | 5.5 4.5 | 9.0 8.5 | 13.0 12.5 | 5.0 4.5 | 14.0 13.5 | ns ns |

AC SETUP REQUIREMENTS

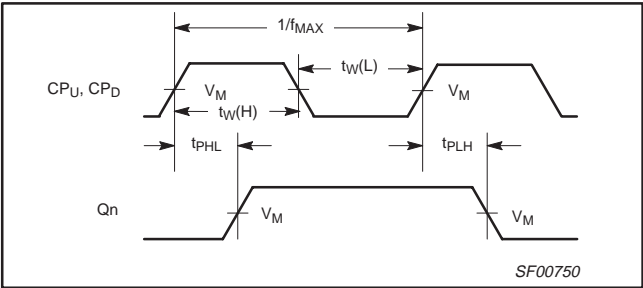
| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | | | UNIT |
|--|---|-----------------|---|-----|-----|--|-----|----------|
| | | | T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω | | | T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω | | |
| | | | MIN | TYP | MAX | MIN | MAX | |
| t _s (H) t _s (L) | Setup time, High or Low Dn to \overline{PL} | Waveform 6 | 4.5 4.5 | | | 5.0 5.0 | | ns ns |
| t _h (H) t _h (L) | Hold time, High or Low Dn to \overline{PL} | Waveform 6 | 2.0 2.0 | | | 2.0 2.0 | | ns ns |
| t _w (L) | \overline{PL} Pulse width Low | Waveform 3 | 6.0 | | | 6.0 | | ns |
| t _w (H) t _w (L) | CP _U or CP _D Pulse width High or Low | Waveform 1 | 3.5 5.0 | | | 3.5 5.0 | | ns ns |
| t _w (L) | CP _U or CP _D Pulse width Low (Change of direction) | Waveform 1 | 10.0 | | | 10.0 | | ns |
| t _w (H) | MR Pulse width High | Waveform 5 | 6.0 | | | 6.0 | | ns |
| t _{rec} | Recovery time, \overline{PL} to CP _U or CP _D | Waveform 3 | 6.0 | | | 6.0 | | ns |
| t _{rec} | Recovery time MR to CP _U or CP _D | Waveform 5 | 4.0 | | | 4.0 | | ns |

Up/down binary counter with separate up/down clocks

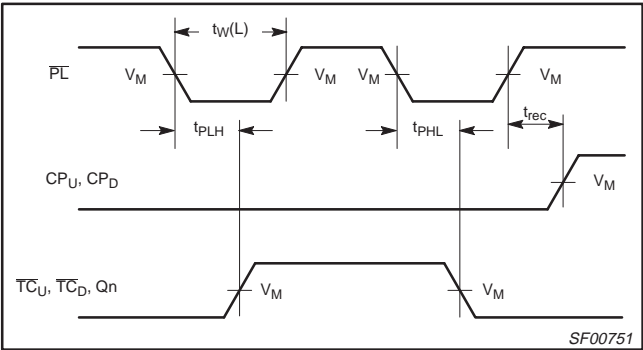
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AC WAVEFORMS

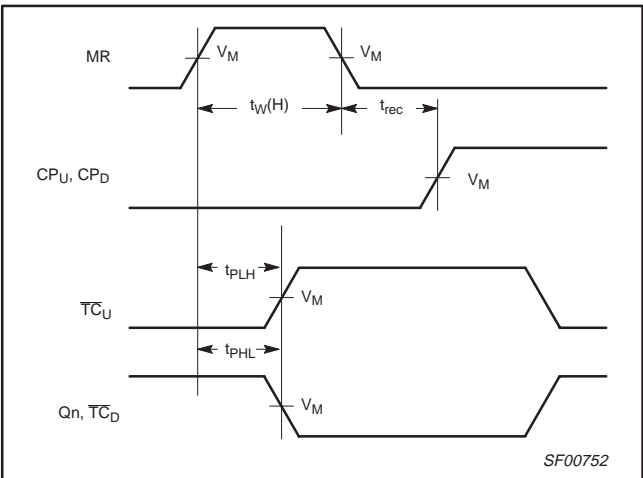
For all waveforms $V_M = 1.5V$



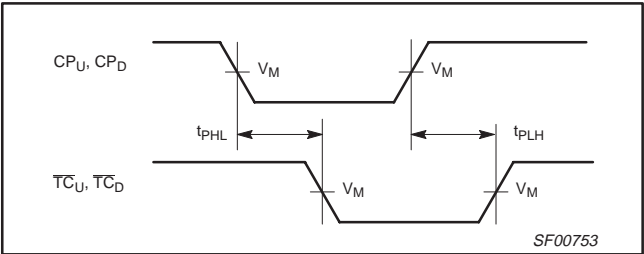
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width and Maximum Clock Frequency



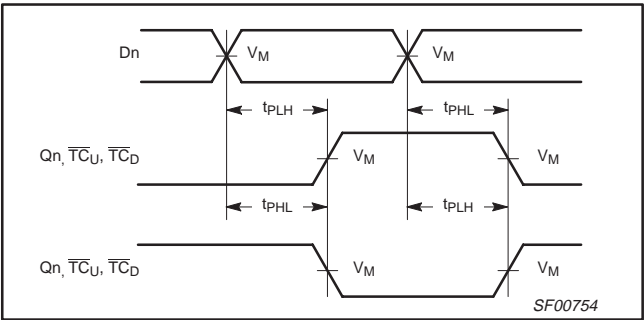
Waveform 3. Parallel Pulse Width, Parallel Load to Output Delays, and Parallel Load to Clock Recovery Time



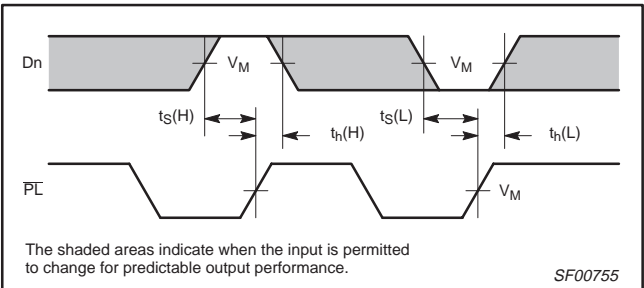
Waveform 5. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Waveform 2. Propagation Delay, Clock to Terminal Count



Waveform 4. Propagation Delay, Data to Flip-Flop Outputs, Terminal Count Up and Down Outputs

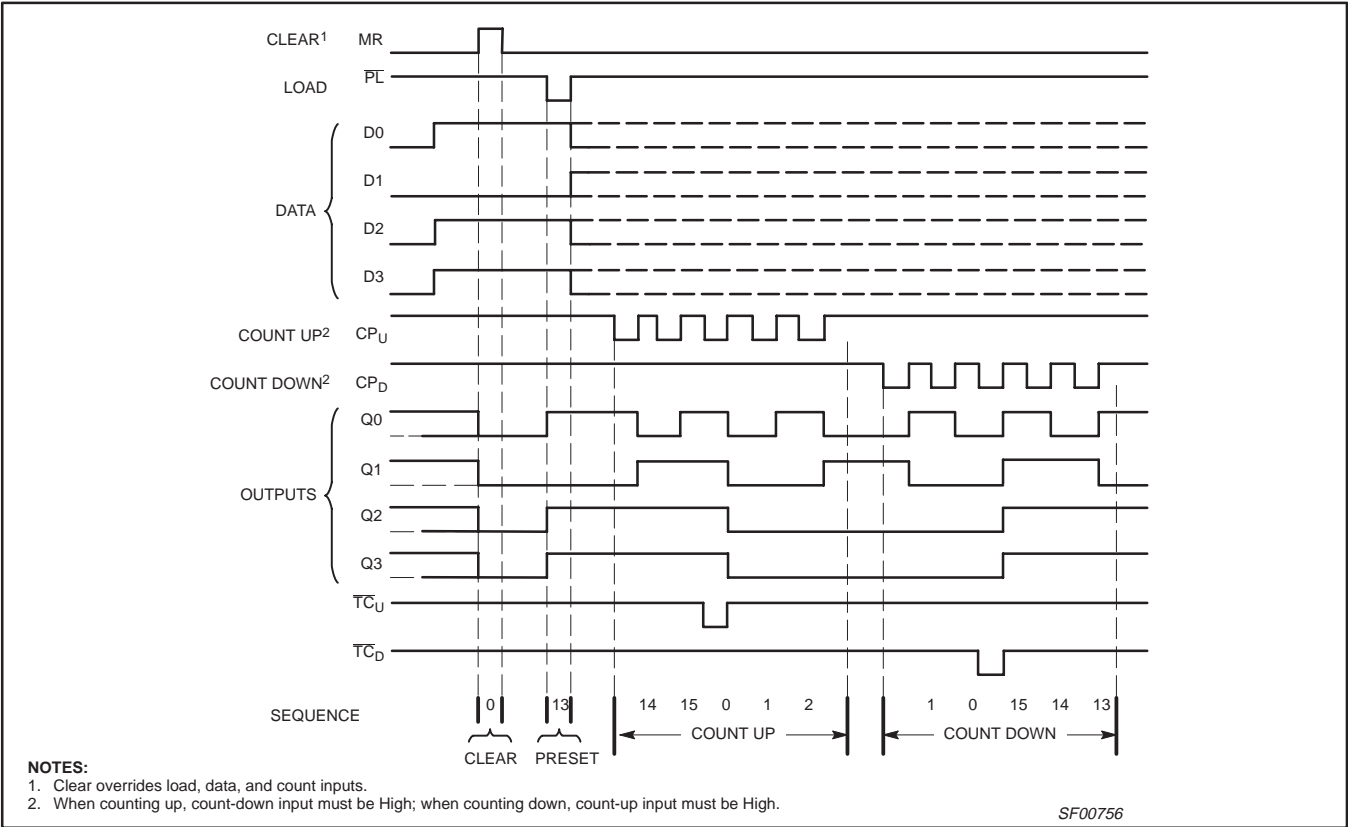


Waveform 6. Data Setup and Hold Times

Up/down binary counter with separate up/down clocks

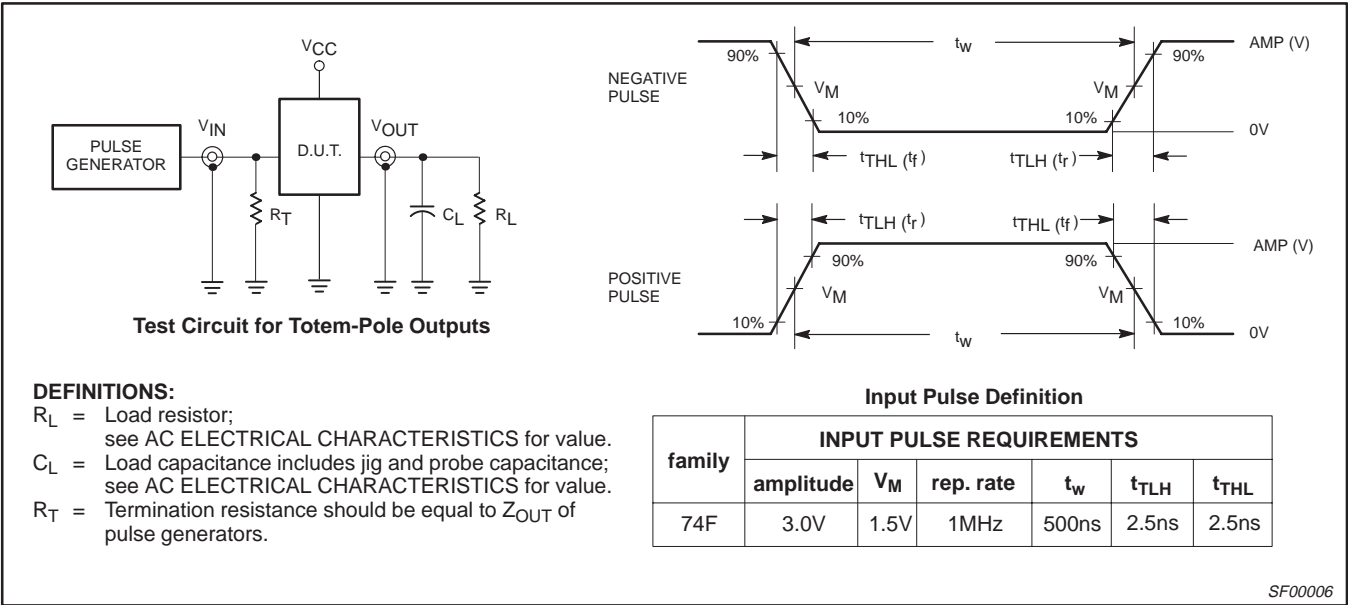
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Timing Diagram (Typical clear, load, and count sequence)



Binary Counter

TEST CIRCUIT AND WAVEFORMS

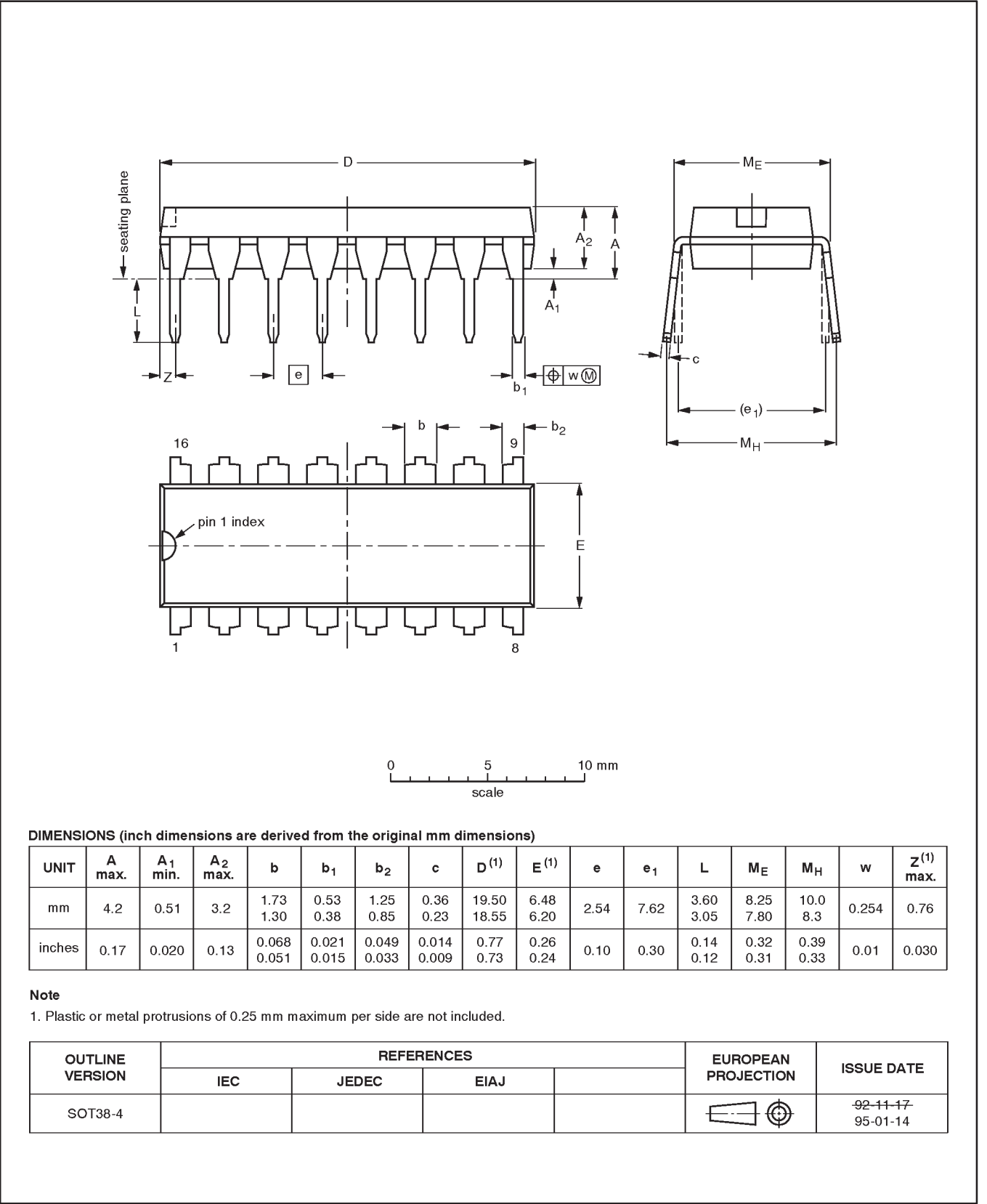


Up/down binary counter with separate up/down clocks

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DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

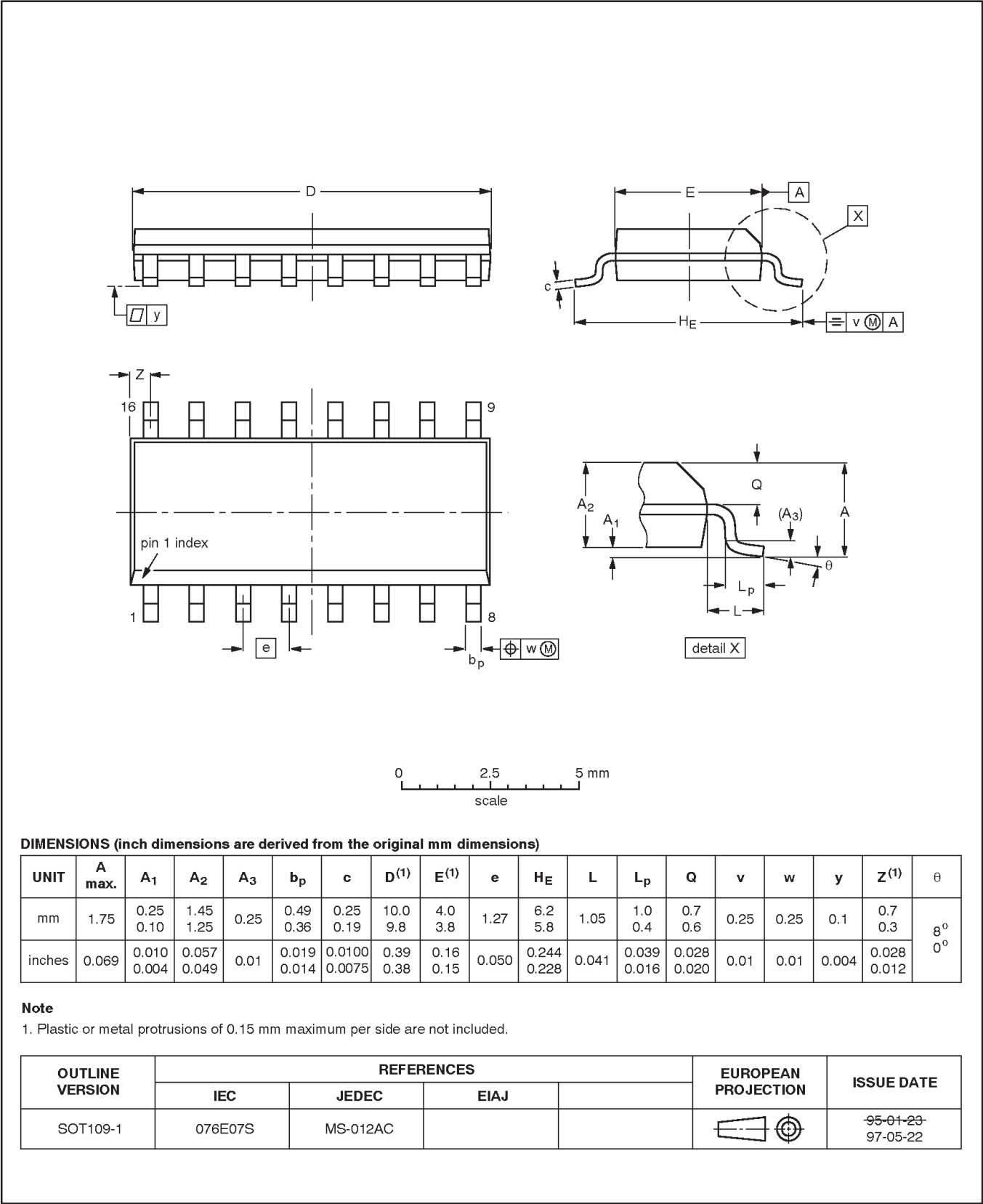


Up/down binary counter with separate up/down clocks

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



Up/down binary counter with separate up/down clocks

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NOTES

Up/down binary counter with separate up/down clocks

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Data sheet status

| Data sheet status | Product status | Definition [1] |
|---------------------------|----------------|--|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
| Preliminary specification | Qualification | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| Product specification | Production | This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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