

74HC107; 74HCT107

Dual JK flip-flop with reset; negative-edge trigger

Rev. 4 — 26 January 2015

Product data sheet

1. General description

The 74HC107; 74HCT107 is a dual negative edge triggered JK flip-flop featuring individual J and K inputs, clock (\overline{CP}) and reset (\overline{R}) inputs and complementary Q and \overline{Q} outputs. The reset is an asynchronous active LOW input and operates independently of the clock input. The J and K inputs control the state changes of the flip-flops as described in the mode select function table. The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Complies with JEDEC standard no. 7A
- Input levels:
 - ◆ The 74HC107: CMOS levels
 - ◆ The 74HCT107: TTL levels
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

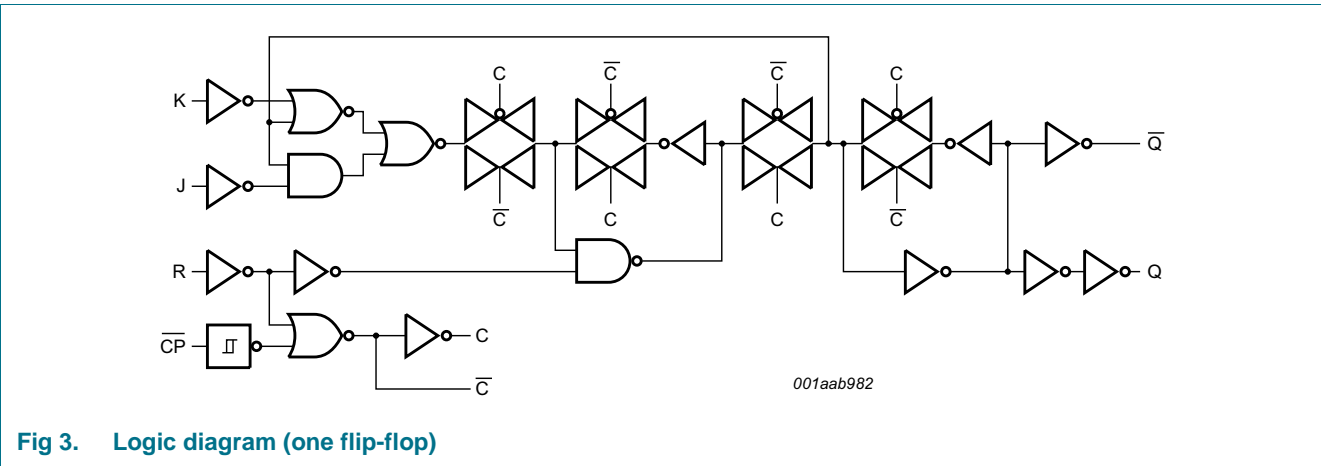
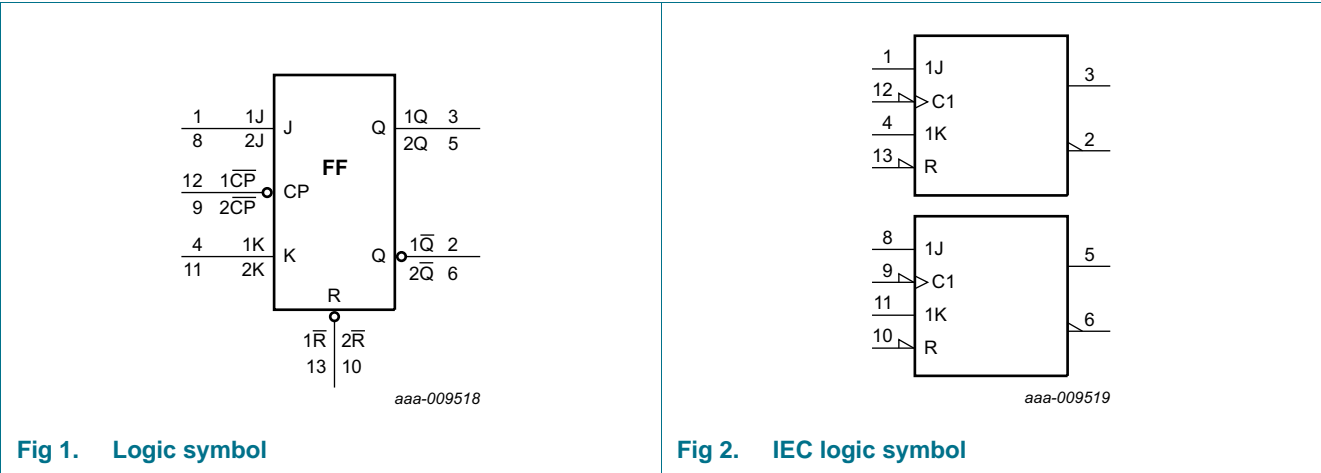
3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|-------------|---|---------|--|----------|
| | Temperature range | Name | Description | Version |
| 74HC107N | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | DIP14 | plastic dual in-line package; 14 leads (300 mil) | SOT27-1 |
| 74HCT107N | | | | |
| 74HC107D | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| 74HCT107D | | | | |
| 74HC107DB | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | SSOP14 | plastic shrink small outline package; 14 leads; body width 5.3 mm | SOT337-1 |
| 74HC107PW | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |



4. Functional diagram



5. Pinning information

5.1 Pinning

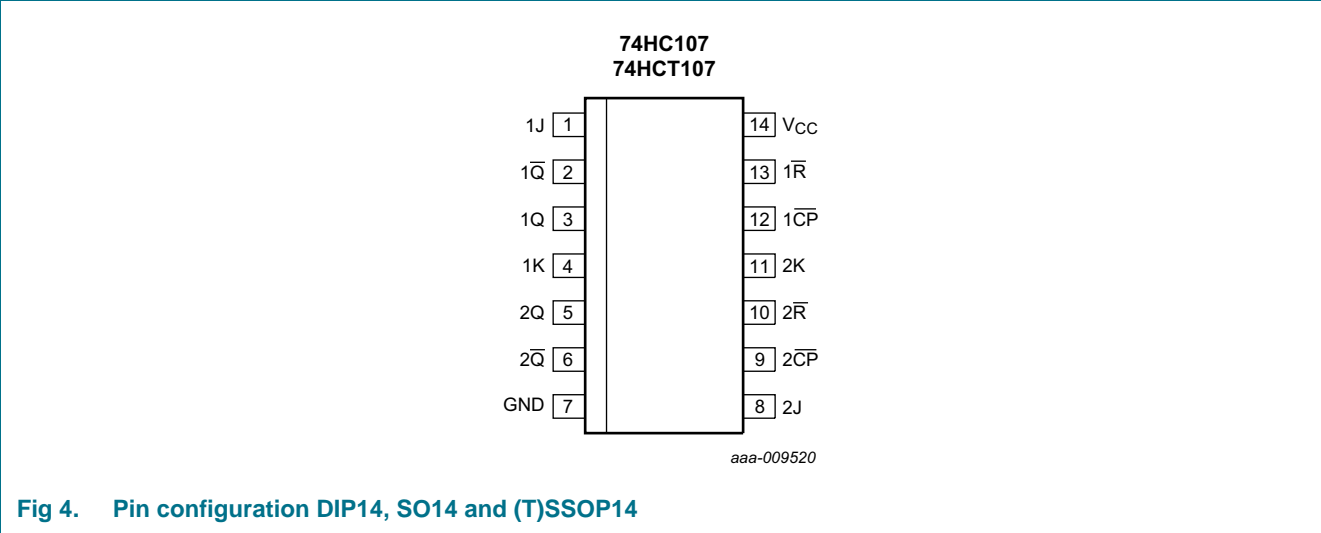


Fig 4. Pin configuration DIP14, SO14 and (T)SSOP14

5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|------------|--------|--|
| 1J, 2J | 1, 8 | synchronous J input |
| 1Q̄, 2Q̄ | 2, 6 | complement output |
| 1Q, 2Q | 3, 5 | true output |
| 1K, 2K | 4, 11 | synchronous K input |
| 1CP̄, 2CP̄ | 12, 9 | clock input (HIGH-to-LOW edge-triggered) |
| 1R̄, 2R̄ | 13, 10 | asynchronous reset input (active LOW) |
| GND | 7 | ground (0 V) |
| VCC | 14 | supply voltage |

6. Functional description

Table 3. Function table^[1]

| Input | | | | Output | | Operating mode |
|----------------|-----------------|---|---|----------------|----------------|--------------------|
| \overline{R} | \overline{CP} | J | K | Q | \overline{Q} | |
| L | X | X | X | L | H | asynchronous reset |
| H | ↓ | h | h | \overline{q} | q | toggle |
| H | ↓ | l | h | L | H | load 0 (reset) |
| H | ↓ | h | l | H | L | load 1 (set) |
| H | ↓ | l | l | q | \overline{q} | hold (no change) |

- [1] H = HIGH voltage level;
 h = HIGH voltage level one set-up time prior to the HIGH-to-LOW clock transition;
 L = LOW voltage level;
 l = LOW voltage level one set-up time prior to the HIGH-to-LOW clock transition;
 q = state of referenced output one set-up time prior to the HIGH-to-LOW clock transition;
 X = don't care;
 ↓ = HIGH-to-LOW clock transition.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|---|------|------|------|
| V_{CC} | supply voltage | | -0.5 | +7.0 | V |
| I_{IK} | input clamping current | $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ ^[1] | - | ±20 | mA |
| I_{OK} | output clamping current | $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ ^[1] | - | ±20 | mA |
| I_O | output current | $V_O = -0.5\text{ V}$ to $V_{CC} + 0.5\text{ V}$ | - | ±25 | mA |
| I_{CC} | supply current | | - | 50 | mA |
| I_{GND} | ground current | | -50 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ | | | |
| | | DIP14 package ^[2] | - | 750 | mW |
| | | SO14 package ^[3] | - | 500 | mW |
| | | (T)SSOP14 package ^[4] | - | 500 | mW |

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 [2] P_{tot} derates linearly with 12 mW/K above 70 °C.
 [3] P_{tot} derates linearly with 8 mW/K above 70 °C.
 [4] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

| Symbol | Parameter | Conditions | 74HC107 | | | 74HCT107 | | | Unit |
|------------------|-------------------------------------|-------------------------|---------|------|-----------------|----------|------|-----------------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V _{CC} | supply voltage | | 2.0 | 5.0 | 6.0 | 4.5 | 5.0 | 5.5 | V |
| V _I | input voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| V _O | output voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| T _{amb} | ambient temperature | | -40 | +25 | +125 | -40 | +25 | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | V _{CC} = 2.0 V | - | - | 625 | - | - | - | ns/V |
| | | V _{CC} = 4.5 V | - | 1.67 | 139 | - | 1.67 | 139 | ns/V |
| | | V _{CC} = 6.0 V | - | - | 83 | - | - | - | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | −40 °C to +85 °C | | −40 °C to +125 °C | | Unit |
|-----------------|---------------------------|--|-------|------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HC107 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | 1.2 | - | 1.5 | - | 1.5 | - | V |
| | | V _{CC} = 4.5 V | 3.15 | 2.4 | - | 3.15 | - | 3.15 | - | V |
| | | V _{CC} = 6.0 V | 4.2 | 3.2 | - | 4.2 | - | 4.2 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | 0.8 | 0.5 | - | 0.5 | - | 0.5 | V |
| | | V _{CC} = 4.5 V | - | 2.1 | 1.35 | - | 1.35 | - | 1.35 | V |
| | | V _{CC} = 6.0 V | - | 2.8 | 1.8 | - | 1.8 | - | 1.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = −20 μA; V _{CC} = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | I _O = −20 μA; V _{CC} = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = −20 μA; V _{CC} = 6.0 V | 5.9 | 6.0 | - | 5.9 | - | 5.9 | - | V |
| | | I _O = −4.0 mA; V _{CC} = 4.5 V | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| | | I _O = −5.2 mA; V _{CC} = 6.0 V | 5.48 | 5.81 | - | 5.34 | - | 5.2 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = 20 μA; V _{CC} = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 6.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 4.0 mA; V _{CC} = 4.5 V | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| | | I _O = 5.2 mA; V _{CC} = 6.0 V | - | 0.16 | 0.26 | - | 0.33 | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±0.1 | - | ±1.0 | - | ±1.0 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V | - | - | 4.0 | - | 40 | - | 80 | μA |

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|------------------|---------------------------|--|-------|------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| C _I | input capacitance | | - | 3.5 | - | | | | | pF |
| 74HCT107 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | 1.6 | - | 2.0 | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | 1.2 | 0.8 | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = –20 µA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = –4 mA | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = 20 µA | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 4.0 mA | - | 0.16 | 0.26 | - | 0.33 | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 5.5 V | - | - | ±0.1 | - | ±1.0 | - | ±1.0 | µA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 4.0 | - | 40 | - | 80 | µA |
| ΔI _{CC} | additional supply current | per input pin; V _I = V _{CC} – 2.1 V; I _O = 0 A; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V | | | | | | | | |
| | | pin nCP, nJ | - | 100 | 360 | - | 450 | - | 490 | µA |
| | | pin nR | - | 65 | 234 | - | 293 | - | 319 | µA |
| | | pin nK | - | 60 | 216 | - | 270 | - | 294 | µA |
| C _I | input capacitance | | - | 3.5 | - | - | - | - | - | pF |

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 7](#)

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|------------------|-------------------|---|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HC107 | | | | | | | | | | |
| t _{pd} | propagation delay | n \overline{CP} to nQ; see Figure 5 ^[1] | | | | | | | | |
| | | V _{CC} = 2.0 V | - | 52 | 160 | - | 200 | - | 240 | ns |
| | | V _{CC} = 4.5 V | - | 19 | 32 | - | 40 | - | 48 | ns |
| | | V _{CC} = 5.0 V; C _L = 15 pF | - | 16 | - | - | - | - | - | ns |
| | | V _{CC} = 6.0 V | - | 15 | 27 | - | 34 | - | 41 | ns |
| | | n \overline{CP} to n \overline{Q} ; see Figure 5 | | | | | | | | |
| | | V _{CC} = 2.0 V | - | 52 | 160 | - | 200 | - | 240 | ns |
| | | V _{CC} = 4.5 V | - | 19 | 32 | - | 40 | - | 48 | ns |
| | | V _{CC} = 5.0 V; C _L = 15 pF | - | 16 | - | - | - | - | - | ns |
| | | V _{CC} = 6.0 V | - | 15 | 27 | - | 34 | - | 41 | ns |
| | | n \overline{R} to nQ, n \overline{Q} ; see Figure 6 | | | | | | | | |
| | | V _{CC} = 2.0 V | - | 52 | 155 | - | 195 | - | 235 | ns |
| | | V _{CC} = 4.5 V | - | 19 | 31 | - | 39 | - | 47 | ns |
| | | V _{CC} = 5.0 V; C _L = 15 pF | - | 16 | - | - | - | - | - | ns |
| | | V _{CC} = 6.0 V | - | 15 | 26 | - | 33 | - | 40 | ns |
| t _t | transition time | nQ, n \overline{Q} ; see Figure 5 ^[2] | | | | | | | | |
| | | V _{CC} = 2.0 V | - | 19 | 75 | - | 95 | - | 110 | ns |
| | | V _{CC} = 4.5 V | - | 7 | 15 | - | 19 | - | 22 | ns |
| | | V _{CC} = 6.0 V | - | 6 | 13 | - | 16 | - | 19 | ns |
| t _w | pulse width | n \overline{CP} input, HIGH or LOW; see Figure 5 | | | | | | | | |
| | | V _{CC} = 2.0 V | 80 | 22 | - | 100 | - | 120 | - | ns |
| | | V _{CC} = 4.5 V | 16 | 8 | - | 20 | - | 24 | - | ns |
| | | V _{CC} = 6.0 V | 14 | 6 | - | 17 | - | 20 | - | ns |
| | | n \overline{R} input, HIGH or LOW; see Figure 6 | | | | | | | | |
| | | V _{CC} = 2.0 V | 80 | 22 | - | 100 | - | 120 | - | ns |
| | | V _{CC} = 4.5 V | 16 | 8 | - | 20 | - | 24 | - | ns |
| | | V _{CC} = 6.0 V | 14 | 6 | - | 17 | - | 20 | - | ns |
| t _{rec} | recovery time | n \overline{R} to n \overline{CP} ; see Figure 6 | | | | | | | | |
| | | V _{CC} = 2.0 V | 60 | 19 | - | 75 | - | 90 | - | ns |
| | | V _{CC} = 4.5 V | 12 | 7 | - | 15 | - | 18 | - | ns |
| | | V _{CC} = 6.0 V | 20 | 6 | - | 13 | - | 15 | - | ns |
| t _{su} | set-up time | nJ, nK to n \overline{CP} ; see Figure 5 | | | | | | | | |
| | | V _{CC} = 2.0 V | 100 | 22 | - | 125 | - | 150 | - | ns |
| | | V _{CC} = 4.5 V | 20 | 8 | - | 25 | - | 30 | - | ns |
| | | V _{CC} = 6.0 V | 17 | 6 | - | 21 | - | 26 | - | ns |

Table 7. Dynamic characteristics ...continuedGND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 7](#)

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|------------------|---|--|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| t _h | hold time | nJ, nK to nCP; see Figure 5 | | | | | | | | |
| | | V _{CC} = 2.0 V | 3 | –6 | - | 3 | - | 3 | - | ns |
| | | V _{CC} = 4.5 V | 3 | –2 | - | 3 | - | 3 | - | ns |
| | | V _{CC} = 6.0 V | 3 | –2 | - | 3 | - | 3 | - | ns |
| f _{max} | maximum frequency | nCP input; see Figure 5 | | | | | | | | |
| | | V _{CC} = 2.0 V | 6 | 23 | - | 4.8 | - | 4.0 | - | MHz |
| | | V _{CC} = 4.5 V | 30 | 70 | - | 24 | - | 20 | - | MHz |
| | | V _{CC} = 5.0 V; C _L = 15 pF | - | 78 | - | - | - | - | - | MHz |
| | | V _{CC} = 6.0 V | 35 | 85 | - | 28 | - | 24 | - | MHz |
| C _{PD} | power dissipation capacitance | per flip-flop; V _I = GND to V _{CC} [3] | - | 30 | - | - | - | - | - | pF |
| 74HCT107 | | | | | | | | | | |
| t _{pd} | propagation delay | nCP to nQ; see Figure 5 [1] | | | | | | | | |
| | | V _{CC} = 4.5 V | - | 19 | 36 | - | 45 | - | 54 | ns |
| | | V _{CC} = 5.0 V; C _L = 15 pF | - | 16 | - | - | - | - | - | ns |
| | | nCP to nQ; see Figure 5 | | | | | | | | |
| | | V _{CC} = 4.5 V | - | 21 | 36 | - | 45 | - | 54 | ns |
| | | V _{CC} = 5.0 V; C _L = 15 pF | - | 18 | - | - | - | - | - | ns |
| | | nR to nQ, nQ; see Figure 6 | | | | | | | | |
| | | V _{CC} = 4.5 V | - | 20 | 38 | - | 48 | - | 57 | ns |
| | V _{CC} = 5.0 V; C _L = 15 pF | - | 17 | - | - | - | - | - | ns | |
| t _t | transition time | nQ, nQ; see Figure 5 [2] | | | | | | | | |
| | | V _{CC} = 4.5 V | - | 7 | 15 | - | 19 | - | 22 | ns |
| t _w | pulse width | nCP input, HIGH or LOW; see Figure 5 | | | | | | | | |
| | | V _{CC} = 4.5 V | 16 | 9 | - | 20 | - | 24 | - | ns |
| | | nR input, HIGH or LOW; see Figure 6 | | | | | | | | |
| | | V _{CC} = 4.5 V | 20 | 11 | - | 25 | - | 30 | - | ns |
| t _{rec} | recovery time | nR to nCP; see Figure 6 | | | | | | | | |
| | | V _{CC} = 4.5 V | 14 | 8 | - | 18 | - | 21 | - | ns |
| t _{su} | set-up time | nJ, nK to nCP; see Figure 5 | | | | | | | | |
| | | V _{CC} = 4.5 V | 20 | 7 | - | 25 | - | 30 | - | ns |
| t _h | hold time | nJ, nK to nCP; see Figure 5 | | | | | | | | |
| | | V _{CC} = 4.5 V | 5 | –2 | - | 5 | - | 5 | - | ns |

Table 7. Dynamic characteristics ...continued

GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 7](#)

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|------------|-------------------------------|--|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| f_{\max} | maximum frequency | nCP input; see Figure 5 | | | | | | | | |
| | | $V_{CC} = 4.5$ V | 30 | 66 | - | 24 | - | 20 | - | MHz |
| | | $V_{CC} = 5.0$ V; $C_L = 15$ pF | - | 73 | - | - | - | - | - | MHz |
| C_{PD} | power dissipation capacitance | per flip-flop; $V_I = \text{GND to } V_{CC} - 1.5$ V [3] | - | 30 | - | - | - | - | - | pF |

[1] t_{pd} is the same as t_{PHL} , t_{PLH} .

[2] t_t is the same as t_{THL} , t_{TLH} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

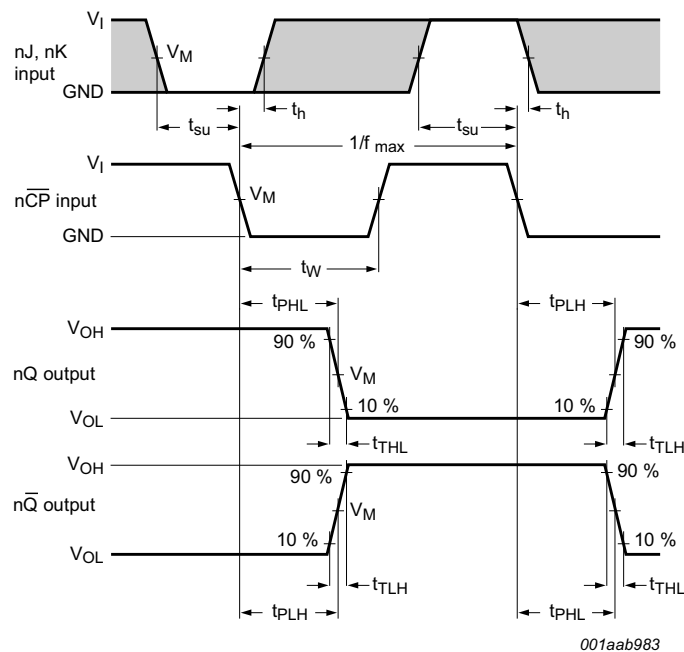
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms

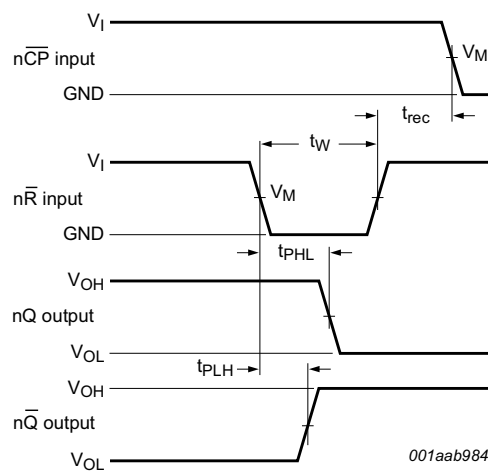


The shaded areas indicate when the input is permitted to change for predictable output performance.

Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. Clock propagation delays, pulse width, set-up and hold times, output transition times and the maximum frequency



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Reset propagation delays, pulse width and recovery time

Table 8. Measurement points

| Type | Input | | Output |
|----------|----------|-------------|-------------|
| | V_I | V_M | V_M |
| 74HC107 | V_{CC} | $0.5V_{CC}$ | $0.5V_{CC}$ |
| 74HCT107 | 3 V | 1.3 V | 1.3 V |

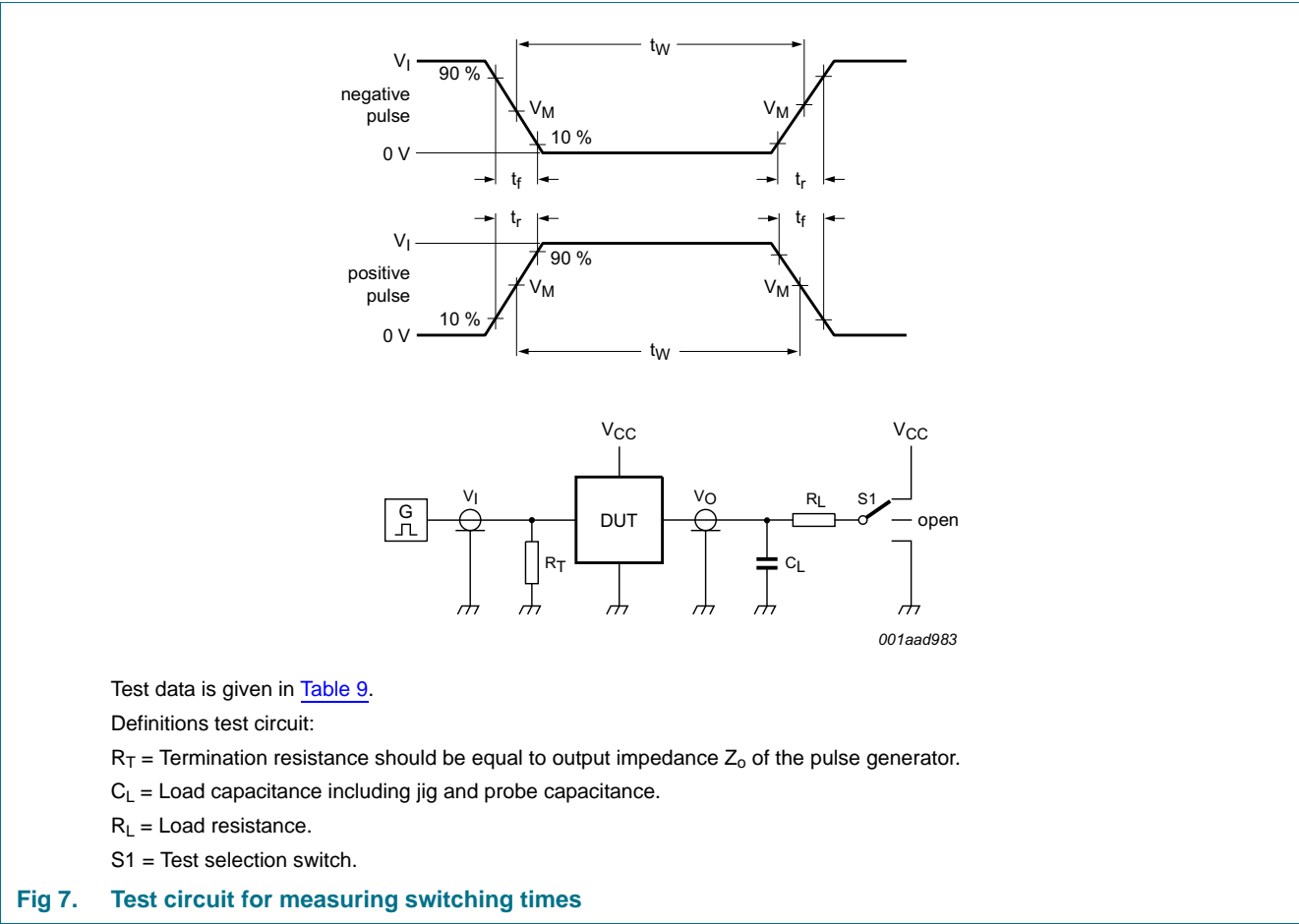


Table 9. Test data

| Type | Input | | Load | | S1 position | | |
|----------|----------|------------|--------------|--------------|--------------------|--------------------|--------------------|
| | V_I | t_r, t_f | C_L | R_L | t_{PHL}, t_{PLH} | t_{PZH}, t_{PHZ} | t_{PZL}, t_{PLZ} |
| 74HC107 | V_{CC} | 6 ns | 15 pF, 50 pF | 1 k Ω | open | GND | V_{CC} |
| 74HCT107 | 3 V | 6 ns | 15 pF, 50 pF | 1 k Ω | open | GND | V_{CC} |

12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

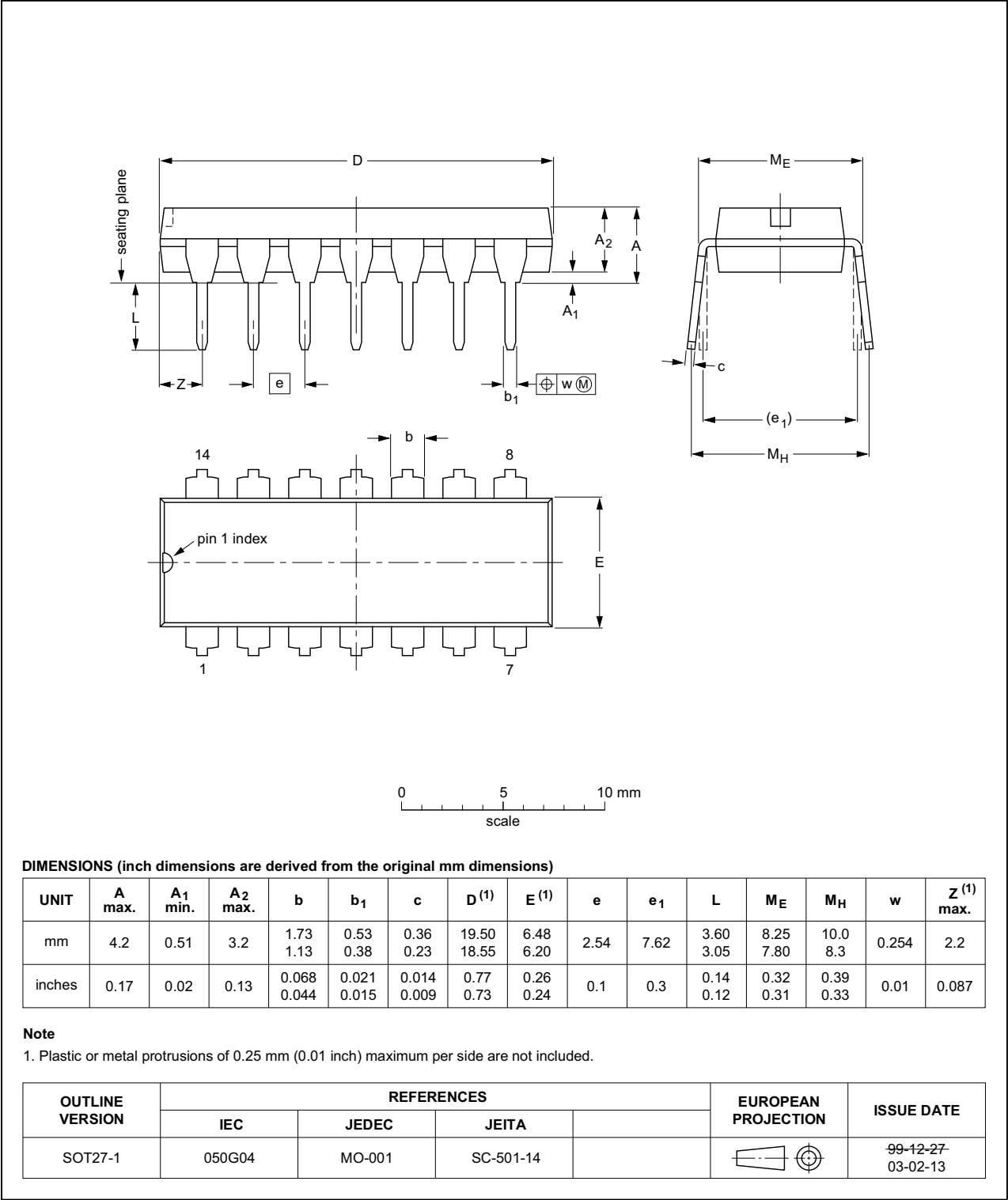


Fig 8. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

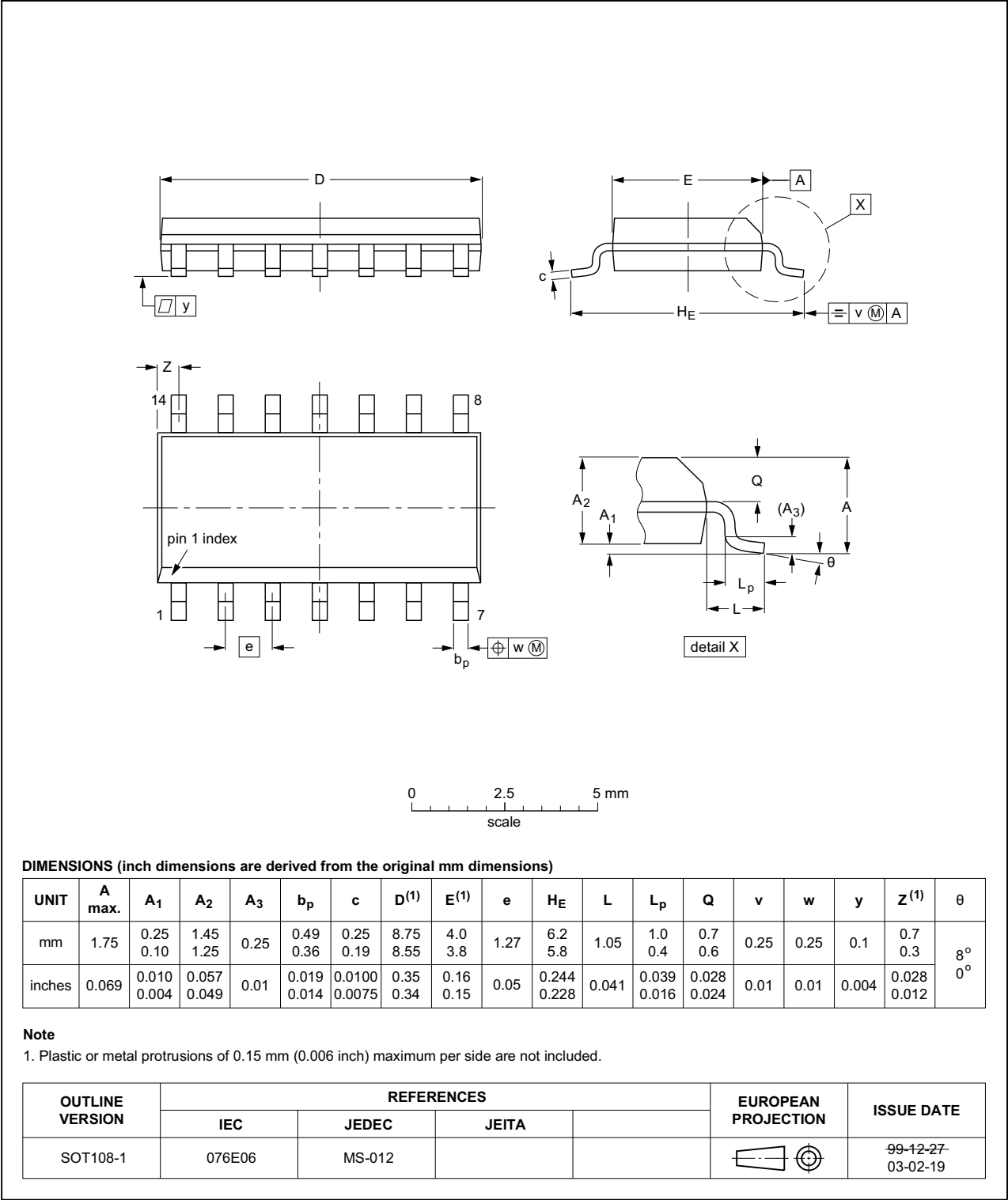


Fig 9. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

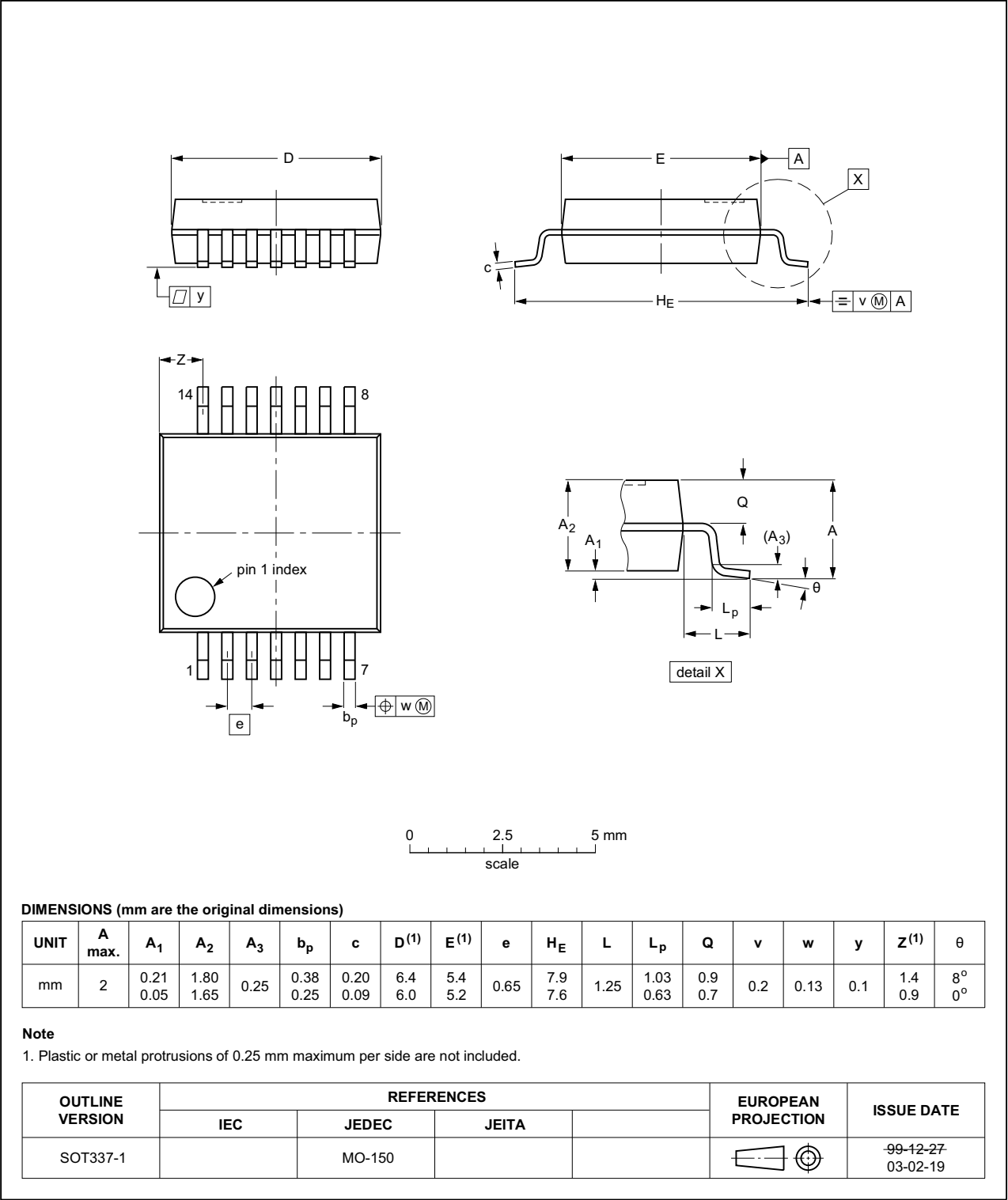
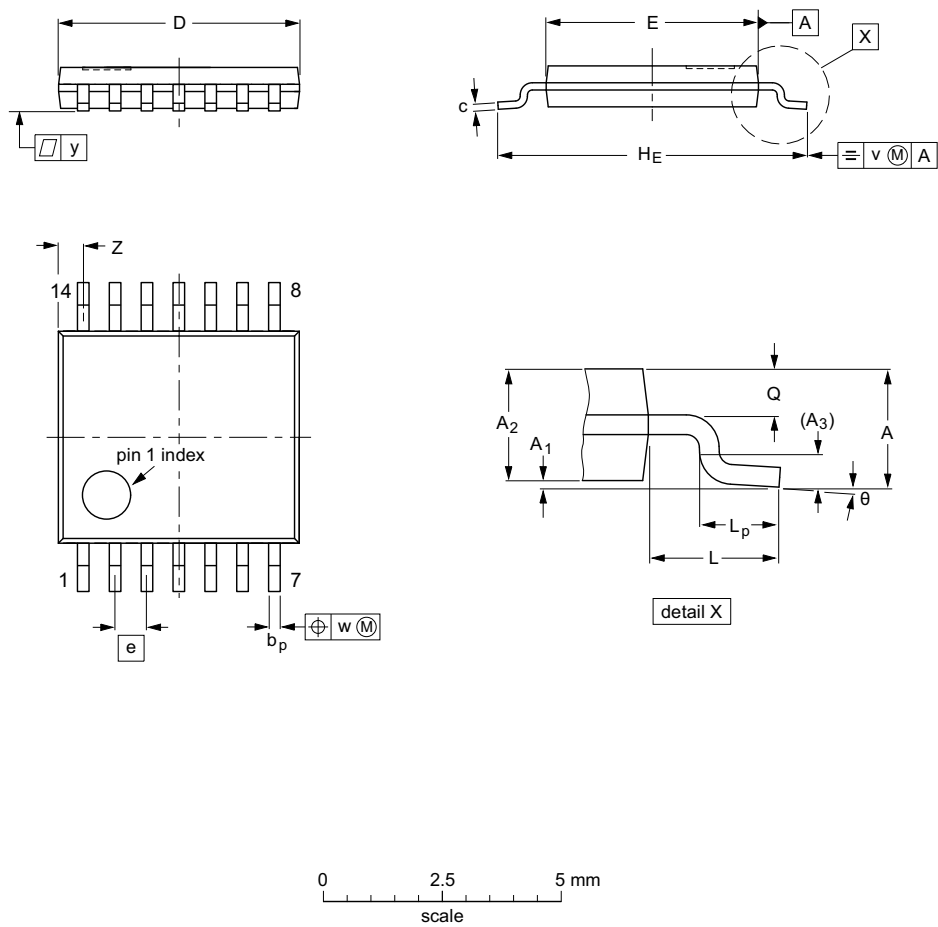


Fig 10. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽²⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|------|-----------|----------------|----------------|----------------|----------------|------------|------------------|------------------|------|----------------|---|----------------|------------|-----|------|-----|------------------|----------|
| mm | 1.1 | 0.15 0.05 | 0.95 0.80 | 0.25 | 0.30 0.19 | 0.2 0.1 | 5.1 4.9 | 4.5 4.3 | 0.65 | 6.6 6.2 | 1 | 0.75 0.50 | 0.4 0.3 | 0.2 | 0.13 | 0.1 | 0.72 0.38 | 8° 0° |

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|--------------------|------------|--------|-------|--|------------------------|-----------------------|
| | IEC | JEDEC | JEITA | | | |
| SOT402-1 | | MO-153 | | | | -99-12-27 03-02-18 |

Fig 11. Package outline SOT402-1 (TSSOP14)

13. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|--|
| CMOS | Complementary Metal Oxide Semiconductor |
| LSTTL | Low-power Schottky Transistor-Transistor Logic |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| CDM | Charge-Device Model |
| TTL | Transistor-Transistor Logic |

14. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---------------------|--|-----------------------|---------------|---------------------|
| 74HC_HCT107 v.4 | 20150126 | Product data sheet | - | 74HC_HCT107 v.3 |
| Modifications: | <ul style="list-style-type: none">Table 7: Power dissipation capacitance condition for 74HCT107 is corrected. | | | |
| 74HC_HCT107 v.3 | 20131118 | Product data sheet | - | 74HC_HCT107_CNV v.2 |
| Modifications: | <ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.Legal texts have been adapted to the new company name where appropriate. | | | |
| 74HC_HCT107_CNV v.2 | 19901201 | Product specification | - | - |

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| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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