DATA SHEET

74LVC1284

3.3V Parallel printer interface transceiver/buffer

Product specification

1995 Nov 10

IC24 Low Voltage Handbook

Philips Semiconductors

PHILIPS

3.3V Parallel printer interface transceiver/buffer 74LVC1284

FEATURES

- Asynchronous operation
- 4-Bit transceivers
- 3 additional buffer/driver lines
- TTL compatible inputs
- ESD protection exceeds 1000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Input Hysteresis
- Low Noise Operation
- Center Pin V_{CC} & GND
- IEEE 1284 Compliant Level 1 & 2
- Overvoltage Protection on B side

DESCRIPTION

The 74LVC1284 parallel interface chip is designed to provide an asynchronous, 4-bit, bi-directional, parallel printer interface for personal computers. Three additional lines are included to provide handshaking signals between the host and the peripheral. The part is designed to match IEEE 1284 standard.

The 4 transceiver pins (A/B 1-4) allow data transmission from the A bus to the B bus, or from the B bus to the A bus, depending on the state of the direction pin DIR.

The B bus and the Y5-Y7 lines have totem pole or open drain style outputs depending on the state of the high drive enable pin HD. The A bus only has totem pole style outputs. All inputs are TTL compatible with at least 300mV of input hysteresis at V_{CC} = 3.3V.

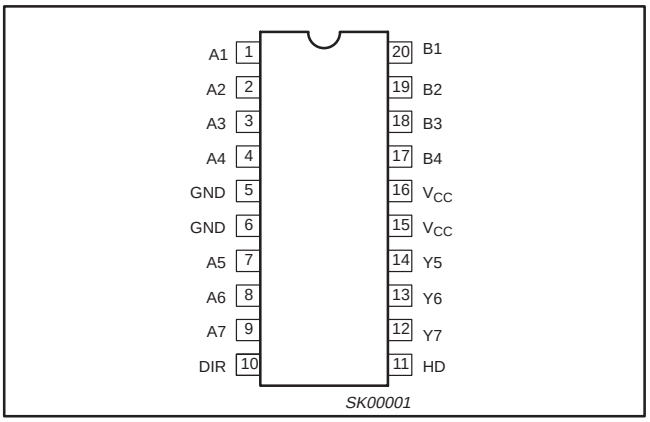
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
R_D	B/Y Side output resistance	V_{CC} = 3.3V; V_O = 1.65V ±0.2V (See Figure 2)	45	Ω
SR	B/Y Side slew rate	R_L = 62Ω; C_L = 50pF (See Waveform 4)	0.2	V/ns
I_{CC}	Total static current	V_I = V_{CC}/GND; I_O = 0	5	µA
V_{HYS}	Input hysteresis	V_{CC}= 3.3V	0.4	V
t_{PLH}/t_{PHL} A –B/Y	Propagation delay to the B/Y side outputs	V_{CC} = 3.3V	12.6/12.4	ns

ORDERING INFORMATION

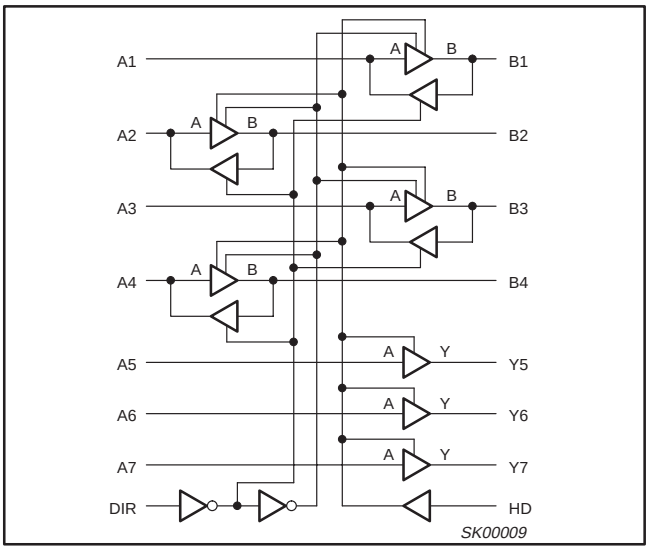
PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin plastic SO	0°C to +70°C	7LVC1284 D	SOT163-1
20-pin plastic SSOP Type II	0°C to +70°C	74LVC1284 DB	SOT339-1
20-pin plastic TSSOP Type I	0°C to +70°C	74LVC1284 PW	SOT360-1

PIN CONFIGURATION



SK00001

LOGIC SYMBOL



SK00009

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1,2,3,4	A1 - A4	Data inputs/outputs
20,19,18,17	B1 - B4	IEEE 1284 Std. outputs/inputs
7,8,9	A5 - A7	Data inputs
14,13,12	Y5 - Y7	IEEE 1284 Std. outputs
10	DIR	Direction selection
11	HD	B/Y–side high drive enable/disable
5,6	GND	Ground (0V)
15,16	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			OUTPUTS	INPUTS/OUTPUTS	
DIR	HD	A5-7	Y5-7	A1-4	B1-4
L	L	L	L	A = B	Inputs
L	L	H	Z	A = B	Inputs
L	H	L	L	A = B	Inputs
L	H	H	H	A = B	Inputs
H	L	L	L	Inputs Low	Outputs Low
H	L	H	Z	Inputs High	Outputs Z
H	H	L	L	Inputs	B = A
H	H	H	H	Inputs	B = A

H = High Voltage
L = Low Voltage
Z = High Impedance, Off-State

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
	ESD Immunity, per Mil Std 883C method 3015		±2	kV
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	±20	mA
I_{OK}	DC output diode current	$V_O < 0$	±50	mA
V_{IN}	DC input voltage[3]		–0.5 to +5.5	V
V_{OUT} B/Y_{DC}	DC output voltage on B/Y side[3]		–0.5 to +5.5	V
V_{OUT} B/Y (tr)	Transient output voltage on B/Y side[4]	40ns transient	–2 to +7	V
V_{OUT} A side	DC output voltage on A side		–0.5 to V_{CC} +0.5	V
I_O	DC output current	Outputs in High or Low state	±50	mA
T_{stg}	Storage temperature range		–60 to +150	°C
I_{CC}/I_{GND}	Continuous current through V_{CC} or GND		±200	mA

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
4. V_{OUT} B/Y (tr) guarantees only that this part will not be damaged by reflections in application so long as the voltage levels remain in the specified range.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	3.0	3.6	V
V_I	Input voltage	0	V_{CC}	V
V_{OUT}	B/Y output voltage	–0.5	5.5	V
V_{OUT}	A side output voltage	0	V_{CC}	V
I_{OH}	B/Y side output current High		–14	mA
I_{OL}	B/Y side output current Low		14	mA
T_{amb}	Operating free-air temperature range	0	+70	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = 25°C			T_{amb} = 0°C to +70°C		
				MIN	TYP	MAX	MIN	MAX	
V_{OH}	High-level output voltage	An	V_{CC} = Min to Max; I_{OH} = –50µA	V_{CC}–0.2	V_{CC}		V_{CC}–0.2		V
			V_{CC} = 3.0V; I_{OH} = –4mA	2.4			2.4		V
		Bn or Yn	V_{CC} = 3.0V; I_{OH} = 14mA	2.2	2.4		2.1		V
V_{OL}	Low-level output voltage	An	V_{CC} = Min to Max; I_{OL} = 50µA; V_I = V_{IL} or V_{IH}			0.2		0.2	V
			V_{CC} = 3.0V; I_{OL} = 4mA; V_I = V_{IL} or V_{IH}			0.4		0.4	V
		Bn or Yn	V_{CC} = 3.0V; I_{OL} = –14mA; V_I = V_{IL} or V_{IH}			0.8		0.9	V
V_{IH}	High-level input voltage		V_{CC} = Min to Max			0.8		0.8	
V_{IL}	Low-level input voltage		V_{CC} = Min to Max	2.0			2.0		
V_{HYS}	Input Hysteresis		V_{CC} = 3.3V		0.4		0.3		V
R_D	B/Y side Output Impedance		See Figure 2	38	45	53	35	55	Ω
I_I	Input leakage current (A5-A7 DIR, HD)		V_{CC} = 3.6V; V_O = V_{CC} or GND; Not for I/O pins			±1.0		±5.0	µA
I_{IHZ}/I_{ILZ}	Input current for common I/O pins		V_{CC} = 3.6V;V_I = 5.5V or GND		± 0.1	± 15			µA
I_{OFF}	B/Y Side Power-off leakage current		V_{CC} = 0.0V; V_O = 0 to 5.5V			±10		±100	µA
I_{OZH}	3-State output High current Yn		V_{CC} = 3.6V; V_O = V_{CC}; V_I = V_{IL} or V_{IH}			5		20	µA
I_{OZL}	3-State output Low current Yn		V_{CC} = 3.6V; V_O = GND; V_I = V_{IL} or V_{IH}			–5		–20	µA
$I_{IH}+I_{OZH}$	current (A1 – A4, Bn)		V_{CC} = 3.6V; $V_{I/O}$ = V_{CC}			5		25	µA
$I_{IL}+I_{OZL}$	current (A1 – A4, Bn)		V_{CC} = 3.6V; $V_{I/O}$ = GND			–5		–25	µA
I_{CC}	Quiescent Supply Current		V_{CC} = 3.6V; I_O = 0; V_I = GND or V_{CC}		5	10		50	µA

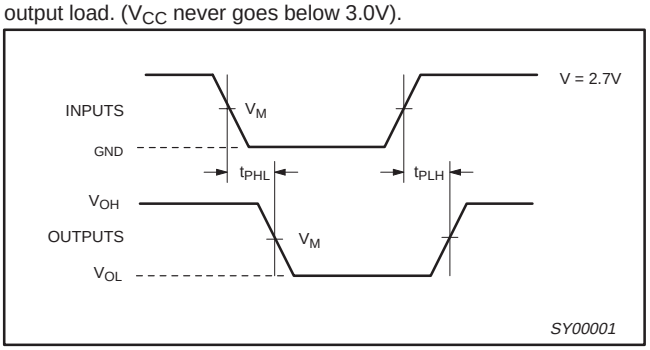
AC CHARACTERISTICS

GND = 0V, t_R = t_F = 3.0ns, C_L = 50pF, R_L = 500Ω

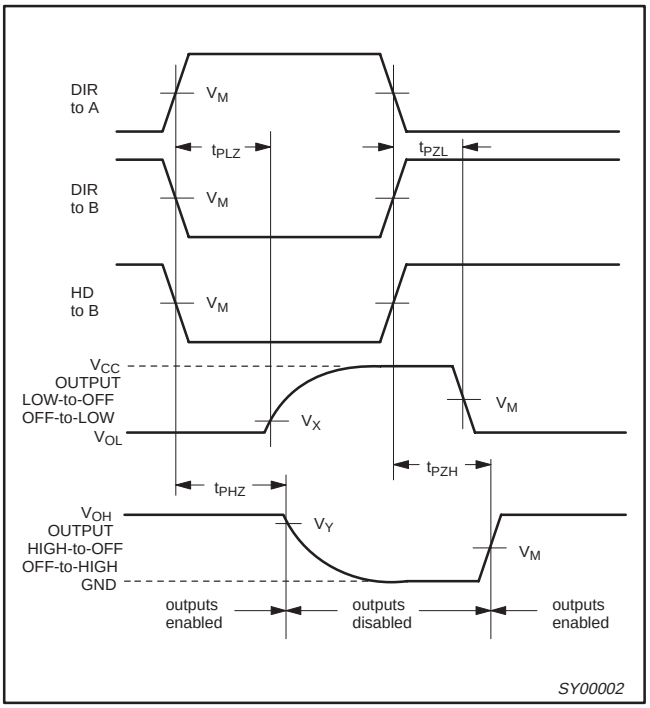
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = 25°C V_{CC} = 3.3V			T_{amb} = 0 to + 70°C V_{CC} = Min to Max		
			MIN	TYP	MAX	MIN	MAX	
SR	B-Side Slew Rate	4	0.05	0.2	0.35	0.05	0.4	V/ns
t_{PLH} t_{PHL}	Propagation delay A toY or A to B	5	6.0 6.0	12.6 12.4	18.0 18.0	5.0 5.0	19.5 20.0	ns
t_{PLH} t_{PHL}	Propagation delay B to A	1	1.5 1.5	5.5 5.6	7.9 7.6	1.5 1.5	9.5 9.0	ns
t_{PZH} t_{PHZ}	Output enable/disable time to/from High level HD to Y or HD to B	2	4.0 2.0	12.0 6.5	16.0 9.1	4.0 2.0	20.0 11.0	ns
t_{PZL} t_{PLZ}	Output enable/disable time to/from Low level A to Y or A to B	2	5.0 1.5	12.7 5.0	16.3 7.1	5.0 1.5	20.0 9.0	ns
t_{PZH} t_{PZL}	Output enable time from DIR to B	2	8.0 8.0	12.3 12.7	18.0 18.0	4.0 4.0	20.0 20.0	ns
t_{PHZ} t_{PLZ}	Output disable time from DIR to B	2	5.0 6.0	8.9 9.1	12.5 12.0	2.0 2.0	14.5 14.0	ns
t_{PZH} t_{PZL}	Output enable time from DIR to A	2	3.5 4.0	6.9 8.6	13.0 14.0	3.0 3.0	14.5 16.0	ns
t_{PHZ} t_{PLZ}	Output disable from DIR to A	2	2.5 2.5	3.7 3.7	5.5 5.0	2.0 2.0	6.0 5.5	ns

AC WAVEFORMS

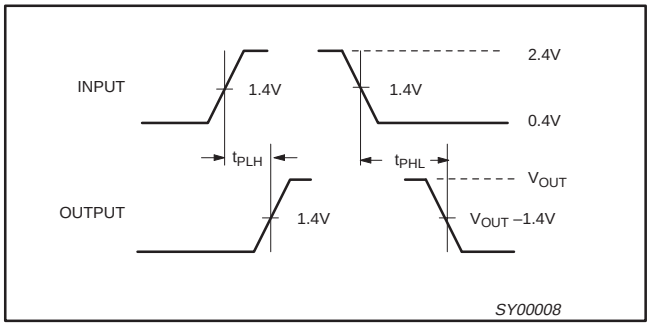
V_M = 1.5V
$V_X = V_{OL} \pm 0.3V$
$V_Y = V_{OH} - 0.3V$
V_{OL} and V_{OH} are the typical output voltage drops that occur with the output load. (V_{CC} never goes below 3.0V).



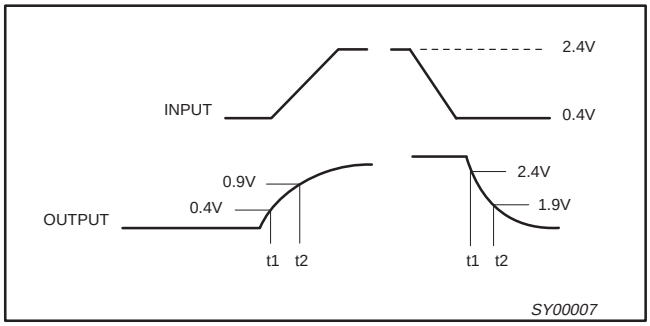
Waveform 1. Input Bn to output An propagation delays



Waveform 2. 3-State enable and disable times



Waveform 3. Voltage Waveforms Propagation Delay Times (A To B) Measured at Output Pin



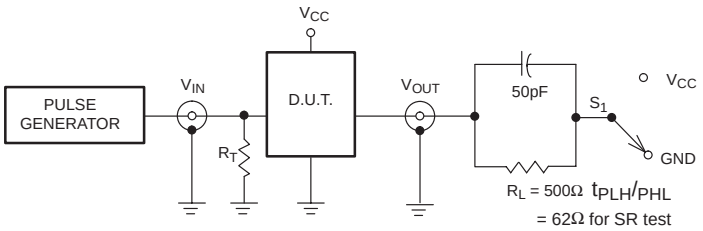
Waveform 4. Slew Rate Waveforms Voltage Waveforms

(Input pulse rise and fall time are 3ns, 150ns < pulse width < 10 µs, for both a Low to High and a High to Low transition.)

Slew Rate measured between 0.4V and 0.9V - rising.

Slew Rate measured between 2.4V and 1.9V - falling.

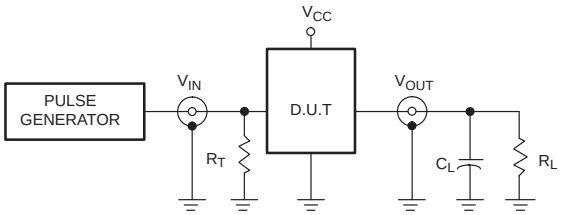
Slew Rate measured at TP1.



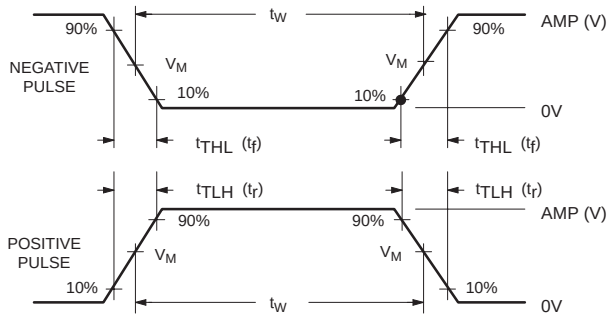
Test Circuit for B_n or Y_n Outputs

SWITCH POSITION
Bn or Yn Outputs

TEST	SWITCH
t_{PLH} t_{PHL}	GND V_{CC}



Test Circuit for A_n Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

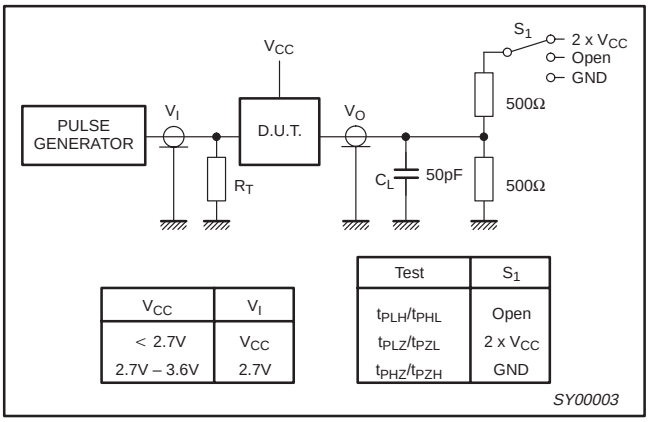
R_L = Load resistor; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_r	t_f
74LVC	3.0V	1MHz	500ns	3ns	3ns

SY00004

Waveform 5.



V_{CC}	V_I
< 2.7V	V_{CC}
2.7V – 3.6V	2.7V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

Figure 1. Load Circuitry for Bn to An Switching Times

TEST CIRCUIT

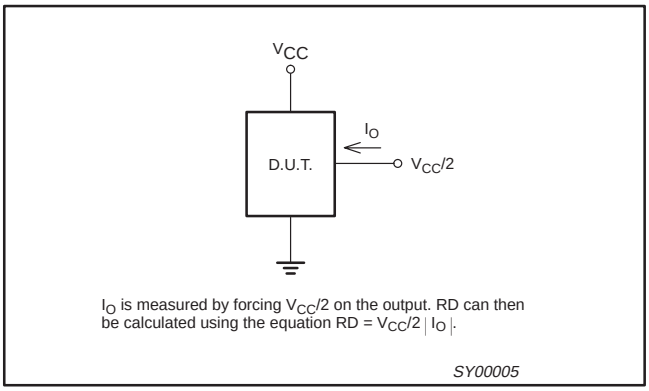
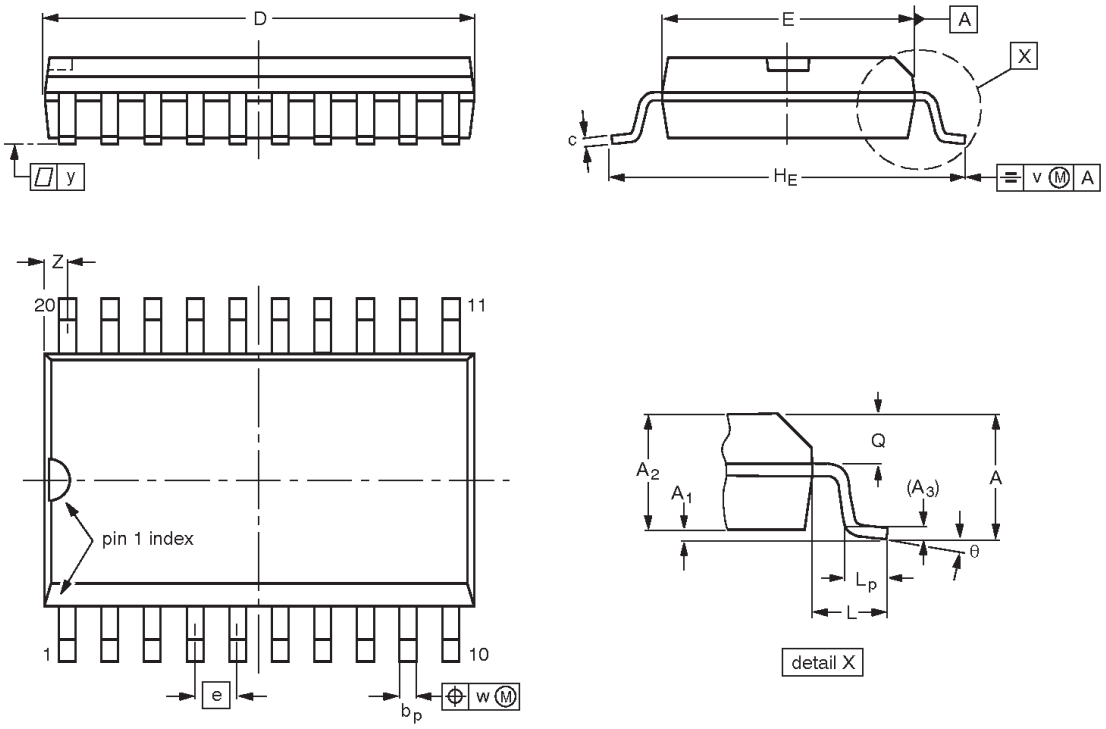
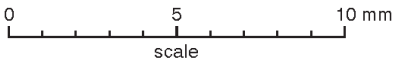


Figure 2. Output Impedance RD

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

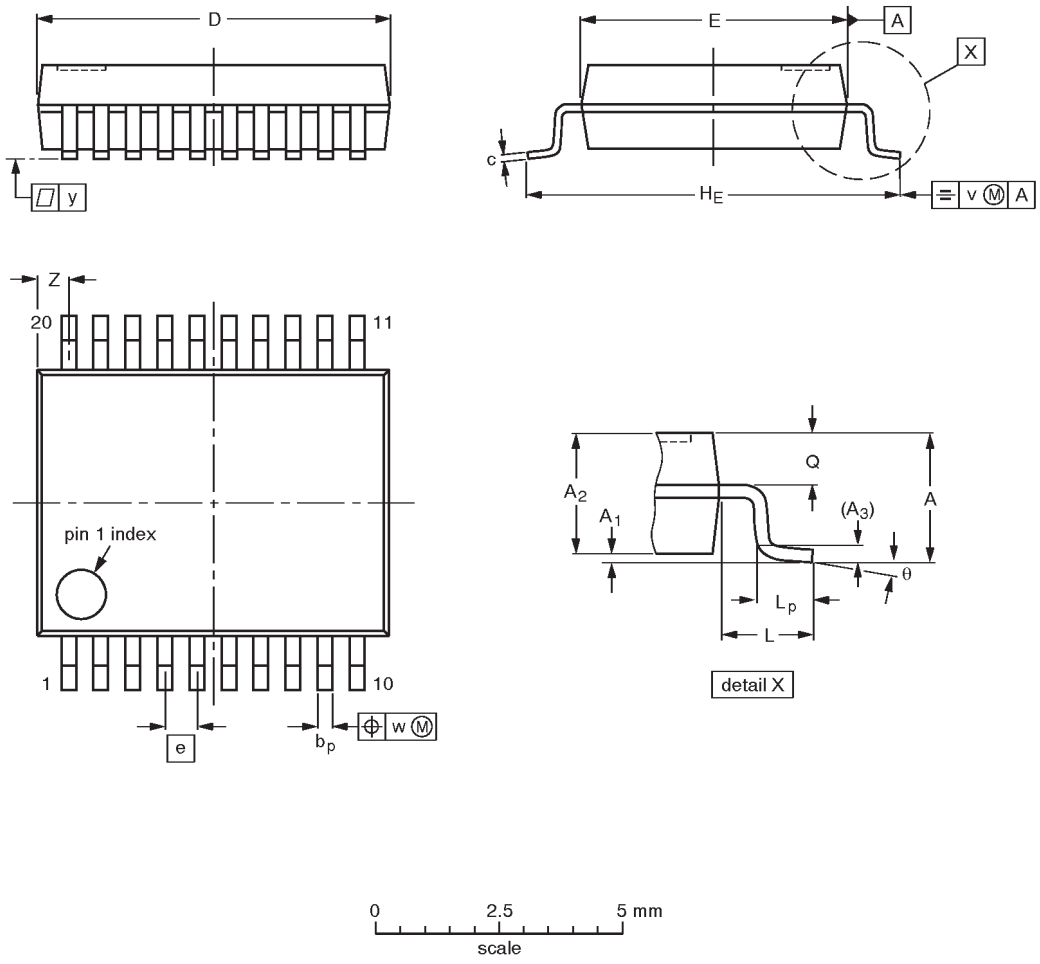
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**



DIMENSIONS (mm are the original dimensions)

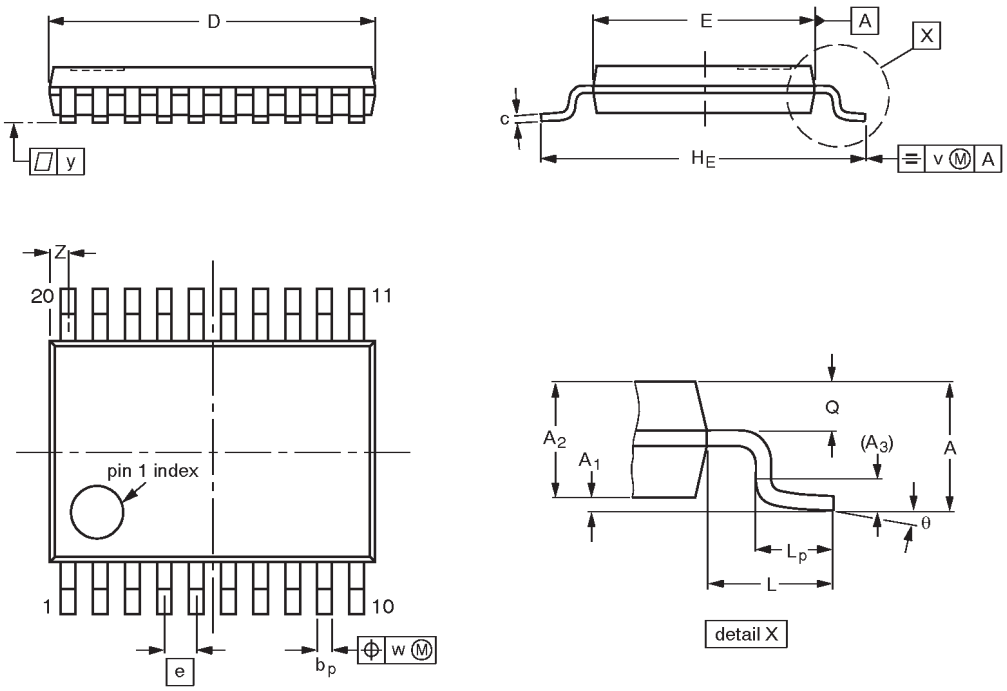
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

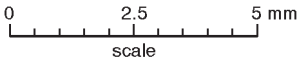
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				~~93-09-08~~ 95-02-04

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				~~93-06-16~~ 95-02-04

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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